THERMAL RESISTANCE

This manual explains about measurement procedures and definitions of thermal resistance.

■INTRODUCTION

Generally, the life of a device would decrease to half, and the failure rate would double whenever Junction Temperature, Tj, goes up by 10°C. Moreover, when Tj exceeds 175°C, a device has the possibility of breaking.
Therefore, it is necessary to keep Tj in the proper temperature range, which is the lower the better, and a heat design should be done under the condition of the range of 80-100°C.
In fact, it is difficult for IC packages that handle high power to keep Tj in this range. Therefore, it is common to make Tj the 80% of a maximum permissible temperature.
A value of a thermal resistance is dependent on a chip, a layout of a leadframe, a board, and so forth. It means even if sizes of the IC packages are the same and layouts of leadframes are different, thermal resistances are not the same.

■DEFINITIONS

The thermal resistance of a IC package is calculated by the difference between Tj and the ambient Temperature, Ta, under the condition that the IC package dissipates electric power of 1W.
Here are three expressions of the thermal resistance, and each term of expressions are defined in Table1 and Fig.1.

$$\theta ja = \frac{Tj - Ta}{Pd}$$

$$\psi jt = \frac{Tj - T_{C1}}{Pd}$$

$$\theta jc = \frac{Tj - T_{C2}}{Pd}$$

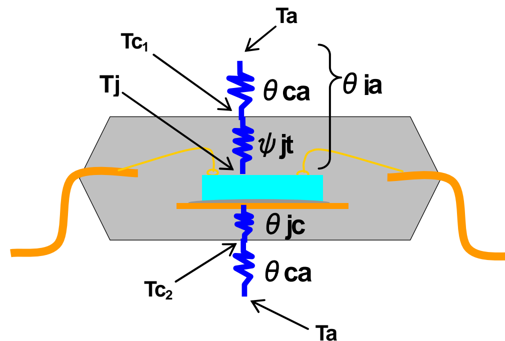


Fig.1 Thermal resistances of a IC package

Table1 Definitions

Item	Definitions
θ ja	thermal resistance between Tj and Ta
ψ jt	thermal resistance between Tj and T_{C1}
θ jc	thermal resistance between Tj and T_{C2}
θ ca	thermal resistance between Tc and Ta
Tj	junction temperature
Ta	ambient temperature
T_{C1}	temperature of the top surface of IC package
T_{C2}	temperature of the bottom surface of IC package
Pd	maximum permissible power

■Estimation of Tj when ψjt is known

Tj can be estimated by following order

1. Power, P, is calculated by operating current and voltage.
2. Tc_1 is measured by using a thermometer like a radiation thermometer and thermocouples.
3. Tj is calculated by Tc_1, and ψjt which is shown in Table 3.

$$Tj = \psi jt \times P + T_{C1}$$

Note) θja and ψjt in Table 3 are measured values based on JEDEC with no wind.
Each value is dependent on a chip, a layout of a leadframe, a board, and so forth.

■Measurement of Thermal Resistance

The measurement of thermal resistance is based on JEDEC.

[Test board]
The outline of the measurement board is shown in Fig.2, which is based on JEDEC.

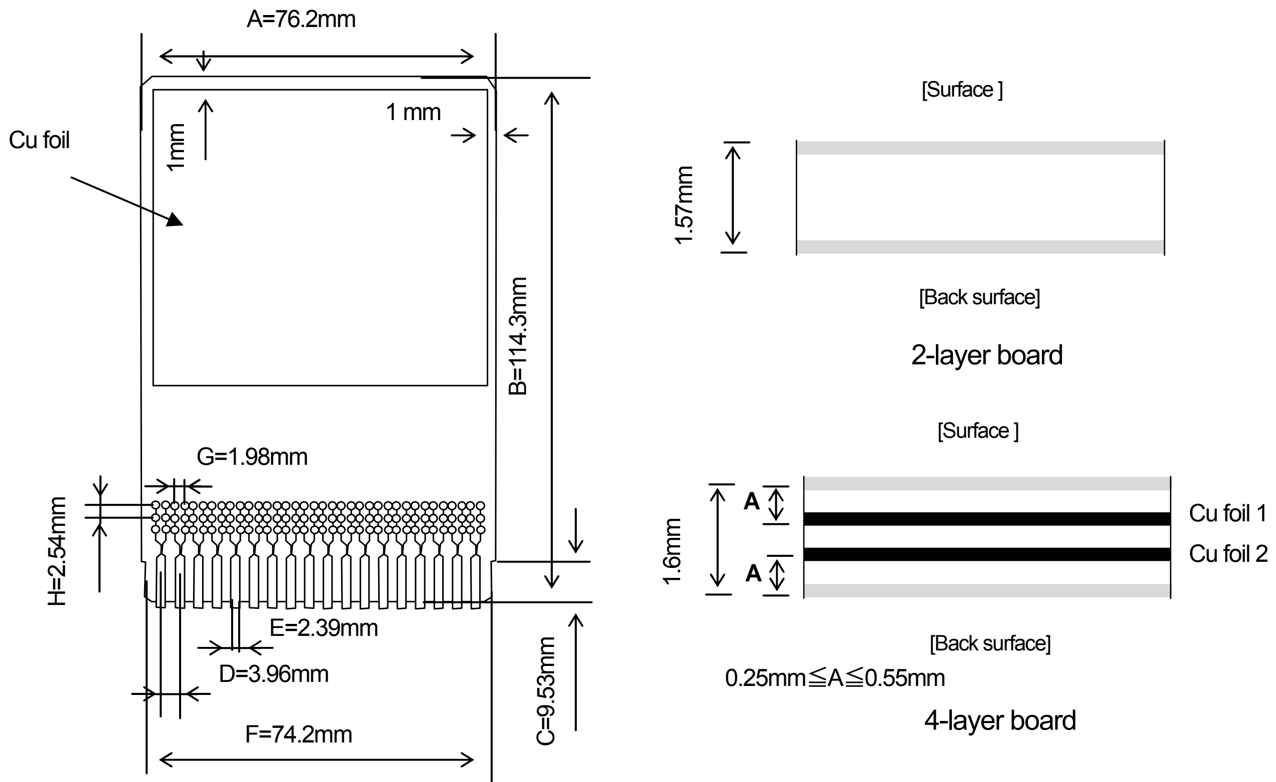


Fig.2 Measurement board

Note)

Board material	: FR-4
Board dimension	:(2-layer board) 114.3×76.2mm,Thickness 1.57mm
	:(4-layer board with Cu foil 1,2) 114.3×76.2mm,Thickness 1.6mm
Cu foil dimension	:74.2x74.2mm (Thickness 35um) are applied to 4-layer board, as Cu foil 1, 2.

[Chip for measurement of Thermal Resistance]

A chip is composed of elements of a resistance and a diode. The resistance is used for heating, and the diode is for a sensor of temperature. We have three kinds of size, because thermal resistance is dependent on a chip size.

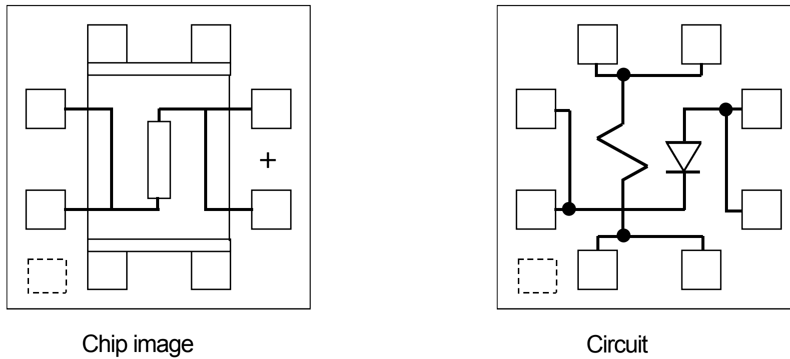


Fig.3 Image of the chip

[Measurement of K factor]

Tj cannot be measured directly. However, by a character of a forward voltage, V_F, of a diode is dependent on temperature. Therefore, Tj is known during a measurement by measuring V_F.

However, dependency of diode which called K-factor, K, should be measured first.

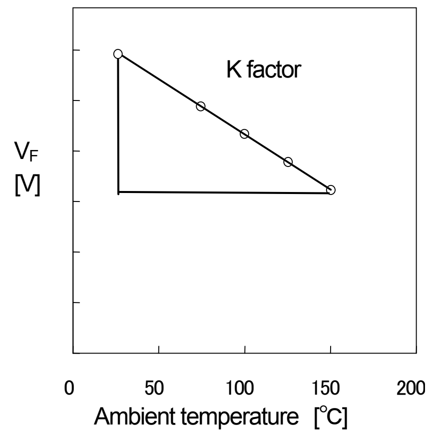
$$K = \left| \frac{\Delta Tj}{\Delta V_F} \right| \ [^\circ C/mV] \qquad \Delta Tj = T_{Hi} - T_{Lo}$$

$$\Delta V_F = V_{Hi} - V_{Lo}$$

where

V_{Hi} : voltage at T_{Hi}

V_{Lo} : voltage at T_{Lo}



[JEDEC chamber]

JEDEC chamber with no wind condition (still air) is adopted.

The ambient temperature is measured with thermocouples at the position that is located 25.4mm below the center of the IC package.

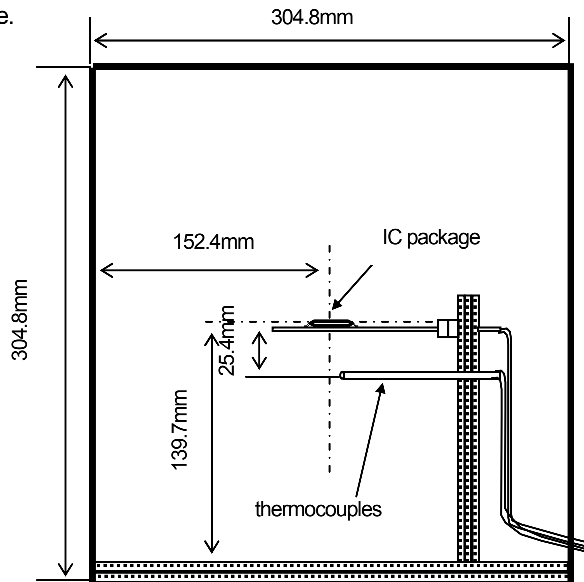


Fig.4 JEDEC chamber

[Measurement circuit]

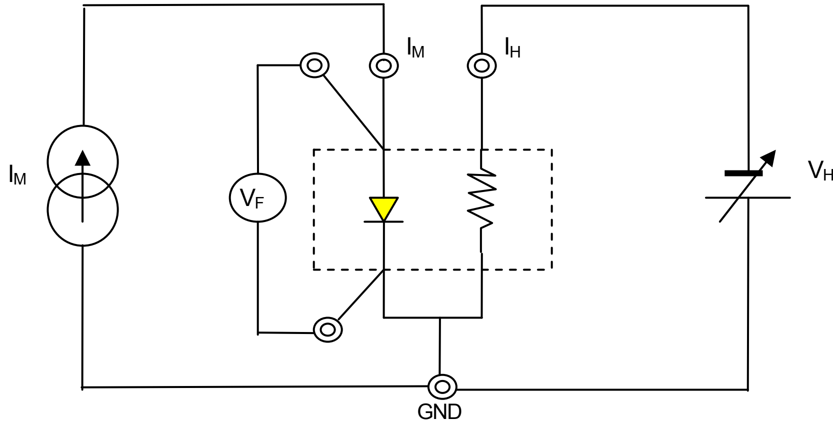


Fig.5 Measurement circuit

[Measurement procedure]

1. V_{F0} is measured by giving the diode with a current (1mA), I_M, at the ambient temperature.
2. A Voltage, V_H, is given to the resistance in the chip until temperature at upper surface of the IC package, which is measured with a radiation thermometer, is saturated. After confirming the saturation, I_H is read.
3. V_{FSS} is measured by giving the diode with a current, I_M.

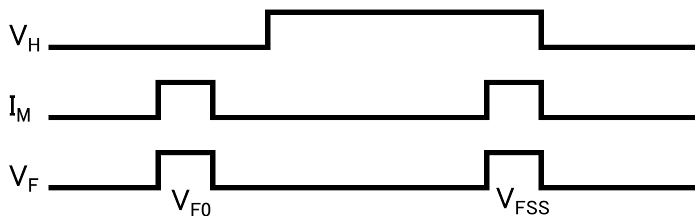


Fig.6 Timing of measurement

Note) V_H is measured at three points, the voltage of Tstg-max, Vstg-max, and lower and higher than Vstg-max.

[Calculation]

θ ja and ψ jt are calculated from the following Table 2.

Table 2 Thermal resistance calculation

Thermal resistance calculation
[θ ja] $\theta ja = \frac{\Delta Tj}{V_H \times I_H} = \frac{K \times \Delta V_F}{V_H \times I_H}$ [°C/W] , where $\Delta V_F = V_{F0} - V_{FSS}$
[ψ jt] $\psi jt = \frac{(\Delta Tj + Ta) - T_{C1}}{V_H \times I_H} = \frac{(K \times \Delta V_F + Ta) - T_{C1}}{V_H \times I_H}$ [°C/W] , where $\Delta V_F = V_{F0} - V_{FSS}$
where V_H : voltage given to the resistance in the chip I_H : current when temperature at the upper surface of the IC package is saturated

[The Permissible Regions of Dissipated Power]
Pd is the maximum permissible power at Ta=25°C.
Pd is dependent on the ambient temperture, which is shown in Fig.7.

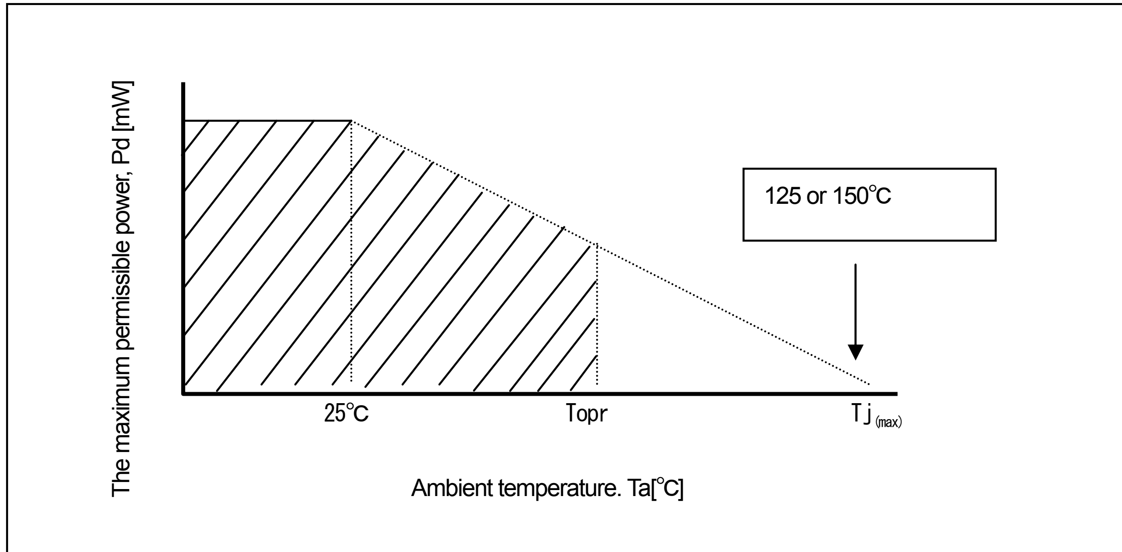


Fig.7 The maximum permissible power

■Thermal Resistance of each package

There are typical measured value based on JEDEC with no wind. Each value is dependent on a chip, a layout of a leadframe, a board, and so forth.

Table 3 Thermal resistance of each package

PKG	2 layer board				4 layer board			
	Tj:125℃			Tj:150℃	Tj:125℃			Tj:150℃
	θja (℃/W)	Ψjt (℃/W)	Pd (mW)	Pd (mW)	θja (℃/W)	Ψjt (℃/W)	Pd (mW)	Pd (mW)
DMP8	235	47	425	530	175	40	570	710
DMP14	195	47	510	640	150	40	665	830
DMP16	195	47	510	640	150	40	665	830
DMP20	150	37	665	830	120	33	830	1040
SOP8 JEDEC(EMP8)	180	34	555	690	125	29	800	1000
SOP16 JEDEC(EMP16-E2)	110	21	905	1135	70	18	1425	1785
SOP8	165	26	605	755	110	23	905	1135
SOP14	125	21	800	1000	80	17	1250	1560
SOP22	120	18	830	1040	85	14	1175	1470
SOP28	155	37	645	805	125	33	800	1000
SOP40-K1	135	37	740	925	105	33	950	1190
SSOP8	270	42	370	460	210	36	475	595
SSOP8-A3	215	36	465	580	155	15	645	805
SSOP10	270	42	370	460	210	36	475	595
SSOP14	225	38	440	555	180	33	555	690
SSOP16	210	35	475	595	160	26	625	780
SSOP20	185	34	540	675	140	26	710	890
SSOP20-B2	200	34	500	625	150	26	665	830
SSOP20-C3	130	13	765	960	85	9	1175	1470
SSOP32	110	20	905	1135	70	14	1425	1785
SSOP44	110	20	905	1135	70	14	1425	1785
TSSOP54-N1	105	10	950	1190	75	9	1330	1665
HSOP8[2)]	160	28	625	780	50	12	2000	2500
HTSSOP24-P1	115	14	865	1085	45	7	2220	2775
MSOP8(TVSP8)	215	27	465	580	160	23	625	780
MSOP10(TVSP10)	215	27	465	580	160	23	625	780
MSOP8(VSP8)	210	33	475	595	155	25	645	805
MSOP10(VSP10)	210	33	475	595	155	25	645	805
SC-82AB	365	89	270	340	255	72	390	490
SC-88A	355	89	280	350	260	73	380	480
SOT-23-5	260	70	380	480	195	60	510	640
SOT-23-6	245	70	405	510	175	60	570	710
SOT-89-3[1)2)]	200	67	500	625	130	65	765	960
QFP32-J2	115	17	865	1085	90	15	1110	1385
QFP44-A1	95	17	1050	1315	75	15	1330	1665
QFP48-P1	65	17	1535	1920	50	15	2000	2500
LQFP48-R3	75	9	1330	1665	45	5	2220	2775
LQFP52-H2	85	11	1175	1470	65	11	1535	1920
QFP56-A1	105	17	950	1190	80	15	1250	1560
QFP64-H1	70	17	1425	1785	50	15	2000	2500
LQFP64-H2	65	6	1535	1920	50	5	2000	2500
QFP100-U1	55	5	1815	2270	45	5	2220	2775
TO-252-3[1)2)]	105	17	950	1190	40	12	2500	3125
PLCC28	55	10	1815	2270	35	7	2855	3570

THERMAL RESISTANCE

PKG	2 layer board				4 layer board			
	Tj:125℃			Tj:150℃	Tj:125℃			Tj:150℃
	θja (℃/W)	Ψjt (℃/W)	Pd (mW)	Pd (mW)	θja (℃/W)	Ψjt (℃/W)	Pd (mW)	Pd (mW)
EPFFP6-A2 2)	370	59	270	335	220	53	450	565
EPFFP10-C4 2)	295	64	335	420	160	55	625	780
PCSP12-C3	240	40	415	520	140	33	710	890
PCSP20-CC	225	40	440	555	140	33	710	890
PCSP20-E3	225	40	440	555	130	33	765	960
PCSP24-ED	205	40	485	605	115	26	865	1085
PCSP32-F7	225	24	440	555	115	17	865	1085
PCSP32-G3 2)	205	24	485	605	115	17	865	1085
PCSP32-GD 2)	205	24	485	605	115	17	865	1085
EPCSP32-L2 2)	210	29	475	595	95	16	1050	1315
DFN6-J1 (SON6-J1)	345	88	285	360	260	69	380	480
DFN4-F1(ESON4-F1) 2)	300	52	330	415	110	27	905	1135
DFN6-H1(ESON6-H1) 2)	280	42	355	445	110	26	905	1135
DFN8-U1(ESON8-U1) 2)	280	43	355	440	110	26	905	1135
DFN8-V1(ESON8-V1) 2)	215	16	465	580	70	8	1425	1785
DFN8-W2(ESON8-W2) 2)	195	21	510	640	60	8	1665	2080
QFN24-T1/T2	150	22	665	830	75	15	1330	1665
EQFN12-E2 2)	285	52	350	435	105	27	950	1190
EQFN12-E4 2)	285	52	350	435	105	27	950	1190
EQFN14-D7 2)	295	53	335	420	95	26	1050	1315
EQFN16-G2 2)	255	43	390	490	100	26	1000	1250
EQFN12-JE 2)	215	22	465	580	80	10	1250	1560
EQFN16-JE 2)	180	21	555	690	70	11	1425	1785
EQFN18-E7 2)	220	33	450	565	90	22	1110	1385
EQFN26-HH 2)	160	15	625	780	60	7	1665	2080
EQFN24-LK 2)	145	13	685	860	65	8	1535	1920

Notes：

1) Thermal resistance values (θja, ψjt) are measured with the 2-layer board having 100mm^2 copper foil, which is based on JEDEC.

2) Thermal resistance values (θja, ψjt) are measured with the 4-layer board having thermal via holes, which is also based on JEDEC.

■Thermal Resistance depending on area of Cu foil

There are typical values by mounting on five kinds of boards, "PAT.1" through "PAT.5", shown in Table 4 and Table 5.
Those are 2-layer boards based on JEDEC. However, they do not have any thermal via holes.

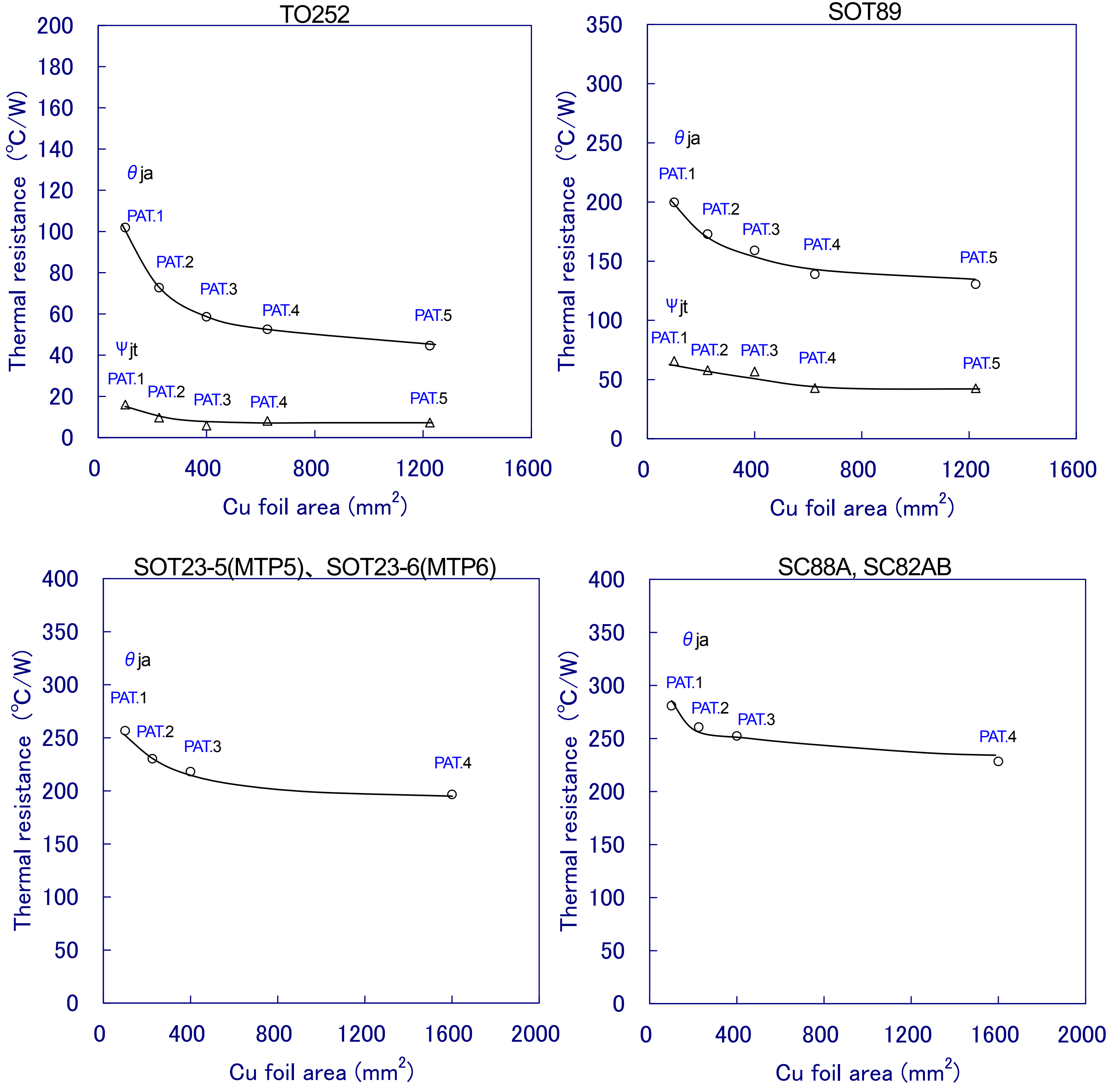


Fig.8 Thermal Resistance depending on area of Cu foil

Table 4 Image of Cu foil

Cu foil \ Package	TO252	SOT89	SOT23-5(MTP5) SOT23-6(MTP6)
PAT.1	Foot pattern → ; Area of Cu foil		
PAT.2			
PAT.3			
PAT.4			
PAT. 5			–

Table 5 Image of Cu foil

Cu foil \ Package	SC88A SC82AB
PAT.1	
PAT.2	
PAT.3	
PAT.4	

Table 6 Area of Cu foil

Cu foil \ Package	TO252	SOT89	SOT23-5(MTP5) SOT23-6(MTP6)	SC88A SC82AB
PAT.1	100 mm^2			
PAT.2	225 mm^2			
PAT.3	400 mm^2			
PAT.4	600 mm^2		1600 mm^2	
PAT.5	1225 mm^2		-	