Designated client product

This product will be discontinued its production in the near term.
And it is provided for customers currently in use only, with a time limit.
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2-CHANNEL ELECTRONIC VOLUME WITH INPUT SELECTOR

■ GENERAL DESCRIPTION

NJW1154 is a two channel electronic volume with 6 in 1 out selector IC. It's suitable for Input signal trimmer of audio equipments such as DVD recorder and VCR. These functions are controlled by I^2C Bus.

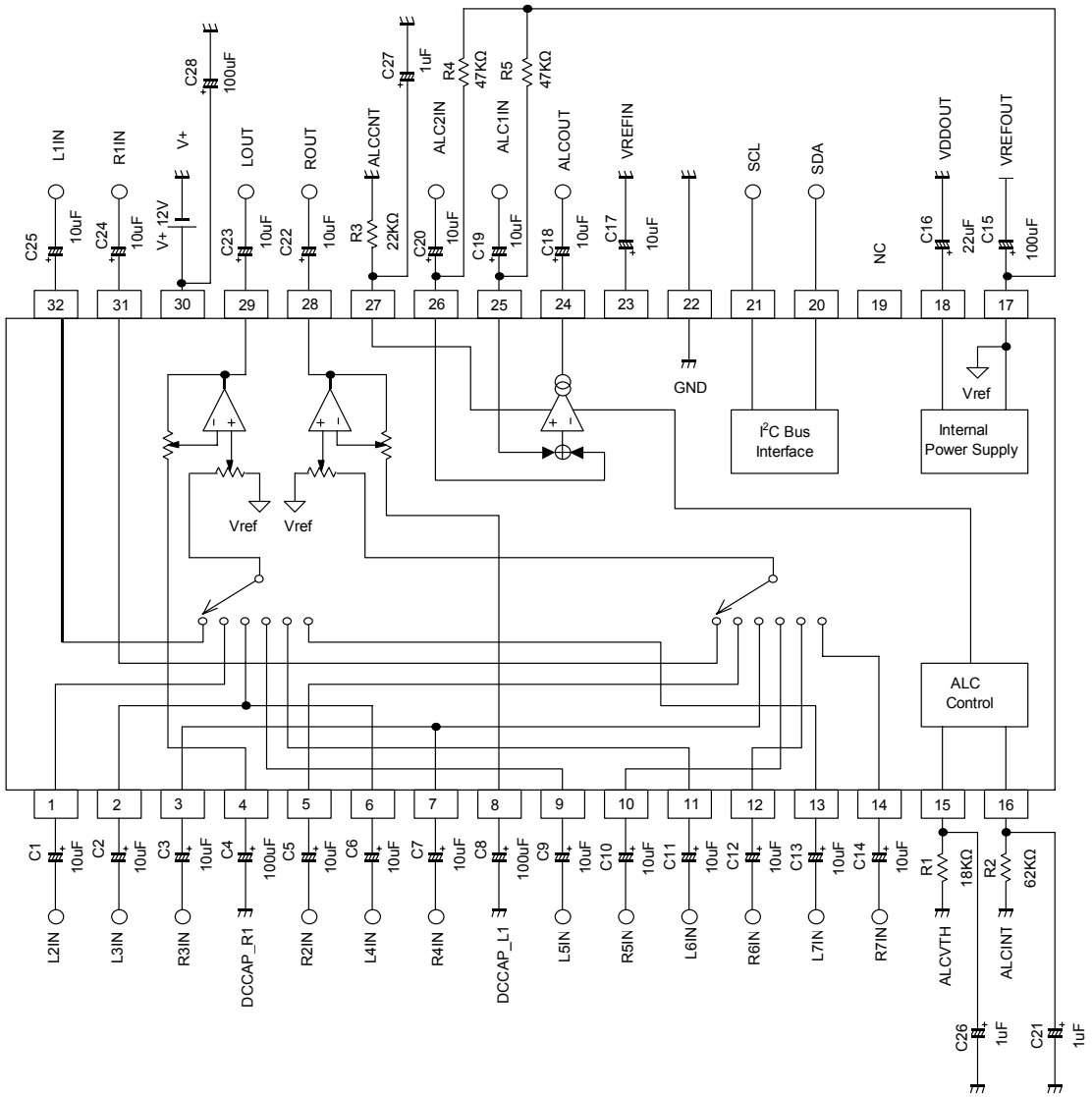
■ PACKAGE OUTLINE

NJW1154V

■ FEATURES

- Operating Voltage 8 to 13V
- I^2C Bus control
- 6in 1out Input Selector
- Volume +12 to -12dB/3dBstep, MUTE
- Bi-CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



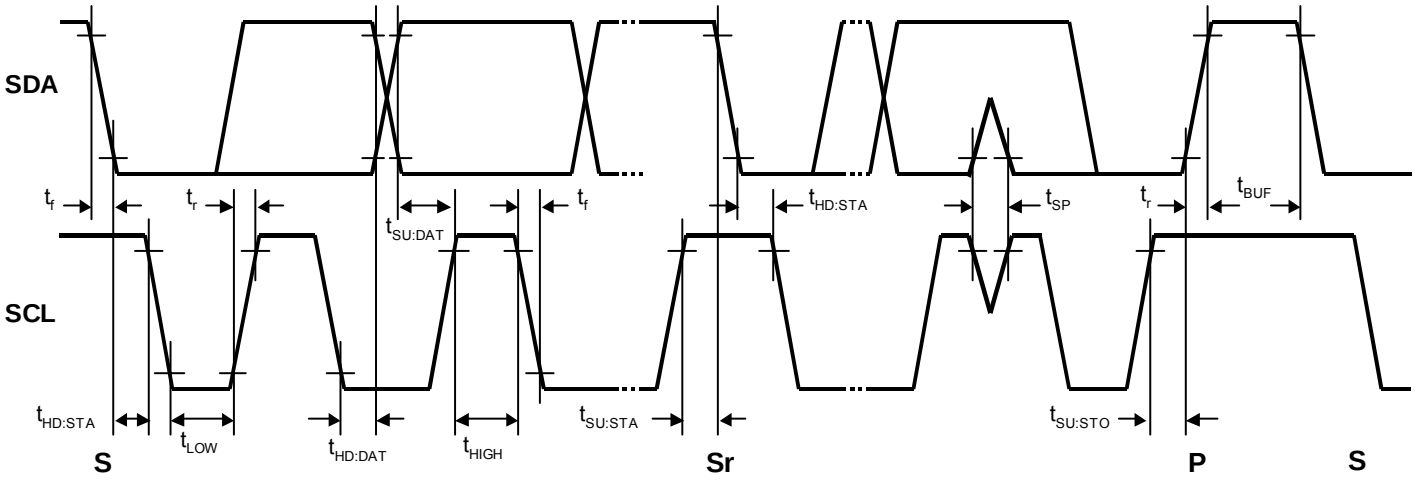
■ **ABSOLUTE MAXIMUM RATING (Ta=25°C)**

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V+	15	V
Power Dissipation	P_D	800 NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ **ELECTRICAL CHARACTERISTICS (Ta=25°C,V^+=+12V, R_L=47kΩ)**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
◆ Power Supply						
Operating Voltage	V+		8	12	13	V
Reference Voltage	V_{ref}		5.5	6	6.5	V
Supply Current	I_{CC}	No signal	-	7	9	mA
◆ Input/Output Characteristics (Output)						
Maximum Output Voltage	V_{OM}	f=1KHz,THD=1% Volume=0dB	3.2	3.7	-	Vrms
Voltage Gain 1	G_{V1}	V_{IN}=1Vrms, f=1kHz Volume=0dB	-0.5	0	0.5	dB
Voltage Gain 2	G_{V2}	V_{IN}=0.25Vrms, f=1kHz Volume=+12dB	+11	+12	+13	dB
Voltage Gain 3	G_{V3}	V_{IN}=2.5Vrms, f=1kHz Volume=-12dB	-13	-12	-11	dB
Voltage Gain Error 1	ΔG_{V1}	V_{IN}=0.25Vrms, f=1kHz Volume=+12dB , Ach - Bch	-0.5	0	0.5	dB
Voltage Gain Error 2	ΔG_{V2}	V_{IN}=2.5Vrms, f=1kHz Volume=-12dB , Ach - Bch	-0.5	0	0.5	dB
Maximum Attenuation	A_{TT}	f=1KHz, V_{IN}=1Vrms Volume=Mute, A-weighted	-	-110	-	dB
Output Noise	V_{NO}	Volume=0dB, Rg=0,A-weighted	-	-114 (2μ)	-100 (10μ)	dBV (Vrms)
Total Harmonic Distortion	T.H.D	f=1KHz,Vo=1Vrms, Volume=0dB, BW:400 – 30kHz	-	0.001	0.05	%
Cross Talk	CT	Selected Input : No signal Rg=0Ω Unselected Input : Input signal A-weighted	-	-100	-	dB
Channel Separation	CS	f=1KHz,Vo=1Vrms,A-weighted Volume=0dB	-	-100	-90	dB
◆ ALC						
Flat Level	ALC_{FLT}	Vin = 300mVrms	-	0	-	dB
ALC Cut Level	ALC_{CUT}	Vin = 2Vrms	-	-12	-	dB

■TIMING ON THE I²C BUS (SDA,SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA,SCL)

I²C BUS Load Conditions

STANDARD MODE: Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			UNIT
		MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	3.0	-	5.0	V
Low level output voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	-10	-	10	μA

■CHARACTERISTICS OF BUS LINES (SDA,SCL) FOR I²C-BUS DEVICES

PARAMETER	SYMBOL	Standard mode			UNIT
		MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	-	-	100	kHz
Hold time (repeated) START condition.	$t_{HD:STA}$	4.0	-	-	µs
Low period of the SCL clock	t_{LOW}	4.7	-	-	µs
High period of the SCL clock	t_{HIGH}	4.0	-	-	µs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	µs
Data hold time NOTE)	$t_{HD:DAT}$	0	-	-	µs
Data set-up time	$t_{SU:DAT}$	250	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	µs
Capacitive load for each bus line	C_b	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	V

C_b ; total capacitance of one bus line in pF.

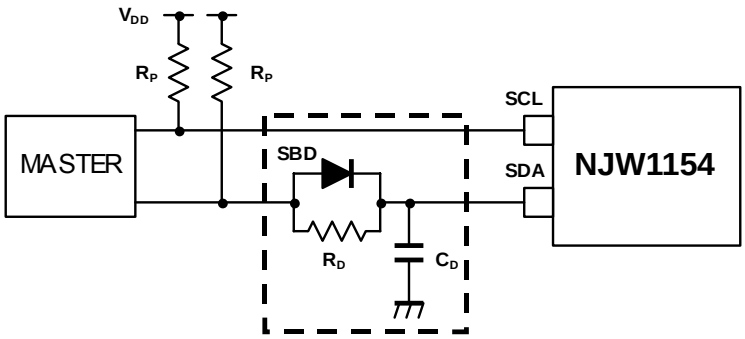
NOTE). Data hold time : $t_{HD:DAT}$

Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

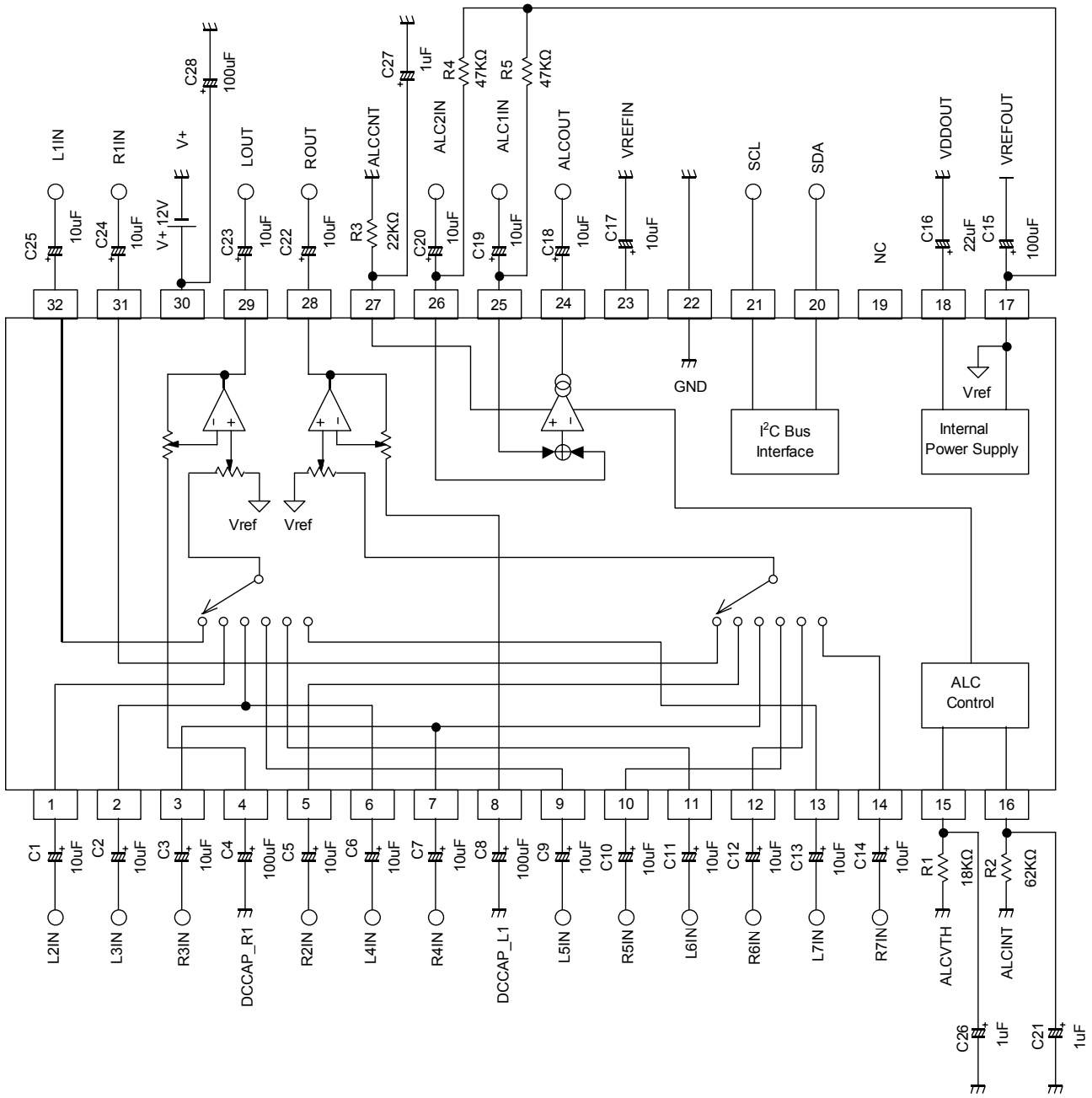
The SDA block in the NJW1154 does not hold data. Add external data-delay-circuit of the SDA terminal, in case of not providing a hold time of at least 300nsec for the SDA in the master device.
The time-consists of the data-delay-circuit of the SDA terminal are as follows.

(a) Low level → High level: $T_{LH} \approx R_P * C_D$
(b) High level → Low level: $T_{HL} \approx R_D * C_D$

In addition, Schottky barrier diode (SBD) influences a Low level at the Acknowledge. Therefore choose the low forward voltage (Vf) as much as possible.



■ APPLICATION CIRCUIT



■ DEFINITION OF I²C REGISTER

♦I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

♦SLAVE ADDRESS

MSB							LSB
1	0	0	0	0	0	1	R/$\overline{W}$

R/$\overline{W}$=0: Receive Only
R/W=1: No Output Data

♦CONTROL REGISTER TABLE

The select address sets each function (Volume, Selector).
The auto increment function cycles the select address as follows.
00H→01H→02H→00H

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Don't Care				VOLa			
01H	Don't Care				VOLb			
02H	Don't Care					Selector		

♦CONTROL REGISTER DEFAULT VALUE

Control register default values are as follows :

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	1	1	1	1	1	1	1	1
01H	1	1	1	1	1	1	1	1
02H	0	0	0	0	0	0	0	0

■ CONTROL COMMAND TABLE

a) Master Volume

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Don't Care				VOLa			
01H	Don't Care				VOLb			

•VOLa / VOLb : Ach and Bch volume level setting from +12dB to -12dB with 3dB step.

	VOLa / VOLb			
Gain (dB)	D3	D2	D1	D0
+12	0	0	0	0
+9	0	0	0	1
+6	0	0	1	0
+3	0	0	1	1
0	0	1	0	0
-3	0	1	0	1
-6	0	1	1	0
-9	0	1	1	1
-12	1	0	0	0
Mute	1	1	1	1

b)Input Selector

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
02H	Don't Care					Selector		

•Selector : Input signal selecting

	Selector		
Input	D2	D1	D0
L1IN / R1IN	0	0	0
L2IN / R2IN	0	0	1
L3IN, L4IN / R3IN, R4IN	0	1	0
L5IN / R5IN	0	1	1
L6IN / R6IN	1	0	0
L7IN / R7IN	1	0	1