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New Japan Radio Co.,Ltd.

<http://www.njr.com/>

## Low Dropout Voltage Regulator with Reset

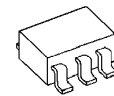
### ■ GENERAL DISCRIPTION

The NJU7271 is a low drop out voltage regulator with output-monitor reset function. Advanced CMOS technology achieves ultra low current consumption and high accuracy.

It delivers up to 5V/100mA output power with the maximum input voltage of 9V.

The NJU7270 is suitable for MPU applications.

### ■ PACKAGE OUTLINE

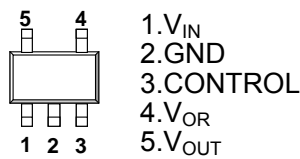


NJU7271F

### ■ FEATURES

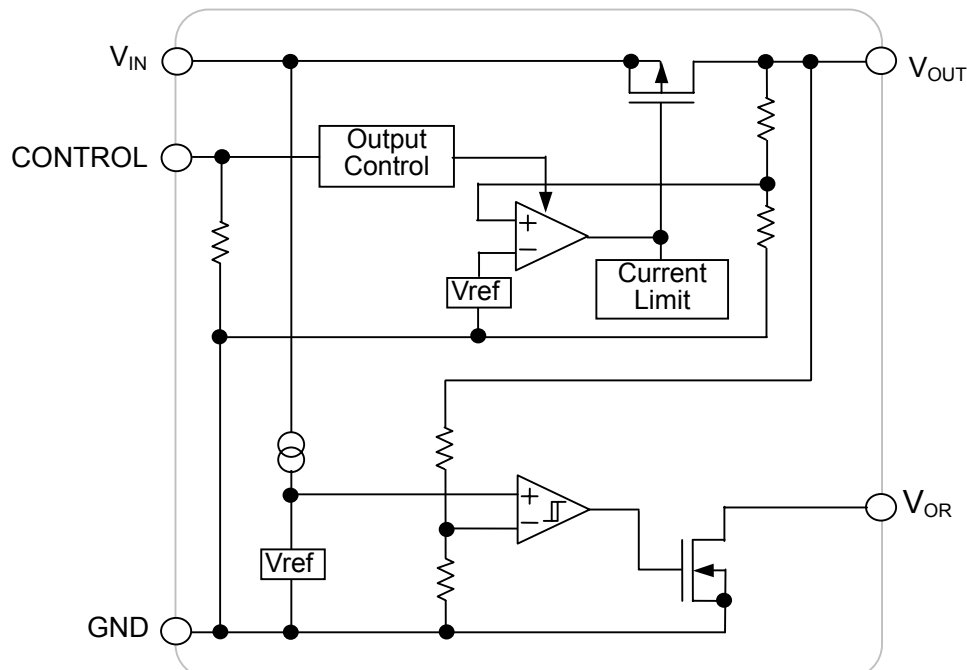
- Ultra Low Quiescent Current  $I_q = 3.0\mu\text{A typ. } (I_o = 0\text{mA})$
- Output Voltage Accuracy  $V_o = \pm 1.0\%$
- Reset Voltage Accuracy  $V_{RT} = \pm 1.0\%$
- Output Voltage Monitor type
- Output Current  $I_o(\text{max.}) = 100\text{mA}$
- Output capacitor with 0.1uF ceramic capacitor
- Nch Open Drain Output
- Internal Short Circuit Current Limit
- CMOS Technology
- Package Outline SOT-23-5

### ■ PIN CONFIGURATION



NJU7271F

### ■ EQUIVALENT CIRCUIT



**■ OUTPUT VOLTAGE/ DETECTION VOLTAGE**

Device Name	Output Voltage	Detection Voltage
NJU7271F1813A	1.8V	1.3V
NJU7271F3328A	3.3V	2.8V
NJU7271F0543A	5.0V	4.3V

Output voltage options available : 1.8 ~ 5.0V (0.1V step)

Detection voltage options available : 1.3 ~ 4.5V (0.1V step)

**■ ABSOLUTE MAXIMUM RATINGS**

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V <sub>IN</sub>	+11	V
Control Voltage	V <sub>CONT</sub>	+11(*1)	V
V <sub>OR</sub> Pin Output Voltage	V <sub>OR</sub>	V <sub>SS</sub> - 0.3 ~ +11	V
V <sub>OR</sub> Pin Output Current	I <sub>OR</sub>	50	mA
Power Dissipation	P <sub>D</sub>	200(*2) 350(*3)	mW
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C

(\*1): Device itself

(\*2): Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

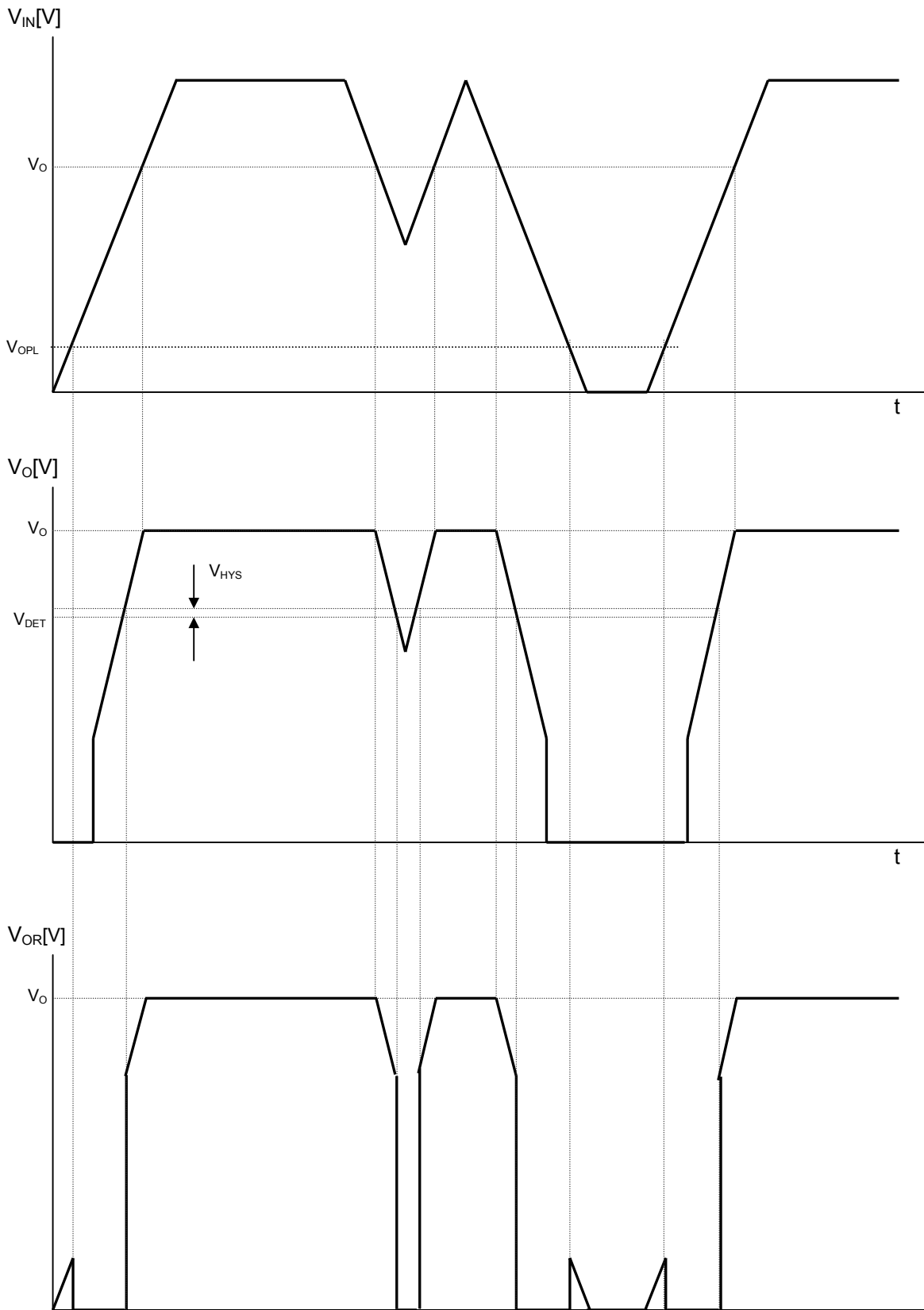
**■ ELECTRICAL CHARACTERISTICS (V<sub>IN</sub>=V<sub>O</sub>+1, C<sub>IN</sub>=0.1μF, C<sub>O</sub>=0.1μF, Ta=25°C)**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
General Characteristics							
Quiescent Current	I <sub>Q</sub>	V <sub>CONT</sub> =V <sub>IN</sub> , I <sub>O</sub> =0mA	-	3.0	7.6	μA	
Quiescent Current at Control OFF	I <sub>Q(OFF)</sub>	V <sub>CONT</sub> =0V, I <sub>O</sub> =0mA	-	0.1	1.0	μA	
Regulator Block							
Output Voltage	V <sub>O</sub>	I <sub>O</sub> =30mA	-1.0%	-	+1.0%	V	
Output Current	I <sub>O</sub>	V <sub>O</sub> - 0.3V	100	-	-	mA	
Line Regulation	ΔV <sub>O</sub> /ΔV <sub>IN</sub>	V <sub>IN</sub> =V <sub>O</sub> +1V ~ V <sub>O</sub> +6V(3.0 > V <sub>O</sub> ) V <sub>IN</sub> =V <sub>O</sub> +1V ~ 9.0V(3.0 ≤ V <sub>O</sub> ) I <sub>O</sub> =30mA	-	-	0.30	%/V	
Load Regulation	ΔV <sub>O</sub> /ΔI <sub>O</sub>	I <sub>O</sub> =0 ~ 100mA	-	-	0.15	%/mA	
Output Voltage Temperature Coefficient	ΔV <sub>O</sub> /ΔTa	Ta=0 ~ 85°C, I <sub>O</sub> =10mA	-	±100	-	ppm/°C	
Control Voltage for ON-State	V <sub>CONT(ON)</sub>		1.6	-	V <sub>IN</sub>	V	
Control Voltage for OFF-State	V <sub>CONT(OFF)</sub>		0	-	0.3	V	
Pull-down Resistance	R <sub>CONT</sub>		2.0	5	10	MΩ	
Short Circuit Limit	I <sub>LIM</sub>	V <sub>O</sub> =0V	-	25	-	mA	
Input Voltage	V <sub>IN</sub>		-	-	9	V	
Dropout Voltage	ΔV <sub>I-O</sub>	I <sub>O</sub> =40mA	1.5V ≤ V <sub>O</sub> ≤ 2.0V	-	0.19	0.60	V
			2.1V ≤ V <sub>O</sub> ≤ 2.4V	-	0.19	0.29	V
			2.5V ≤ V <sub>O</sub> ≤ 2.7V	-	0.18	0.27	V
		I <sub>O</sub> =60mA	2.8V ≤ V <sub>O</sub> ≤ 3.3V	-	0.17	0.26	V
			3.4V ≤ V <sub>O</sub> ≤ 5.0V	-	0.16	0.24	V
			5.1V ≤ V <sub>O</sub> ≤ 6.0V	-	0.15	0.22	V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Reset Block							
Detection Voltage	$V_{DET}$		-1.0%	-	+1.0%	V	
Hysteresis Voltage	$V_{HYS}$		$V_{DET} \times 0.03$	$V_{DET} \times 0.05$	$V_{DET} \times 0.08$	V	
$V_{OR}$ Pin Output Current	$I_{OR}$	Nch, $V_{DS}=0.5V$ $V_{CONT}=0V$	$V_{IN}=1.2V$	0.75	2.0	-	mA
			$V_{IN}=2.4V$ ( $V_{DET} \geq 2.7V$ Version)	4.5	7.0	-	mA
Output Leak Current	$I_{LEAK}$	$V_{IN}=V_{OR}=V_{CONT}=9V$	-	-	0.1	$\mu A$	
Detection Voltage	$\Delta V_{DET}/\Delta Ta$	$Ta=0 \sim 85^{\circ}C$	-	$\pm 100$	-	ppm/ $^{\circ}C$	
Operating Voltage(*4)	$V_{OPL}$	$R_L=100k\Omega$	-	-	0.8	V	

(\*3): The value condition that  $V_{OR}$  become 10% or less of  $V_{IN}$ .

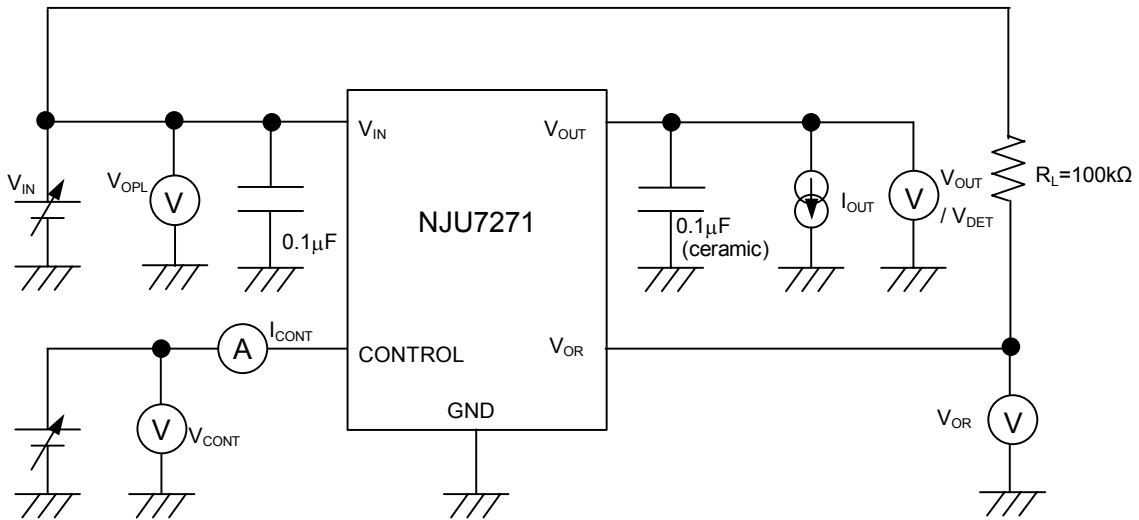
■ TIMING CHART



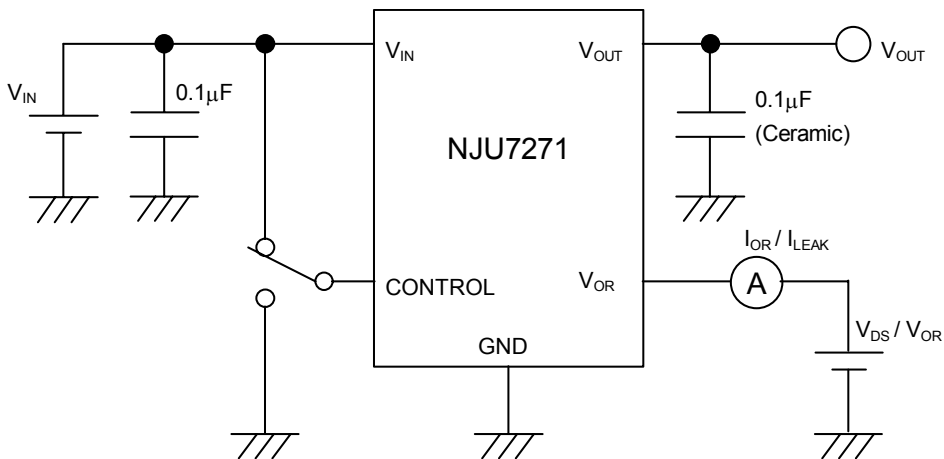
\*  $V_{OR}$  is the case where a pull-up is carried out to  $V_{IN}$  through resistance.

■ TEST CIRCUIT

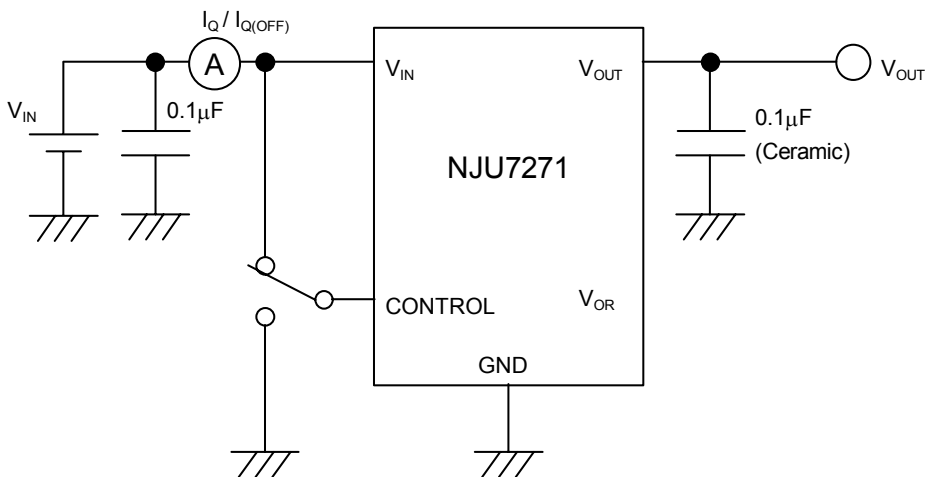
① COMMON TEST CIRCUIT



② OUTPUT CURRENT/OUTPUT LEAK CURRENT TEST CIRCUIT

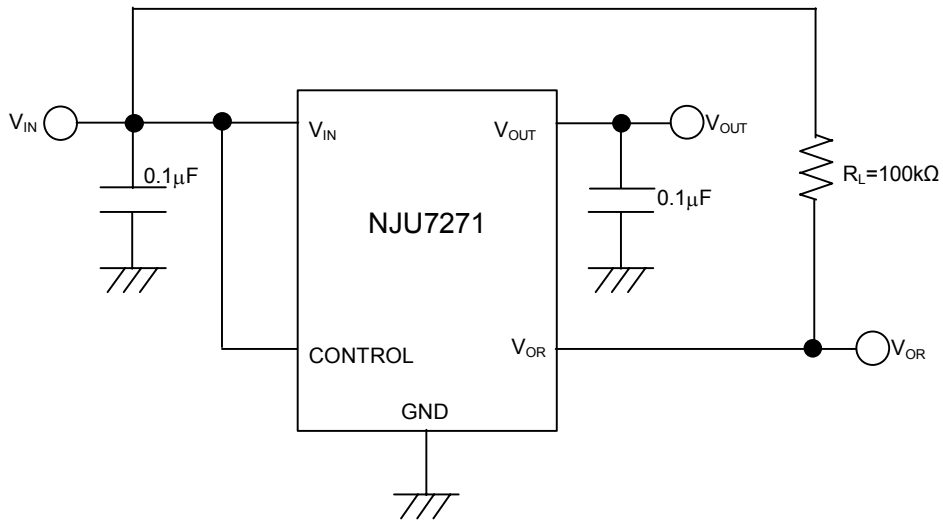


③ QUIESCENT CURRENT TEST CIRCUIT



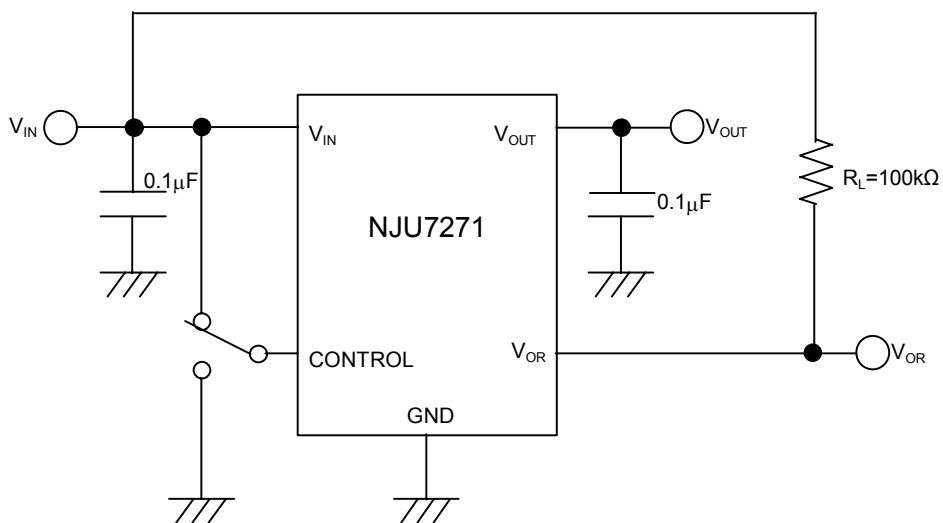
■ TYPICAL APPLICATION

① In case that ON/OFF Control is not required:



Connect control terminal to V<sub>IN</sub> terminal.

② In use of ON/OFF Control:



State of control terminal:

- "H" → output is enabled.
- "L" or "open" → output is disabled.

**\*Input Capacitance  $C_{IN}$**

Input Capacitance  $C_{IN}$  is required to prevent oscillation and reduce power supply ripple for applications with high power supply impedance or a long power supply line.

Use the  $C_{IN}$  value of 0.1  $\mu$ F greater to avoid the problem.

$C_{IN}$  should connect between GND and  $V_{IN}$  as short as possible.

**\*Output Capacitance  $C_o$**

Output capacitor ( $C_o$ ) is required for a phase compensation of the internal error amplifier. The capacitance and the equivalent series resistance (ESR) influence stability of the regulator.

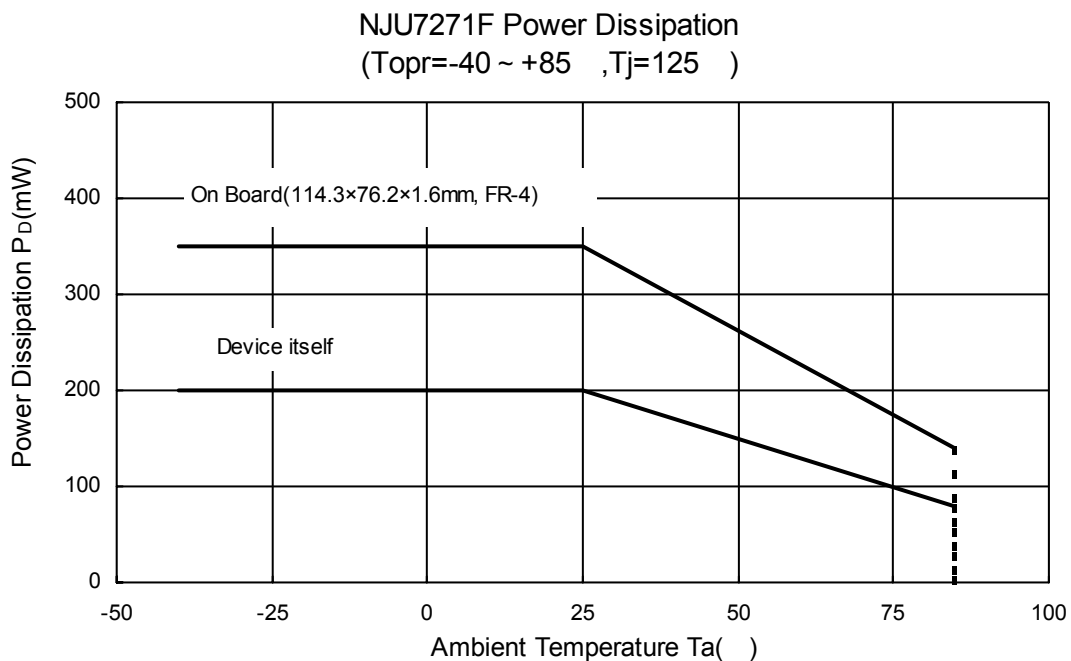
If use a smaller  $C_o$ , it may cause excess output noise or oscillation of the regulator due to lack of the phase compensation. Therefore, use  $C_o$  with the recommended capacitance or greater value and connect between  $V_o$  terminal and GND terminal with minimal wiring.

The recommended capacitance depends on the output voltage. Low voltage regulator requires greater value of the  $C_o$ . Thus, check the recommended capacitance for each output voltage.

Use of a greater  $C_o$  reduces output noise and ripple output, and also improves transient response of the output voltage against rapid load change.

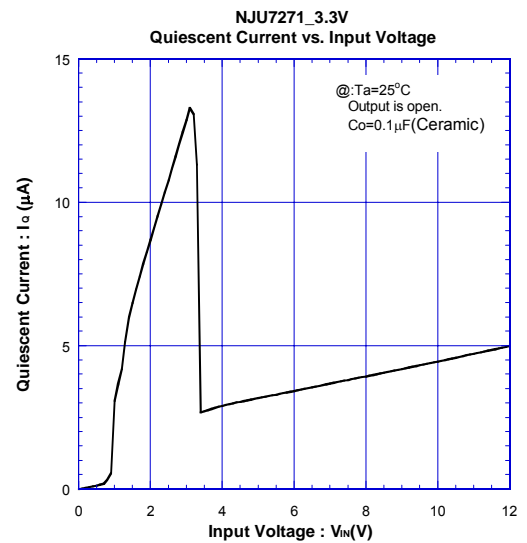
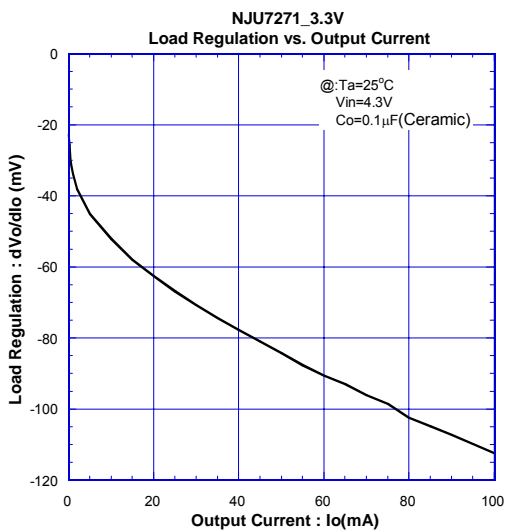
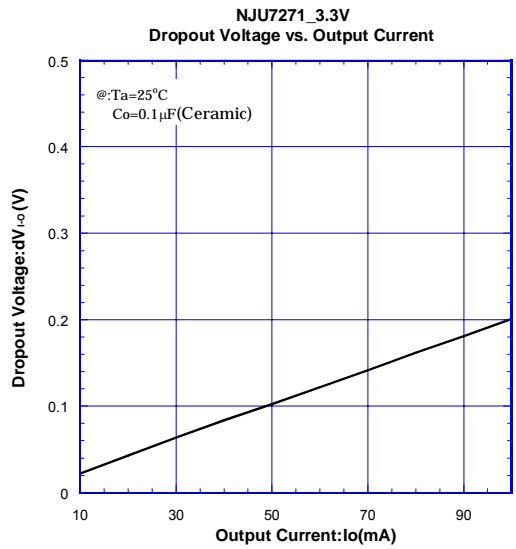
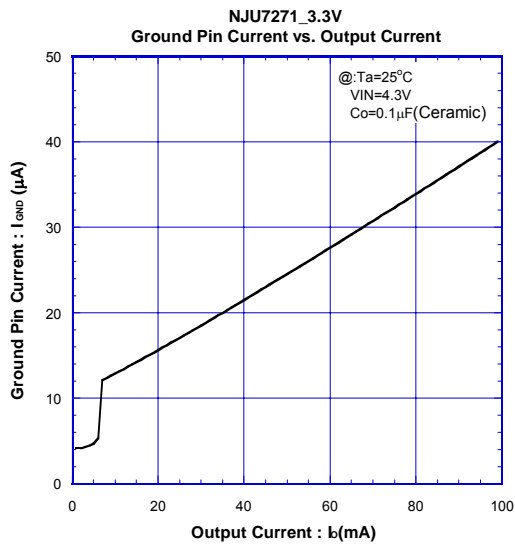
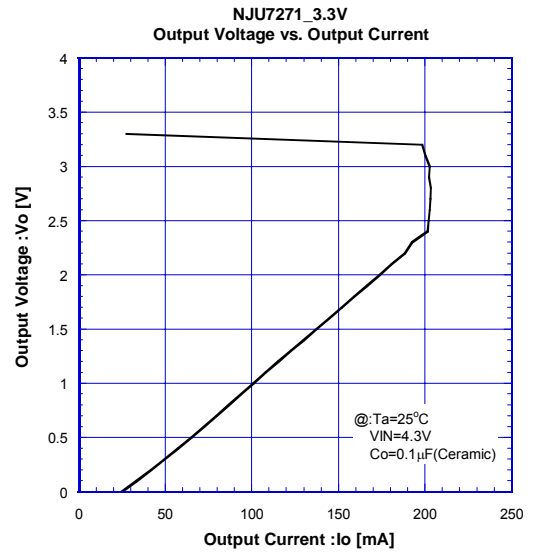
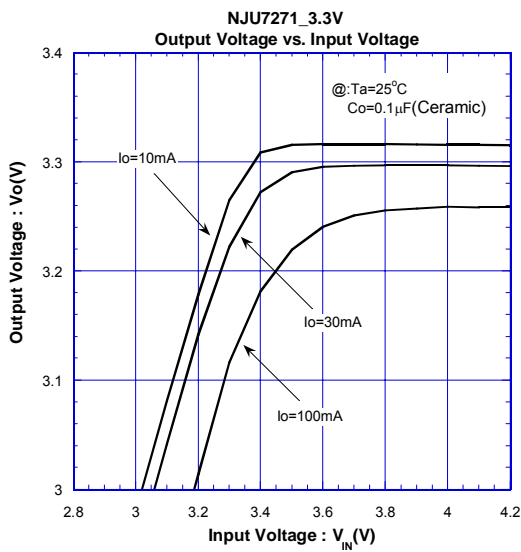
This product is designed to work with any capacitor including a low ESR capacitor for the  $C_o$ ; however, refer "Equivalent Series Resistance vs. Output Current" and choose suitable capacitor.

**POWER DISSIPATION vs. AMBIENT TEMPERATURE**

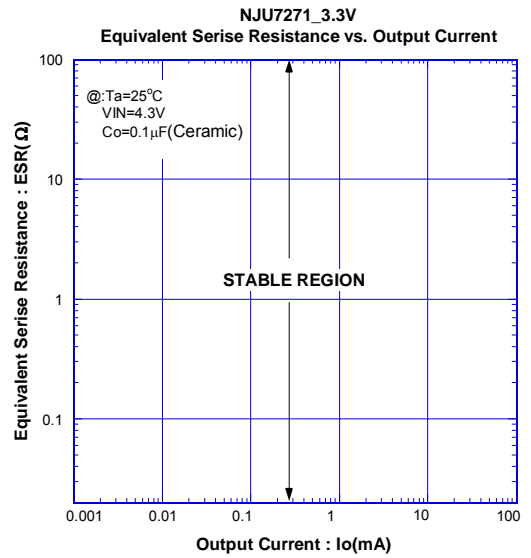
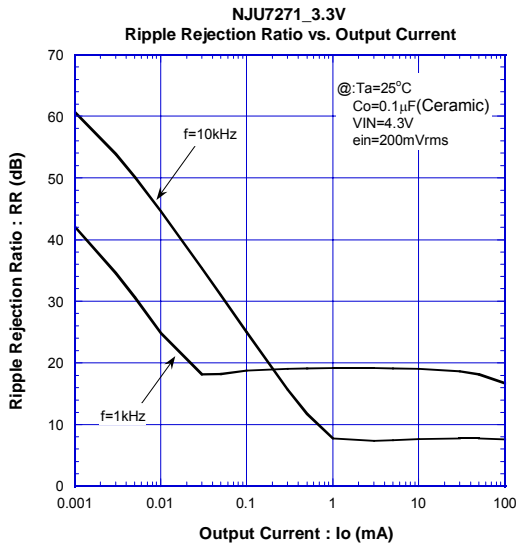
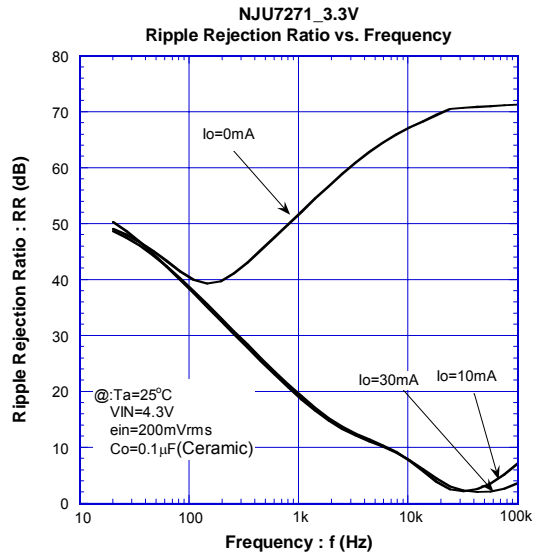
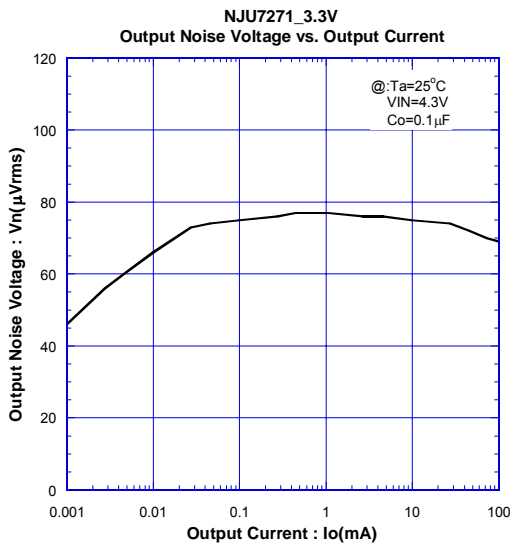




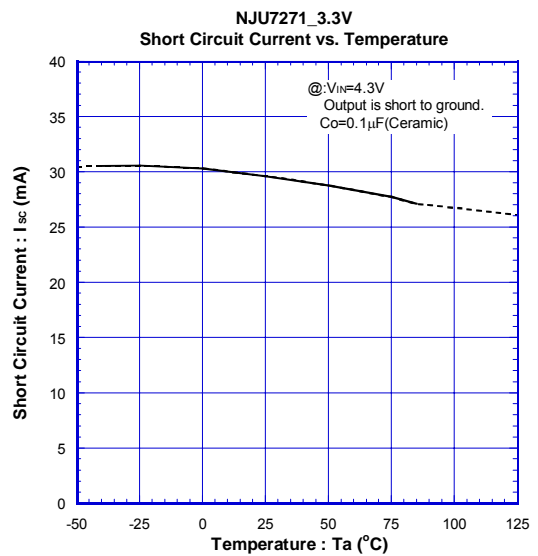
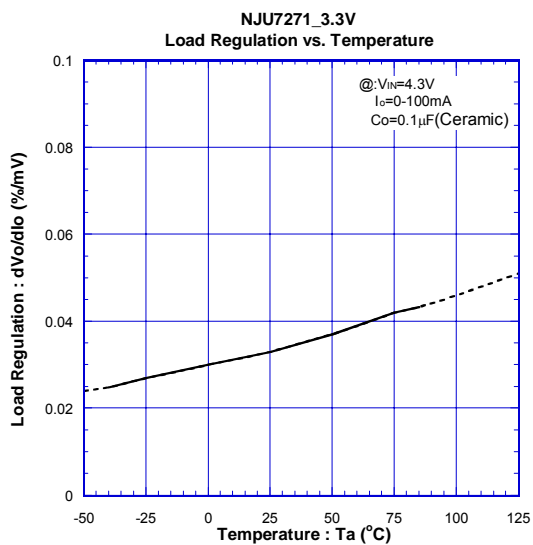
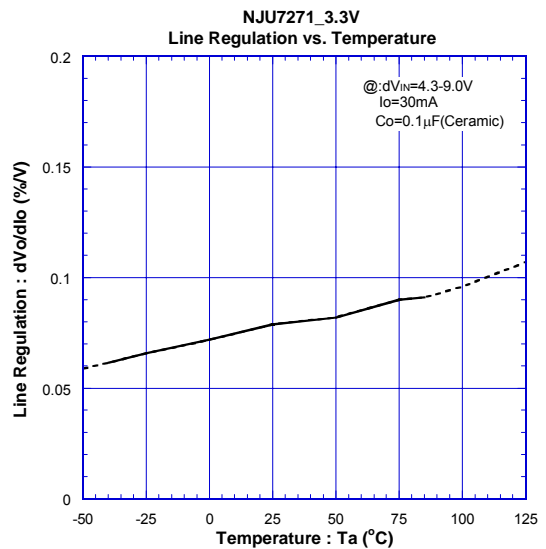
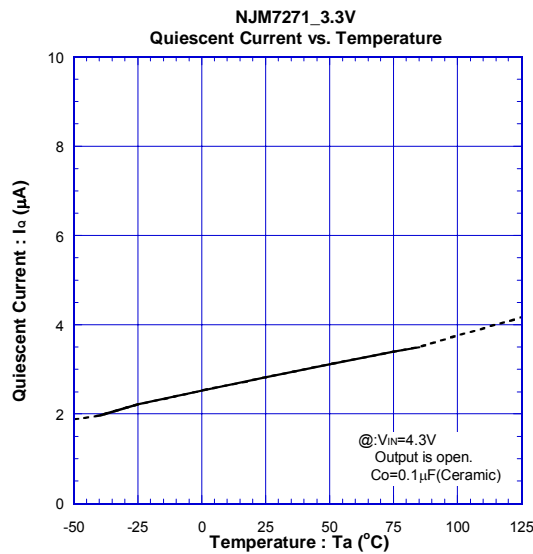
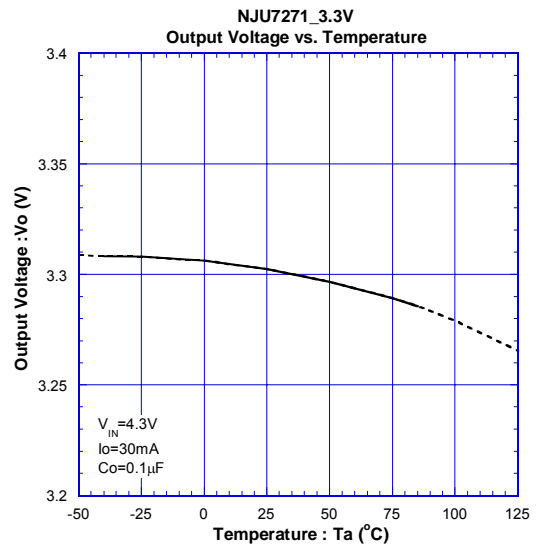
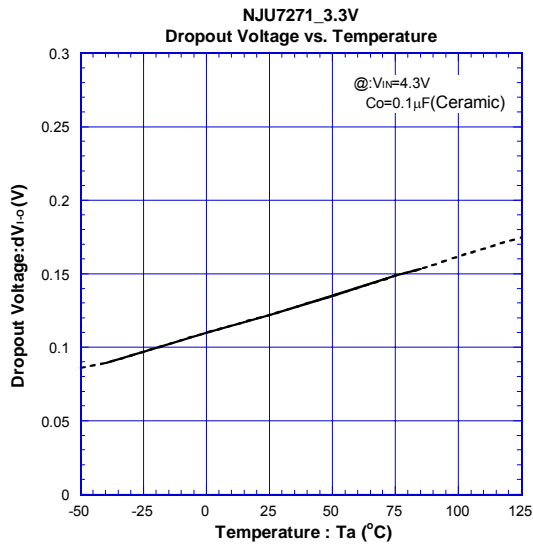
■ TYPICAL CHARACTERISTICS (LDO BLOCK)



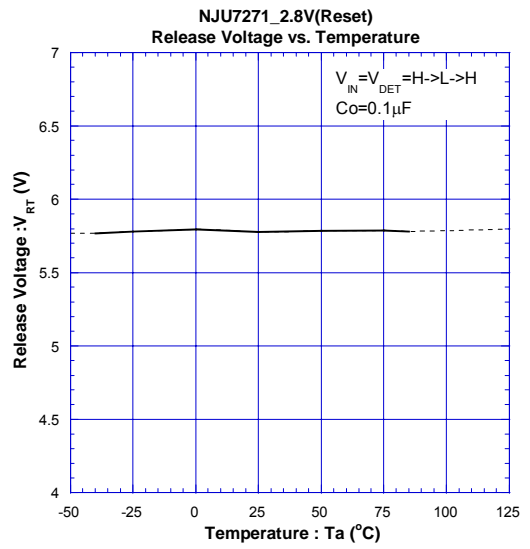
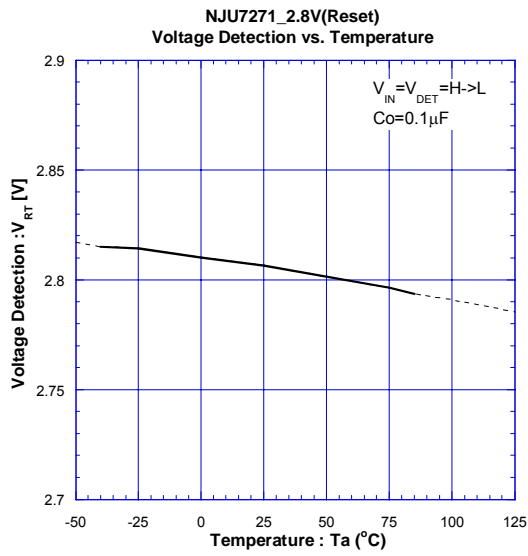
■ TYPICAL CHARACTERISTICS (LDO BLOCK)



## ■ TYPICAL CHARACTERISTICS (LDO BLOCK)



■ TYPICAL CHARACTERISTICS (RESET BLOCK)



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