Analog Signal Input Monaural Class D Power Amplifier

■ GENERAL DESCRIPTION

The **NJU8754** is an Analog signal input monaural class D power amplifier. The IC incorporates the PWM modulator, which converts an analog signal to a 1-bit PWM signal, and the class D operation power MOSFET outputs.

By using external LC low-pass filters, the IC efficiently reproduces audio sound. In addition, the IC features a built-in short-circuit protection for the output, a voltage detector for suppressing pop noise at power-on and a standby function.

■ APPLICATION CIRCUIT

Figure 1 shows the **NJU8754** typical application circuit.

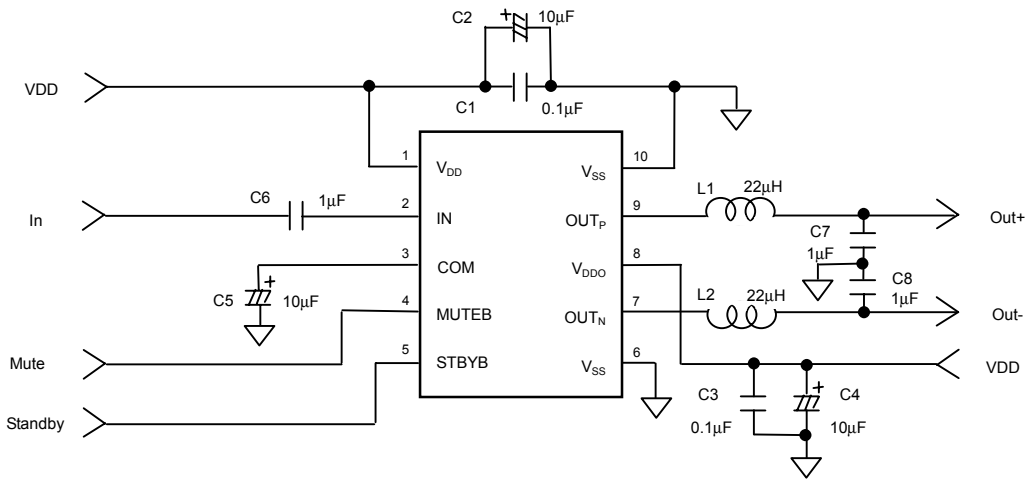

Figure 1 Typical Application

[CAUTION]

The specifications on this application note are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this application note are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

■ MAXIMUM OUTPUT POWER

[BTL Connection]

Figure 2 shows an example of the BTL (bridge-tied-load) connection, where the OUT_P and the OUT_N terminals are connected at both ends of a load.

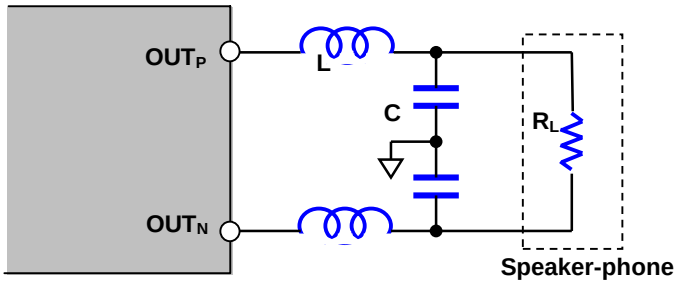

Figure 2 BTL Connection

The maximum output voltage without distortion (V_{RL}[Vrms]), the maximum output current (I_{RL}[Arms]) and the output power (P_O[W]) are calculated with the formula (1) and (2), where R_{DS}[Ω] is the on-resistance of the MOSFET, R_{DC}[Ω] is the DC resistance of the coil and R_L[Ω] is the load impedance.

$$P_O = \frac{V_{RL}^2}{R_L} = I_{RL}^2 \times R_L \quad \cdots (1)$$

$$P_O = \left(\frac{V_{DD} \times \frac{R_L}{2(R_{DS} + R_{DC}) + R_L}}{\sqrt{2}} \right)^2 \div R_L \quad \cdots (2)$$

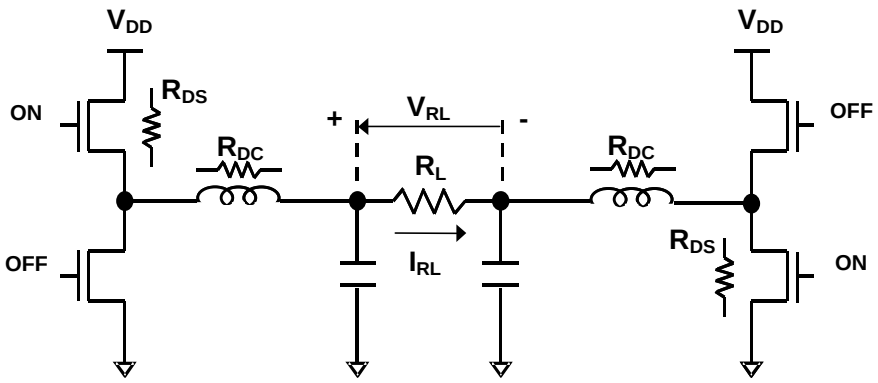

Figure 3 H-bridge Class D Output

For instance, if R_{DS}=0.5[Ω], V_{DD} =5.0[V], R_L=8[Ω] and R_{DC}=0.2[Ω], the maximum output power is calculated as approximately 1.1[W] using the formulas (1) and (2).

■ OUTPUT FILTER

The carrier frequency of the output signal is about 300[kHz]. A secondary or higher LC low-pass filter is required to reject higher-frequency harmonics beyond the audio band. And that filter is composed of a coil (L[H]) and a capacitor (C[F]), which values should be chosen in consideration of a load impedance. The L and C values, shown in Figure 2, are given by the formulas (3) and (4), where the frequency in between 25kHz and 50kHz is used as the cutoff frequency (F_{CL}[Hz]) and the value 1/√2 as the quality factor (Q).

For example, if F_{CL}=30[kHz], C=1.0[μF] and L=22[μH] are the best choices at R_L=8[Ω], and C=2.2[μF] and L=15[μH] at R_L=4[Ω].

NOTE1) Both DC resistance of a coil and series-equivalent resistance of a capacitor may reduce output efficiency. Therefore, the components should be low resistance.

NOTE2) Be aware that the cutoff frequency and the quality factor impact on sound quality. And also, the higher the quality factor, the more the operating current at around the cutoff frequency becomes. Therefore, the quality factor by the C and the L should be designed for Q≤1.

$$C = \frac{Q}{\pi \cdot F_{CL} \cdot R_L} \quad \cdots(3) \qquad L = \frac{R_L}{4\pi \cdot F_{CL} \cdot Q} \quad \cdots(4)$$

■ VOLTAGE GAIN

The voltage gain of the IC itself is about 14x (A_V) due to the built-in inverting operational amplifier with 7x gain and the BTL connection with 2x gain. Although the original gain of IC is fixed by the internal input resistors R_I[Ω] and the feedback resistor R_F[Ω], the voltage gain can be adjusted by the external gain-adjustment resistor r[Ω] as shown in Figure 4.

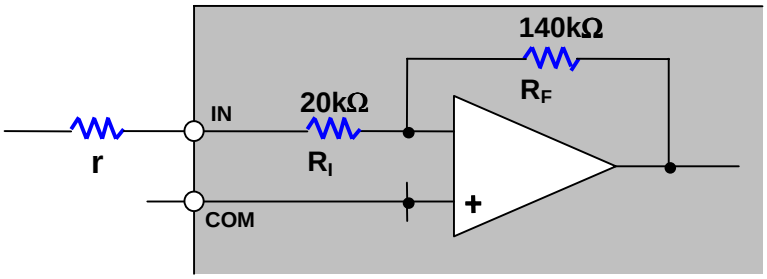

Figure 4 Adjustment of Voltage Gain

The A_V is calculated with the formula (5).

$$A_V = \frac{140k\Omega}{20k\Omega + r} \times 2 \quad \cdots(5)$$

NOTE) It is recommended to choose the external resistor (r) to achieve the maximum output voltage at the maximum input voltage.

■ INPUT FILTER

A primary RC high-pass filter is applied to the input. And its cutoff frequency (F_{CH}[Hz]) is calculated with the formula (6), where R_I[Ω] is the built-in input resistor, r[Ω] is the external gain-adjustment resistor and C_C[F] is the AC coupling capacitor. For example, if C_C=1[F] and r=0[Ω] (no resistor), F_{CH}=8[Hz] is given.

NOTE1) The cutoff frequency is adjusted by the gain-adjustment resistor.
NOTE2) The D/A converter with a post filter may occur some aliasing noise. In this case, a pre-filter (RC low-pass filter) would work in reducing the noise.

$$F_{CH} = \frac{1}{2\pi \cdot (R_I + r) \cdot C_C} \quad \cdots(6)$$

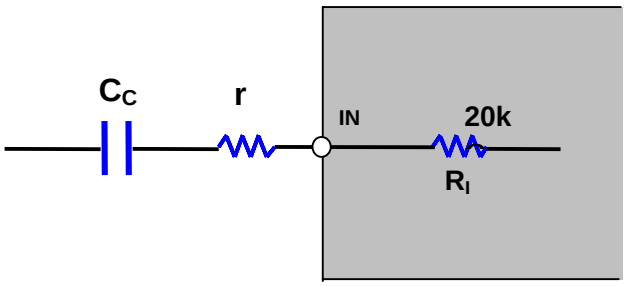

Figure 5 Input Filter

■ STANDBY / MUTE CONTROL

By setting the STBY terminal to “L”, the IC is completely halted. In this state, the outputs such as the OUT_P and OUT_N are in high impedance and an operating current is reduced down to less than 1[uA].

By setting the MUTE terminal to “L” at STBY=”H”, the outputs generate the audio-mute (no-sound) signal with 50% duty independently of the audio input signal.

By setting the STBY terminal to “H”, the AC coupling capacitors are charged up to the voltage level of COM terminal such as 1/2×V_{DD}. And this charge should be executed at MUTE=”L”. If the MUTE terminal goes to “H” while charging the capacitors, the noise is reproduced by the charge. The charging time depends on the value of the coupling capacitor, and as a guideline, it is about 100[ms] at least in use of 2.2[μF] coupling capacitor.

In addition, the power-off with the standby off may cause noise by the discharge of the coupling capacitor. For this reason, the power-off should be performed after the standby on.

NOTE1) The standby function has a priority over the mute function. When the standby or the mute is not used, the unused terminal should be fixed at “H”.
NOTE2) The transition time of the standby control signal and the mute must be less than 100[μs].

■ POWER CONSUMPTION

The power consumption (P_D[W]) of the IC itself is calculated with the formula (7), where P_O[W] is the output power, R_O[Ω] is the on-resistance of the power MOSFET (R_{DS} x2 in using the BTL connection), R_L[Ω] is the load impedance and P_{DIC}[W] is the power dissipation inside the IC.

$$P_D = P_O \times \frac{R_O}{R_L} + P_{DIC} \quad \cdots(7)$$

For example, if R_L=8[Ω] and P_O=1[W], the power consumption (P_D[W]) is calculated as 153[mW], as follows.

$$1W \times \frac{1.0\Omega}{8\Omega} + 28mW = 153mW \quad \cdots(8)$$

CONDITION)

The power supply voltage for the outputs is 5[V]. The LC filter is configured as 22[μH] coil (A918CY-220M manufactured by TOKO, INC.) and 1[μF] capacitor (GRM31MB11E105KC12B manufactured by Murata Manufacturing Co.). On this condition, P_{DIC} is measured as about 28[mW] at no sound reproduction.

The power efficiency η[%] is calculated with the formula (9), where P_D[W] is the power consumption of the IC itself, P_C[W] is the power consumption of the coil and P_O[W] is the output power. Then, 83% is given on condition just described. Figure 6 shows the typical characteristic of “Power Efficiency vs. Output Power”.

$$\eta = \frac{P_O}{P_O + P_D + P_C} \times 100 \quad \cdots(9)$$

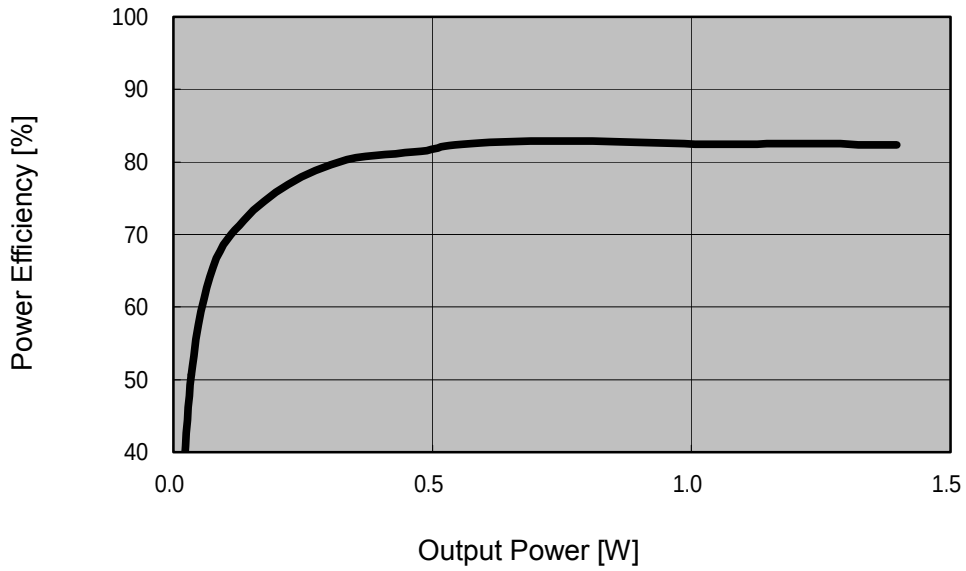

Figure 6 Power Efficiency vs. Output Power

■ POWER DISSIPATION

The class D amplifiers achieve higher efficiency and dissipate the power less than general analog amplifiers. However, if the IC is continuously generating the maximum output power, the power dissipation may theoretically exceed the absolute maximum rating because the package SSOP10 is very small. In this regards, the effective output-power of typical sound is in the range of 1/5 and 1/10 of the maximum and the PCB works as a heatsink, so it may never exceed the absolute maximum rating in actual application. Just to be safe, it is recommended that it not exceed the maximum rating in consideration of the heatsink, ambient temperature, output power, etc.

The maximum power dissipation of this package (P_{dMAX}[W]) is calculated with the formula (10), where P_{dMAX}[W] is the maximum power dissipation, T_{jMAX}[°C] is the junction temperature, Ta[°C] is the ambient temperature and θja[°C/W] is the thermal resistance of the package. For instance, if T_{jMAX}=125[°C], θja=400[°C/W] and Ta=25[°C], the maximum power dissipation is calculated as approximately 250[mW].

$$P_{dMAX} = \frac{T_{jMAX} - T_a}{\theta_{ja}} \qquad \cdots(10)$$

Figure 7 shows the power dissipation on condition that the IC is mounted on a two- or four-layer PCB (EIA/JEDEC STD) or the IC itself.

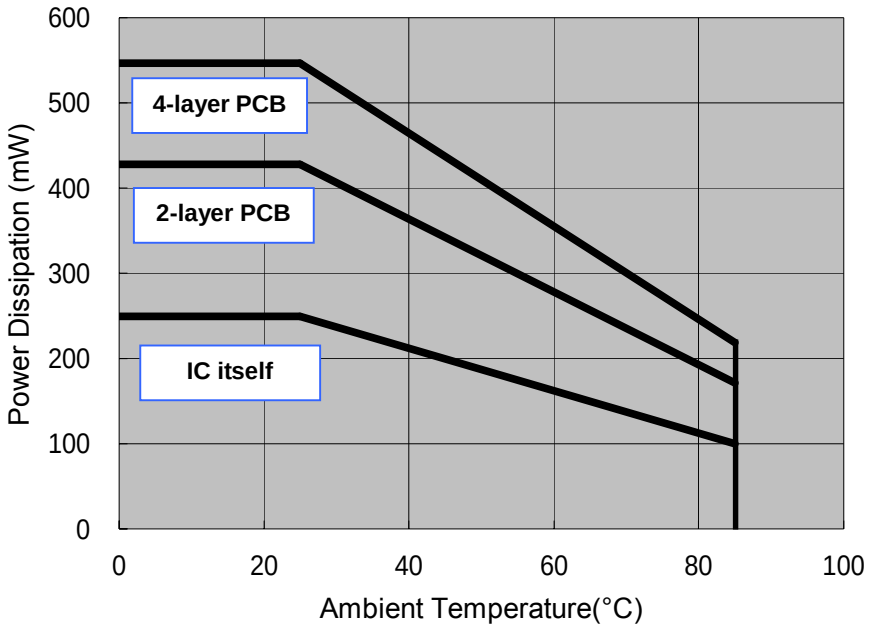

Figure 7 Power Dissipation of SSOP10

■ POWER SUPPLY

The power supply for the outputs is required to provide the enough power and stable operation for not only audio reproduction given with formula (1) but also Source/Sink current of output power MOSFET's switching. And the decoupling capacitors between V_{DD}-V_{SS}, V_{DDO}-V_{SS} would help suppressing ripples on the power supply lines. Make sure what the best capacitor size is in the user's particular application. In addition, because a parasitic inductance may deteriorate the frequency response of the decoupling capacitors, high-frequency capacitors should be placed as close as possible to the terminals of IC, and wide and short track layout should be applied.

■ LAYOUT

Figure 8 shows the typical PCB layout, where external components are mounted on the surface of the PCB and the power supply lines and GND plane are laid out on its backside.

The **NJU8754** operates under the single power supply voltage. The V_{DD} and V_{DDO} lines should be connected together as close as possible to the IC. And the layout of the LC filter and the power supply circuit for the outputs should be symmetric so that the OUT_P and OUT_N audio outputs have the same performance.

The EMI noise depends on the area and length of current loop formed by layout of high-frequency components and path on PCB. Thus, place the external components as the current loop formed by the output power supply terminals and the decoupling capacitors and the loop by the output terminals and the LC filters should be the narrowest. And a wide and short track would work in reducing the EMI noise.

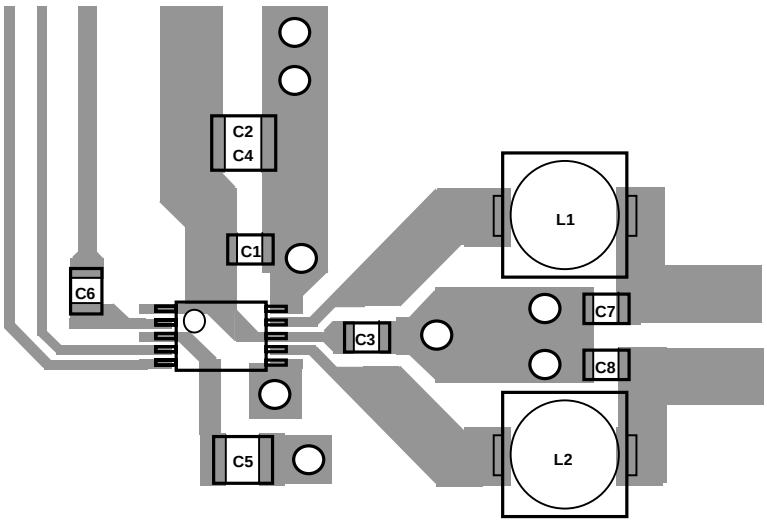

Figure 8 PCB Layout Example (Surface)