NJU26203A Application Note

Hardware Manual

New Japan Radio Co., Ltd

Version 1.01

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CAUTION

The products specifications and descriptions listed in this application note are subject to change at anytime without notice.

The specifications on this application note are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this application note are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

NJU26203A Application Note
Hardware Manual

1. General Description

This application note describes the NJU26203A hardware applications and usages. The main items described in this document are the next four application circuits, Master/Slave mode, MCK clock, crystal oscillation circuit, reset circuit and the suggestions on the design of the NJU26203A and so on.

1) The NJU26203A application circuit with DIR and DAC (I^2C Bus)
2) The NJU26203A application circuit with ADC and DAC (I^2C Bus)
3) The NJU26203A application circuit with DIR, ADC and DAC (I^2C Bus)
4) The NJU26203A application circuit with DIR, ADC and DAC (4-wire Serial Bus)

2. NJU26203A Block Diagram

The Figure 1 shows the NJU26203A block diagram.

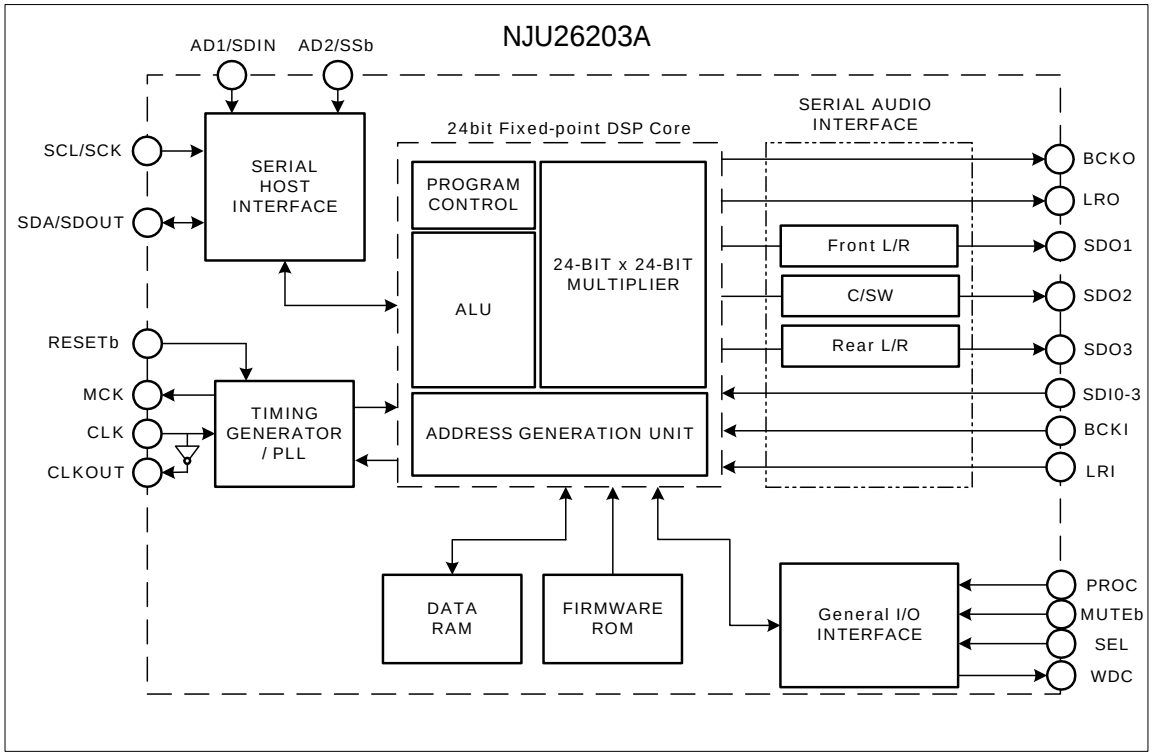

Figure 1. NJU26203A Block Diagram

Note1: The NJU26203A provides four digital audio inputs and four digital audio outputs. The application circuits do not use all inputs. The input and output circuits should be modified according to the target application.

Note2: Refer to the NJU26200 Series Hardware Specification, the NJU26203A Data Sheet and the NJU26203A Software Manual together with this application note.

3. Application Circuit Examples

The next four application circuits are described in this section.

1) The NJU26203A application circuit with DIR and DAC (I^2C Bus)
2) The NJU26203A application circuit with ADC and DAC (I^2C Bus)
3) The NJU26203A application circuit with DIR, ADC and DAC (I^2C Bus)
4) The NJU26203A application circuit with DIR, ADC and DAC (4-wire Serial Bus)

Note1: DIR: Digital Interface Receiver
ADC: Analog to Digital Converter DAC: Digital to Analog Converter
Note2: DSP denotes the NJU26203A in this document.
Note3: The ADCs and DACs operate in Slave mode in the Figure 3 to Figure 6.
Note4: The DSP command selects Master/Slave mode.
Note5: The settings of the master volume and the command operation mode after reset is described in Table1. These settings can be selected by PROC and MUTEb terminals (Table 1).
The PROC and MUTEb terminals should be connected to VDDIO or VSSIO through the resistor.
The recommended resistor value is 3.3kΩ.

Terminal	Symbol	Value	DSP Status After Reset
11	MUTEb	"High"	Master volume is 0dB.
		"Low"	Master volume is mute.
13	PROC	"High"	The DSP is operating with the default settings and ready for any commands.
		"Low"	The DSP is not operating and wait for the start command. Sending the start command is required to start the operation.

Table1. The settings of Master volume and Command operation after reset

In the application circuits of this document, the MUTEb and PROC terminals are set to "High". After reset, the DSP sets master volume 0dB and is ready for any commands.

3.1 Application circuit 1 "The NJU26203A application circuit with DIR and DAC (I^2C Bus)"

This application circuit 1 employs the digital audio signal input, for example DIR input.
The Figure 3 shows the circuit with DIR, DSP and DAC. The DSP operates in the Slave mode.
The DIR supplies DAC with MCK clock.

3.2 Application circuit 2 "The NJU26203A application circuit with ADC and DAC (I^2C Bus)"

This application circuit 2 employs the analog audio signal input, for example ADC input.
The Figure 4 shows the circuit with ADC, DSP and DAC. The DSP operates in the Master mode.
The DSP supplies ADC and DAC with MCK clock.

3.3 Application circuit 3 "The NJU26203A application circuit with DIR, ADC and DAC (I^2C Bus)"

This application circuit 3 employs the analog audio signal input, for example ADC input, and digital audio signal input, for example DIR input.
The Figure 5 shows the circuit with DIR, ADC, DSP and DAC. The DSP should be set in Master mode in case of analog input. The DSP should be set in Slave mode in case of digital input.
The DSP supplies ADC and DAC with MCK clock in case of analog input. The DIR supplies ADC and DAC with MCK clock in case of digital input.

Note1: In case of digital audio input, DIR, DSP and DAC process the input signal. The DSP is set in Slave mode. The DIR supplies DAC with MCK clock. The S1 switch should be selected for DIR mode.

Note2: In case of analog audio input, ADC, DSP and DAC process the input signal. The DSP is set in Master mode. The DSP supplies ADC and DAC with MCK clock. The S1 switch should be selected for DSP mode.

3.4 Application circuit 4 "The NJU26203A application circuit with DIR, ADC and DAC (4-wire Serial Bus)"

This application circuit 4 is the example circuit to control the DSP by the 4-wire serial bus.
The Figure 6 shows the circuit with DIR, ADC, DSP and DAC.
The difference between the application circuit 3 and this application is just using the I^2C Bus or the 4-wire serial bus.

4. Master/Slave Mode

The definition and the usage of Master/Slave mode are described in this section.

4.1 Master/Slave Mode Definition

The definition of Master mode DSP is as follows. The Master mode DSP supplies peripheral ICs with MCK, LRCK and BCK clock. The peripheral ICs process the signal synchronizing with the MCK, LRCK and BCK clock. In the above state, the DSP operates as Master mode.

The definition of Slave mode DSP is as follows. The Slave mode DSP receives LRCK and BCK clock from the *external peripheral ICs. The DSP processes the signal synchronizing with the external LRCK and BCK clock. In the above state, the DSP operates as Slave mode.
Note: External peripheral ICs denotes DIR or ADC with Master mode.

4.2 DSP MCK Clock

The usages of MCK clock in Mater/Slave mode are described in this section.
After the power-on initialization, the MCK terminal outputs the MCK clock that comes from the CLK terminal in Slave and Master mode. The frequency inputted to CLK should be 12.288MHz according to the specification. Therefore the MCK terminal generates the 12.288MHz clock.

4.3 Master/Slave Mode usages

The usages of Master/Slave Mode are described in this section.

1) In case of digital audio input, the DSP should operate in Slave mode. The DIR should supply DAC with MCK clock. Refer to the application circuit 1.
2) In case of analog audio input, the DSP should operate in Master mode. The DSP should supply ADC and DAC with MCK clock. Refer to the application circuit 2.

5. DIR MCK Clock

The MCK clock generation of DIR is described in this section.
The DIR extracts MCK clock from digital audio signal and supplies DAC or others with it. In case that the DIR cannot extract MCK clock, ADC or others are supplied with MCK clock by the next methods.

DIR MCK clock generation

1) In case of no digital audio signal, DIR generates MCK, LRCK and BCK clock by the internal oscillator. In this document, the example circuits adopt this kind of DIR.
2) In case of no digital audio signal, DIR generates MCK, LRCK and BCK clock by the DIR crystal oscillator.
3) In case of no digital audio signal, DIR buffers the externally generated MCK clock and outputs it to the next ICs.

Note: In case that DIR is adopted, the DSP should operate in Slave mode. DAC or others are supplied with the DIR MCK clock. Under this condition, the DSP system can process the digital audio signal correctly.

6. ADC/DAC MCK Clock

The set-up of ADC, DAC and Codec are described in this section.

In case of analog audio input, ADC, DAC and Codec should operate in Slave mode. The DSP should operate in Master mode. The DSP supplies ADC and DAC with MCK clock.

In case of using ADC with crystal oscillator or Codec with DIR, the DSP can operate in Slave mode. And ADC or Codec should operate in Master mode.

7. Crystal Oscillation Circuit

The Figure2 shows crystal oscillation circuit. The NJU26203A employs the PLL circuit inside that is tailored to the frequency of 12.288MHz.

The oscillation margin, frequency and application circuit depend on the crystal unit. The detail information of the crystal oscillation circuit should be asked to the crystal maker.

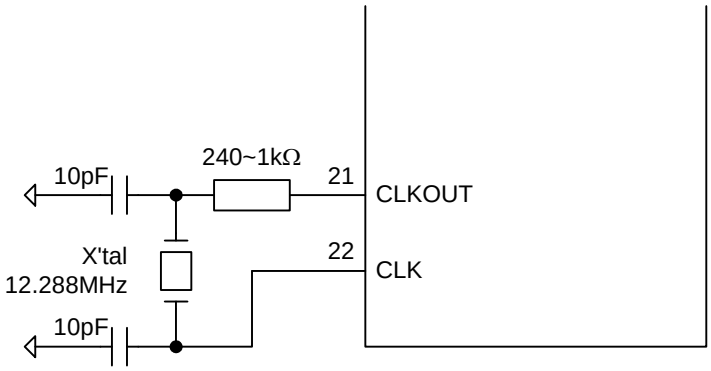

Figure 2. Crystal Oscillation Circuit

8. Reset

Suggestions to design the reset circuit are described in this section.

Suggestions to design reset circuit

1) Reset line should be connected shortly to protect it from the external noise. The next countermeasures are also effective.
   - Do not layout the parts and lines that generate noise near the reset line.
   - Guard reset line by ground line.
   - Current loop space should be minimized as small as possible.

2) In case of long reset line, the next countermeasures are effective.
   - Insert a several-tens-ohm resister in reset line serially.
   - Insert a several-kilos-ohm pull-up resister between the reset terminal and power supply.
   - Insert a 10pF up to 100pF capacitor between the reset terminal and ground.

9. Suggestions to design DSP circuit

Suggestions to design the DSP circuit are described in this section.

1) The DSP employs three kinds of power supplies, core (V_{DD}), PLL (V_{DDPLL}), and IO (V_{DDIO}). The V_{DD} and V_{DDPLL} are 1.8V. The V_{DDIO} is 3.3V. The input terminals accept 5V signal. The Figure 3 to Figure 6 circuits assumes that the peripheral ICs employ 3.3V power supply. Then the DSP can connect to the peripheral ICs directly.

   The DSP employs the two-level power supplies. So the next procedure is recommended to power on. First, power on 3.3V. And then, power on 1.8V.

2) The DSP and other ICs require 0.1uF capacitors, for example ceramic capacitor, between the power supply terminals and ground as bypass capacitors. Also the around 10uF capacitor is required between the DSP power supply and ground.

3) The analog ground and digital ground should be separated to prevent analog signal from digital noise. The analog ground and digital ground should be connected at the adequate point. And the common ground should be connected to frame ground or something.

4) The long digital signal line emits noise and also receives the influence of noise. So MCK, BCKO, LRO, DATA, RESET line should be guarded by ground line to reduce noise problem. The digital signal line should be short and wide to prevent it from noise.

5) The quantity of EMI noise depends on the current loop space of digital signal. So the digital signal line should be short, wide and also guarded by ground.

6) The EMI noise is generated by digital signal in most cases. To reduce the EMI noise, insert a several-tens-ohm dumping-resister at an output terminal serially. But the dumping-resister sometimes affects the output level. So check the specification of the next IC, before inserting it.

Notice: The effects of countermeasures in this document depend on the Implementation of the PCB board.

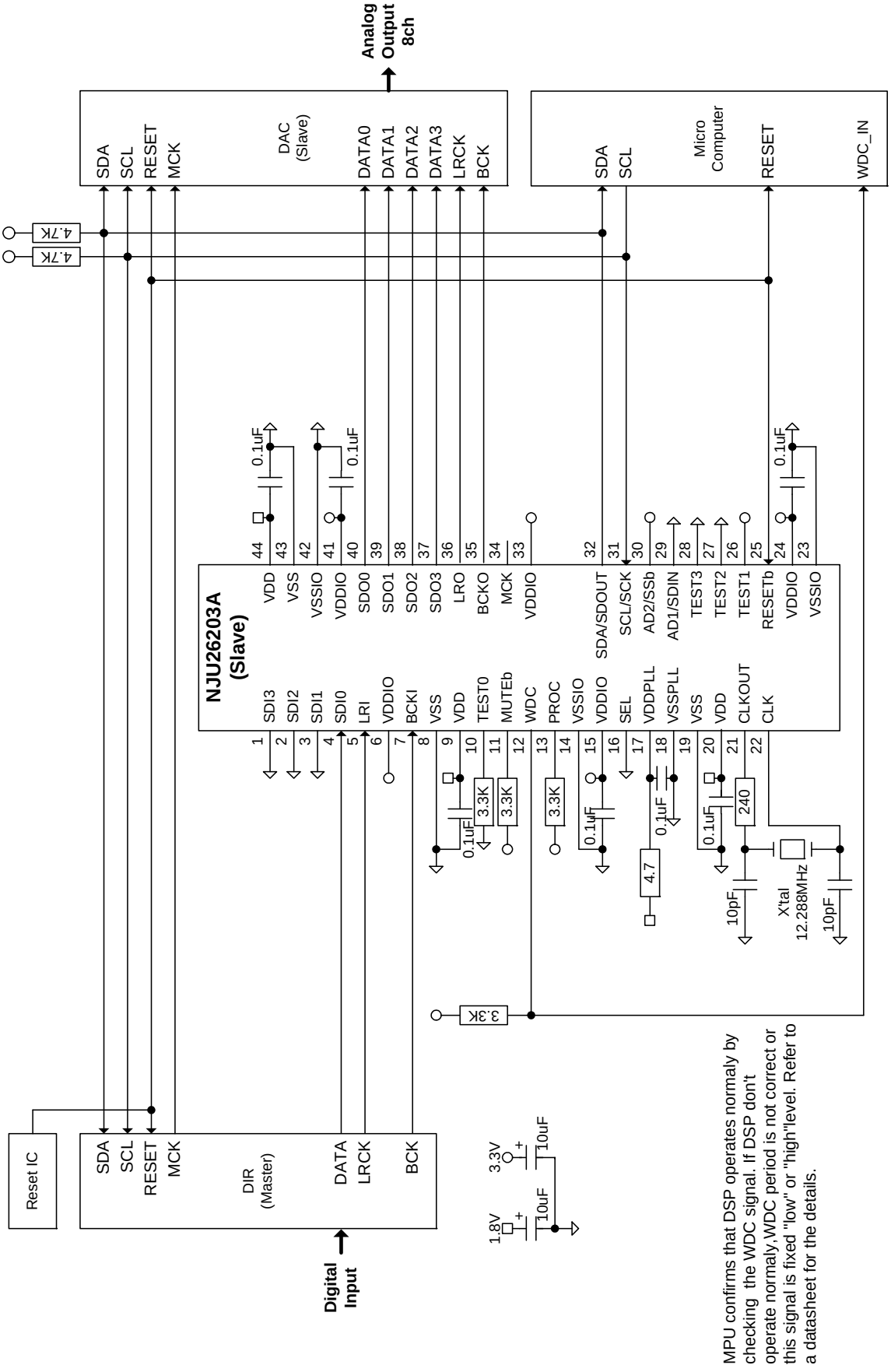

Figure 3. Application circuit 1: NJU26203A with DIR and DAC (I^2C Bus)

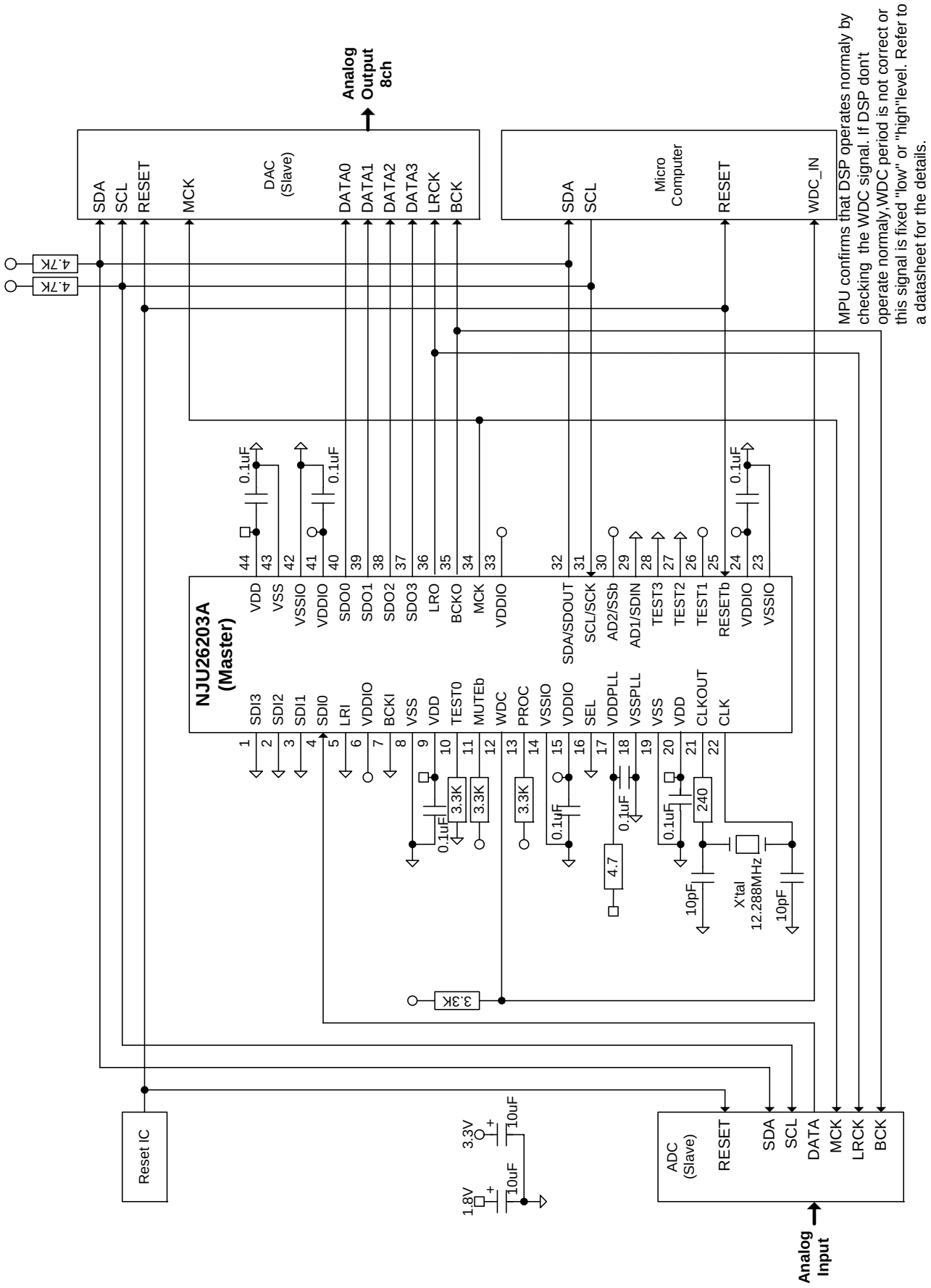

Figure 4. Application circuit 2: NJU26203A with ADC and DAC (I^2C Bus)

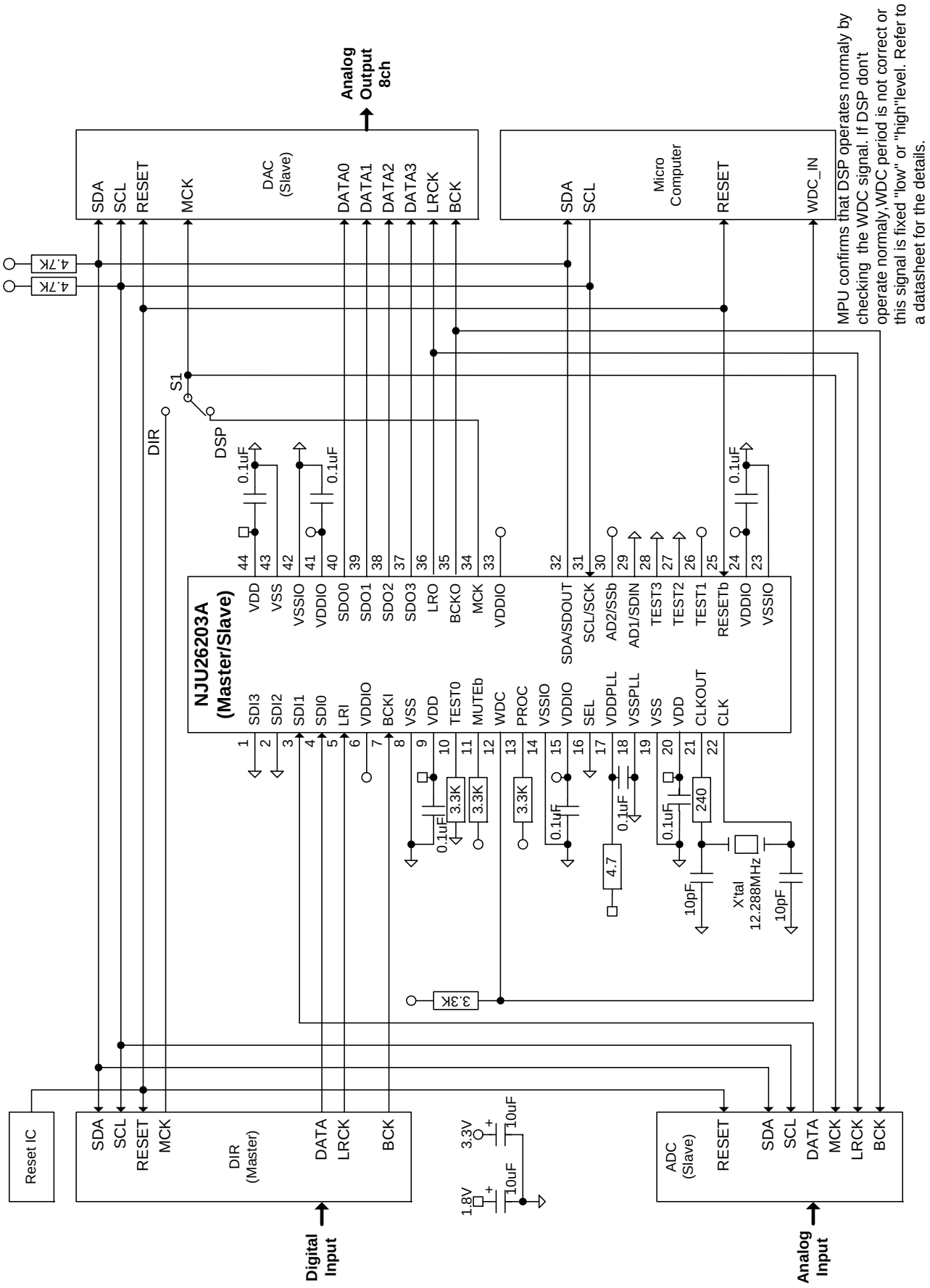

Figure 5. Application circuit 3: NJU26203A with DIR, ADC and DAC (I^2C Bus)

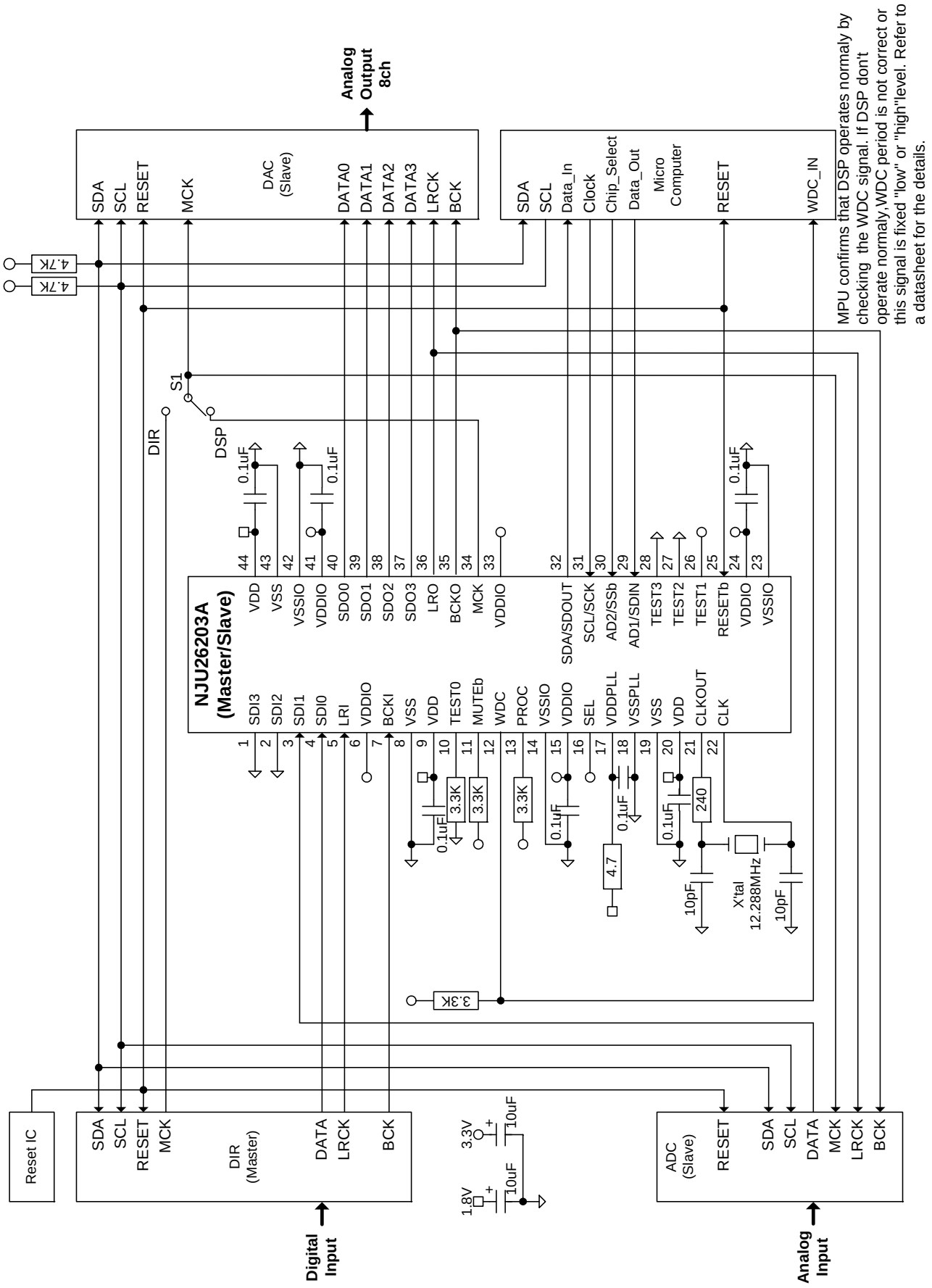

Figure 6. Application circuit 4: NJU26203A with DIR, ADC and DAC (4-wire Serial Bus)