NJU26200 Series Hardware Specification

■ General Description

This document describes the NJU26200 Series common hardware specifications. This document is applied to the NJU26201 up to the NJU26249. The individual function is described in the each data sheet. Please refer to the each data sheet to find the detail functions. The firmware commands are described in the each firmware document.

■Package

■ Hardware Specification

NJU26200FR3 **NJU26200V**

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz (Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 4 Output ports
- Digital Audio Format : I^2S 24bit, Left- justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode
  - In Master mode, MCK : 128fs @fs=96kHz / 192fs @fs=64kHz / 256fs @fs=48kHz / 384fs @fs=32kHz
- Host Interface
  - I^2C Bus (Fast-mode/400kbps)
  - 4-Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Power Supply : $V_{DD} = V_{DDPLL}$ =1.8V, V_{DDIO} = 3.3V
- Input terminal : 5V Input tolerant
- Package : LQFP48-R3 (Pb-Free), SSOP44 (Pb-Free)

■ Block Diagram

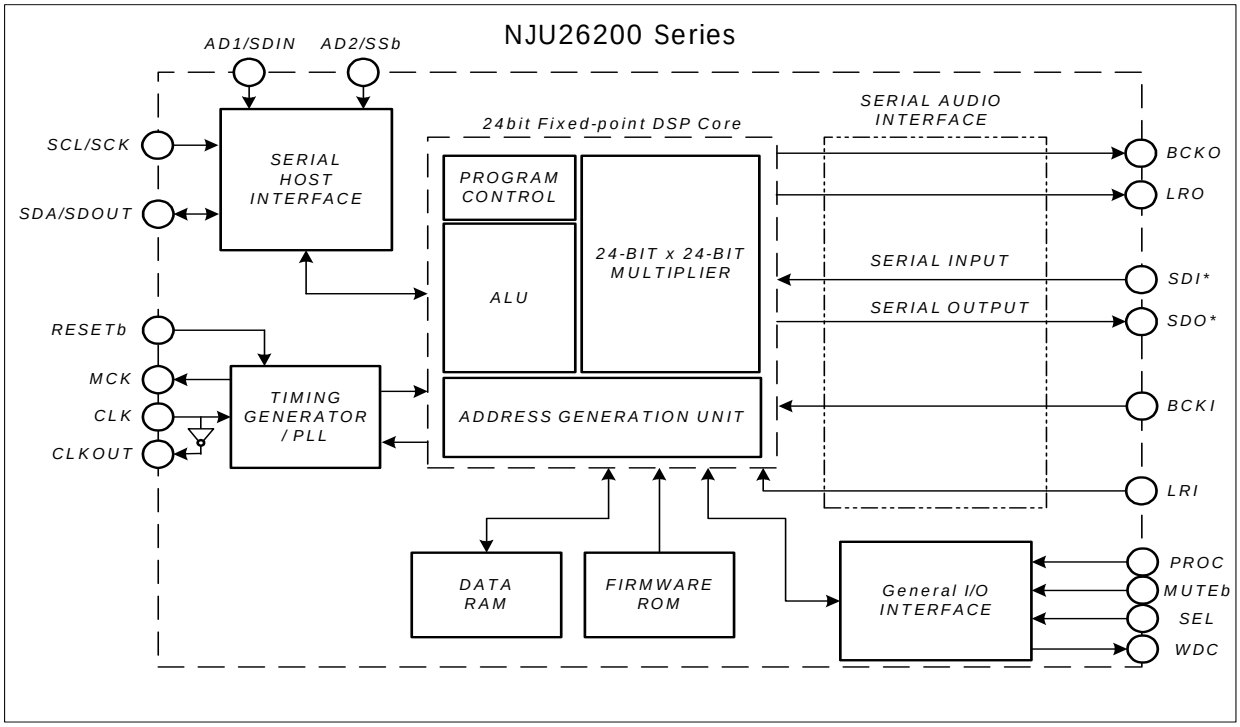


Fig.1 NJU26200 Series Hardware Block Diagram

■ Pin Configuration

(1) LQFP48-R3

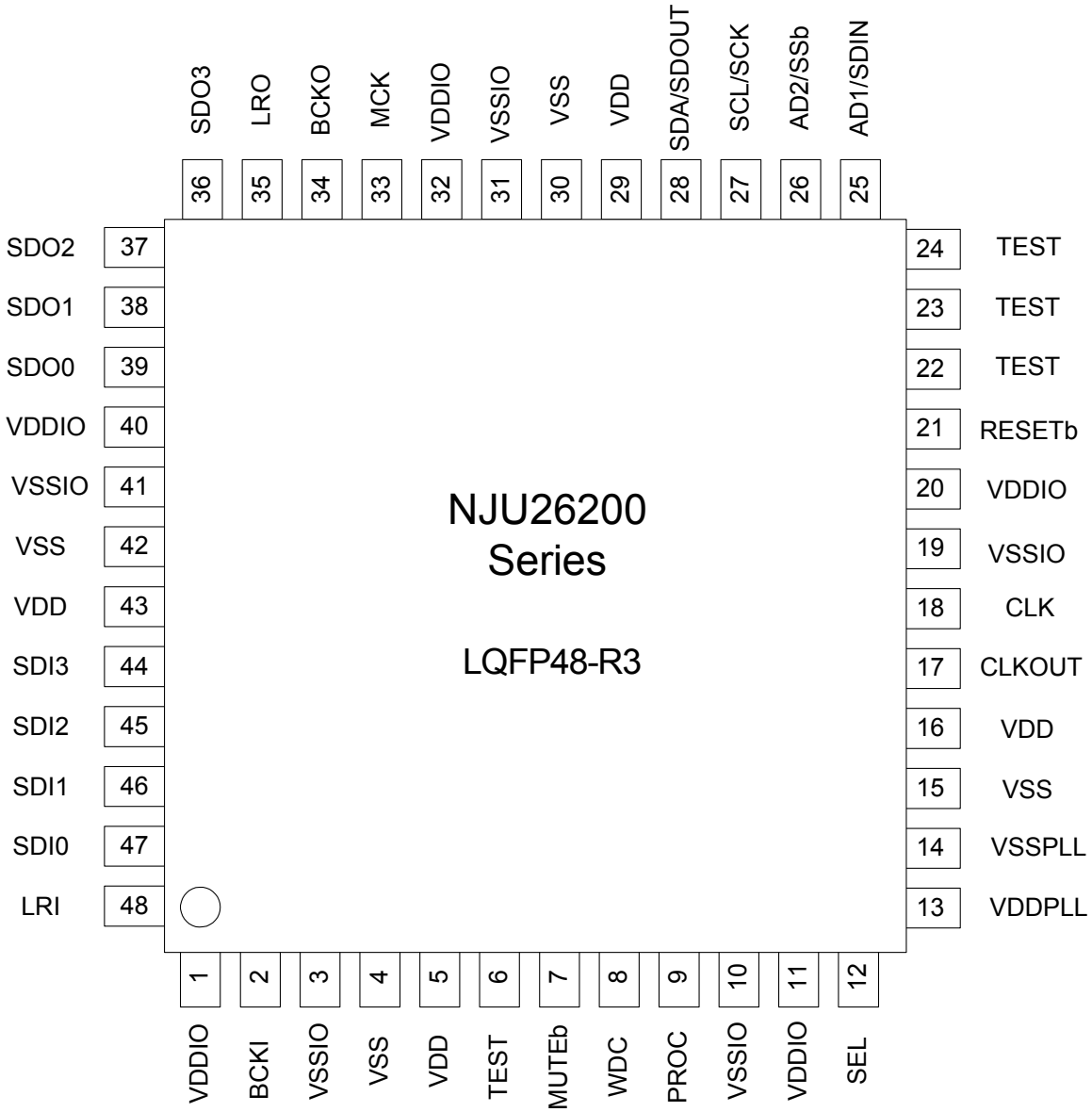


Fig. 2 LQFP48-R3 Pin Configuration

(2) SSOP44

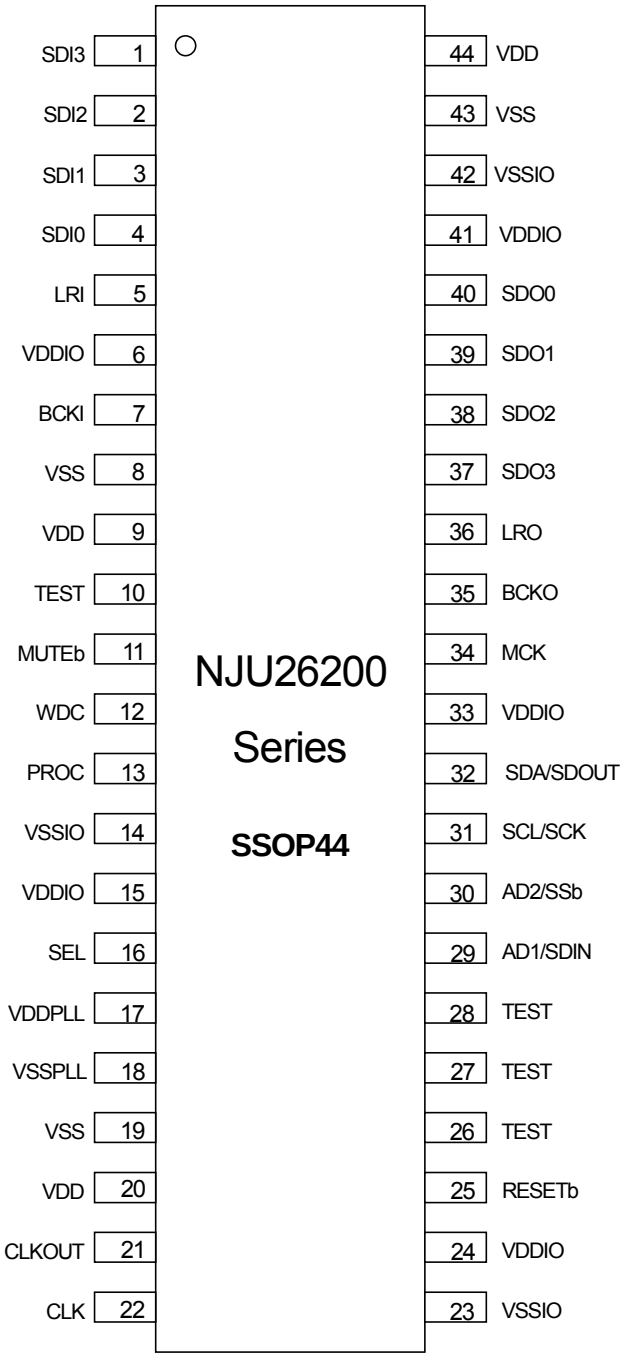


Fig.3 SSOP44 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.		Symbol	I/O	Function
LQFP48-R3	SSOP44			
1,11,20,32,40	6,15,24,33,41	VDDIO	-	I/O Power Supply +3.3V
2	7	BCKI	I	Bit Clock Input
3,10,19,31,41	14,23,42	VSSIO	-	I/O Power Supply GND
4,15,30,42	8,19,43	VSS	-	DSP Core Power Supply GND
5,16,29,43	9,20,44	VDD	-	DSP Core Power Supply +1.8V
6	10	TEST	I	for test (connect with VSSIO through 3.3kΩ resistance.)
7	11	MUTEb *	I	Master Volume Status after reset '1': 0dB, '0': Mute
8	12	WDC *	OD	Watchdog Clock output pin (Open-Drain Output)
9	13	PROC *	I	Signal Processing after reset '1': Normal Processing, '0': Waiting for a Command without Processing
12	16	SEL	I	Host Interface Selection '1': Serial Interface, '0': I^2C bus
13	17	VDDPLL	-	PLL Power Supply +1.8V
14	18	VSSPLL	-	PLL Power Supply GND
17	21	CLKOUT	O	OSC Clock Output
18	22	CLK	I	OSC Clock Input
21	25	RESETb	I	Reset (RESETb='0': DSP Reset)
22	26	TEST	I	for test (connect to VDDIO)
23,24	27,28	TEST	I	for test (connect to VSSIO)
25	29	AD1/SDIN	I	I^2C Address (I^2C mode) / Serial In (4-wire serial mode)
26	30	AD2/SSb	I	I^2C Address (I^2C mode) / Serial enable (4-wire serial mode)
27	31	SCL/SCK	I	I^2C SCL (I^2C mode) / Serial clock (4-wire serial mode)
28	32	SDA/SDOUT	I/O	I^2C SDA (I^2C mode) / Serial Out (4-wire serial mode) - I^2C Bus mode : SDA pin requires a pull-up resistance. - 4-wire Serial mode : SDOUT does not require a pull-up resistance.
33	34	MCK	O	Master Clock Output (buffer output of a CLK pin)
34	35	BCKO	O	Bit Clock Output
35	36	LRO	O	LR Clock Output
36	37	SDO3	O	Audio Data Output ch.3
37	38	SDO2	O	Audio Data Output ch.2
38	39	SDO1	O	Audio Data Output ch.1
39	40	SDO0	O	Audio Data Output ch.0
44	1	SDI3	I	Audio Data Input ch.3
45	2	SDI2	I	Audio Data Input ch.2
46	3	SDI1	I	Audio Data Input ch.1
47	4	SDI0	I	Audio Data Input ch.0
48	5	LRI	I	LR Clock Input

I : Input
O : Output
OD : Open-Drain Output
I/O : Bidirectional

Note : Pins symbol with * : Connect with VDDIO or VSSIO through 3.3kΩ resistance
SDI0 to SDI3, SDO0 to SDO3 are different by any function. Refer to each datasheet.

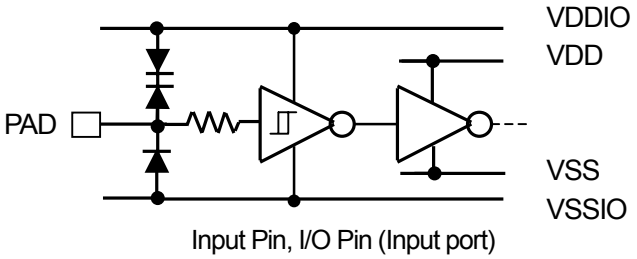
■ Absolute Maximum Ratings

Table2 Absolute Maximum Ratings (V_{SS}=V_{SSPLL}=V_{SSIO}=0V, Ta=25°C)

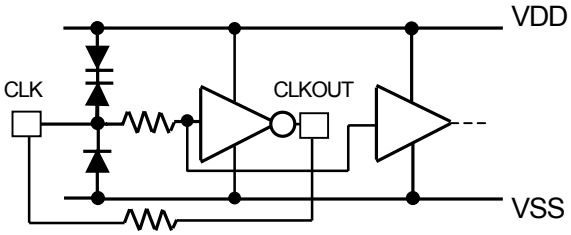
Parameter		Symbol	Rating	Units
Supply Voltage	Logic	V_{DD}	-0.3 to 2.1	V
	PLL	V_{DDPLL}	-0.3 to 2.1	
	I/O	V_{DDIO}	-0.3 to 3.8	
Terminal Voltage *	In	V_x	-0.3 to 5.5 (V_{DDIO}≥3.0V) -0.3 to 3.8 (V_{DDIO}<3.0V)	V
	I/O	$V_{x(I/O)}$	-0.3 to 3.8	
	Out	$V_{x(OUT)}$	-0.3 to 3.8	
	CLK	$V_{x(CLK)}$	-0.3 to 2.1	
	CLKOUT	$V_{x(CLKOUT)}$	-0.3 to 2.1	
Power Dissipation		P_D	300	mW
Operating Temperature		T_{OPR}	-40 to 85	°C
Storage Temperature		T_{STR}	-40 to 125	°C

* V_x : LQFP48-R3 ->No. 2, 12, 21 to 27, 44 to 48 pin SSOP44->No. 1 to 5, 7, 16, 25 to 31 pin
* $V_{x(I/O)}$: LQFP48-R3->No. 6 to 9, 28 pin SSOP44->No. 10 to 13, 32 pin
* $V_{x(OUT)}$: LQFP48-R3->No. 33 to 39 pin SSOP44->No. 34 to 40 pin
* $V_{x(CLK)}$: LQFP48-R3->No. 18 pin SSOP44->No.22 pin
* $V_{x(CLKOUT)}$: LQFP48-R3->No. 17 pin SSOP44->No.21 pin

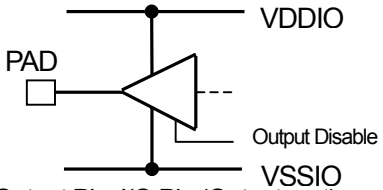
■ Equivalent Circuits



Input Pin, I/O Pin (Input port)
(LQFP48-R3->No.2, 6 to 9, 12, 21 to 28, 44 to 48 pin)
(SSOP44->1 to 5, 7, 10 to 13, 16, 25 to 32 pin)



CLK/CLKOUT Pin
(LQFP48-R3->No.17, 18 pin)
(SSOP44->No. 21, 22 pin)



Output Pin, I/O Pin (Output port)
(LQFP48-R3->No. 6 to 9, 28, 33 to 39 pin)
(SSOP44->No.10 to 13, 34 to 40 pin)

Fig.4 NJU26200 Series Equivalent Circuits

■ Electric Characteristics

Table3 Electric Characteristics **(V_{DD}=V_{DDPLL}=1.8V, V_{DDIO}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)**

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating Voltage	Logic	V_{DD}	V_{DD} Pin	1.7	1.8	1.9	V
	PLL	V_{DDPLL}	V_{DDPLL} Pin	1.7	1.8	1.9	
	I/O	V_{DDIO}	V_{DDIO} Pin	3.0	3.3	3.6	
Operating Current *1	Logic	I_{DD}	V_{DD}=V_{DDPLL}=1.8V V_{DDIO}=3.3V	-	31	-	mA
	PLL	I_{DDPLL}		-	4.0	-	
	I/O	I_{DDIO}		-	1.0	-	
High Level Input Voltage *2	In	V_{IH}	V_{DDIO}=3.0 to 3.6V	V_{DDIO} x 0.7	-	5.25	V
	I/O	$V_{IH(I/O)}$	V_{DDIO}=3.0 to 3.6V	V_{DDIO} x 0.7	-	V_{DDIO}	V
	CLK	$V_{IH(OSC)}$	V_{DD}=1.7 to 1.9V V_{DDIO}=3.0 to 3.6V	V_{DD} x 0.7	-	V_{DD}	
Low Level Input Voltage *2	In, I/O	V_{IL}, $V_{IL(I/O)}$	V_{DDIO}=3.0 to 3.6V	0	-	0.5	V
	CLK	$V_{IL(OSC)}$	V_{DD}=1.7 to 1.9V V_{DDIO}=3.0 to 3.6V	0	-	V_{DD} x 0.3	
Terminal Leakage Current *2	In, I/O	I_{IN}, $I_{IN(I/O)}$	V_{IN} = V_{SSIO} to V_{DDIO}	-10	-	10	µA
	CLK	$I_{IN(OSC)}$	V_{IN} = V_{SS} to V_{DD}	-15	-	15	µA
High Level Output Voltage *2	Out, I/O	V_{OH}, $V_{OH(I/O)}$	I_{OH}= -2mA V_{DDIO}=3.0 to 3.6V	V_{DDIO} x 0.85	-	V_{DDIO} *3	V
	CLKOUT	$V_{OH(OSC)}$	I_{OH}=-100µA V_{DD}=1.7 to 1.9V	V_{DD} x 0.85	-	V_{DD} *3	
Low Level Output Voltage *2	Out, I/O	V_{OL}, $V_{OL(I/O)}$	I_{OL}=2mA V_{DDIO}=3.0 to 3.6V	0	-	V_{DDIO} x 0.15	V
	CLKOUT	$V_{OL(OSC)}$	I_{OL}=100µA V_{DD}=1.7 to 1.9V	0	-	V_{DD} x 0.15	
Input Rise/Fall Transition Time		t_r / t_f	*4	-	-	100	ns
Clock Frequency		f_{OSC}	No.18pin(CLK) *5	12.0-	12.288	12.5	MHz
Ext. System Clock Duty Cycle		r_{EC}	No.18pin (CLK)	45	50	55	%

*1 The operating current value at default status is a measured value at Ta=25°C on EVA Board.

*2 $V_{IH(OSC)}$, $V_{IL(OSC)}$, $I_{IN(OSC)}$: No.18 pin/LQFP48-R3, No.22pin/SSOP44 (Clock Input Pin)

$V_{IH(I/O)}$, $V_{IL(I/O)}$, $V_{OH(I/O)}$, $V_{OL(I/O)}$, $I_{IN(I/O)}$: No.6 to No.9, No,28 pin/LQFP48-R3, No.10 to No.13, No.32/SSOP44 (Bidirectional Pin)

$I_{IN(I/O)}$: It include terminal leakage current at output high impedance.

$V_{OH(OSC)}$, $V_{OL(OSC)}$: No.17pin/LQFP48-R3, No.21pin/SSOP44 (Clock Output Pin)

*3 Do not carry out the pull-up of the output terminals on the voltage more than V_{DDIO}.
Connect an unused input terminals and I/O terminals to VDDIO or VSSIO.

*4 The tr / tf of LQFP48-R3:No.25 to No.28 pins (SSOP44:No.29 to 32 pin) are specified separately by the operational mode (I^2C / 4-Wire Serial).

*5 Please give usually the clock of 12.288MHz.

NOTICE:

The input impedance of CMOS IC is very high. Therefore, the noise is picked up easily when the input terminal and the I/O terminal (input mode) are opened, and IC is not steady. Moreover, it causes the terminal to be damaged. Please do not use it with the input terminal and the I/O terminal open.

1. Clock and Reset

1.1 Power Supply

The NJU26200 Series has three power supplies V_{DD}/V_{SS}, V_{DDPLL}/V_{SSPLL} and V_{DDIO}/V_{SSIO}. V_{DD}/V_{SS} is used as an internal core supply, V_{DDPLL}/V_{SSPLL} is used as an internal PLL power supply and V_{DDIO}/V_{SSIO} is used as an I/O terminal power supply.

The power supply is turned on or turned off in order of the follow.

The power supply is turned on : V_{DDIO} -> V_{DD}, V_{DDPLL}
The power supply is turned off : V_{DDPLL}, V_{DD} -> V_{DDIO}

When V_{DD} and V_{DDPLL} are made another power supply, V_{DDPLL} is recommended to be turned on the end. Turn off of a power supply by the reverse sequence of turning on the power supply.

NOTICE:

To setup good power supply condition, the decoupling capacitors should be implemented at power supply terminals. Supply voltage must be within recommended operating voltage. Furthermore supplying power voltage must be linear, quick and smooth to prevent abnormal operation. Once the power supply is set up, supply voltage must be kept within the operating voltage range. After setting up the power supply, even if the supply voltage dropped off and recovered to normal range, reset function and the all following operations can not be guaranteed. After using this DSP, power supply must be dropped to V_{SS} level.

The V_{DDPLL}/V_{SSPLL} supplies the power for internal PLL circuit. The V_{DDPLL}/V_{SSPLL} is sensitive to power-line noise. The V_{DDPLL}/V_{SSPLL} line should be separate from internal core power supply V_{DD} or provide noise filters to prevent from power supply noise.

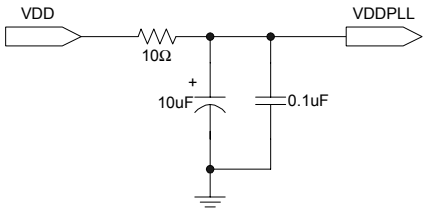


Fig. 5 The example of a simple power supply filter

1.2. Clock

The NJU26200 Series CLK pin requires the system clock. The system clock is usually 12.288MHz into CLK pin. The CLK/CLKOUT pins can generate the system clock by connecting the crystal oscillator. Refer to the application circuit diagram about the circuit parameters. The crystal oscillator uses the one of the fundamental. There is not necessary to connect the negative feedback resistor outside because negative feedback resistor is built into.

NOTICE:

The NJU26200 has an internal PLL circuit, which is designed on 12.288MHz. In case of the system clock is lower than 12.0MHz, NJU26200 does not operate and is not able to process audio correctly. If the frequency needs to change due to EMI problem or external components, it must be with the frequency range shown in Table 3. In this case, be careful of changing the divided frequency.

Contact with a manufacture maker about use of a crystal oscillator.

When the external oscillator is connected to CLK/CLKOUT pins, check the voltage level of the pins. Because the maximum input voltage level of CLK pin is deferent from the other input or bidirectional pins. The maximum voltage-level of CLK pin equals to V_{DD}.

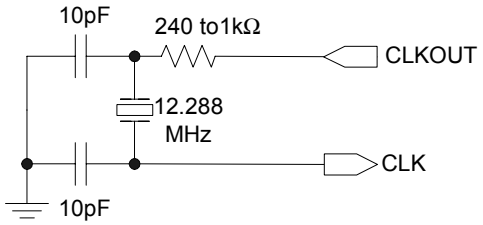


Fig. 6 The example of the oscillator circuit

Note: After Reset, MCK pin outputs clock that is supplied from CLK pin. If MCK is not necessary, NJU26200 stops clock output by command.

1.3. Reset

To initialize the NJU26200 Series, RESETb pin should be set 'Low' level during some period. After some period of 'Low' level, RESETb pin should be 'High' level. This procedure starts the initialization of the NJU26200 Series. After the power supply and the oscillation of the NJU26200 Series becomes stable, RESETb pin should be kept Low-level more than t_{RESETb} period.

To select I^2C bus or 4-Wire serial bus, some level should be supplied to SEL pin. When SEL pin='Low', I^2C bus is selected. When SEL pin='High', 4-Wire serial bus is selected.

After RESETb pin level goes to 'High', the NJU26200 internal hardware setting in the host interface is finished in 1 m sec, and the NJU26200 is able to communicate with the host controller.

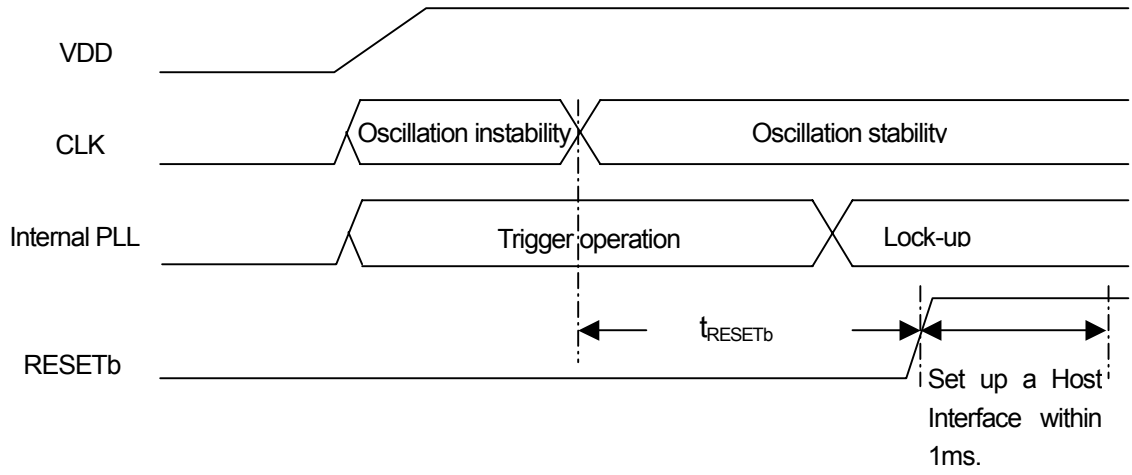


Fig. 7 Reset Timing

Table 4 Reset Time

Symbol	Time
t_{RESETb}	≥300μs

Note : The built-in PLL is triggered after the power-on. If stopping to providing the clock during operation and changing the frequency, or reset function is needed for some reason, the 'RESETb' pin must be kept at 'Low' level during t_{RESETb} with providing normal clock. After then, initial setting is required.

When the 'RESETb' is changed from 'High' level to 'Low' level with providing normal clock, the NJU26200 provides a reset pulse with 32-times speed of clock timing(ex. approx 2.6us at CLK=12.288MHz) and PLL is re-triggered. When the 'RESETb' is changed from 'Low' level to 'High' level, re-triggered is not executed.

Do not stop providing clock during operation. If stopped, the built-in PLL can not provide a normal clock toward internal NJU26200 and NJU26200 doesn't work correctly.

2. Digital Audio Clock

Digital audio data needs to synchronize and transmit between digital audio systems.
The NJU26200 Series - master mode / slave mode - both of the modes are supported.

Note: Although the NJU26200 Series is usually used as a slave device, it can also be used as MASTER device. The clock frequency supplied to the NJU26200 Series is 12.288MHz. **When the NJU26200 Series is in MASTER mode,** the NJU26200 Series can generate a required system clock to 32kHz/48kHz/64kHz/96kHz of sampling frequency and can't generate a required system clock 44.1kHz/88.2kHz of sampling frequency. (Table 5)

- In Master mode ; Use the clock of BCKO and a LRO pin output clock for digital audio data transfer.
- In Slave mode ; The clock output from a master device is needed for the input terminal of BCKI and LRI.

2.1 Audio Clock

Three kinds of clocks are needed for digital audio data transfer.

(1) LR clock (LRI, LRO) is needed by serial-data transmission. It is the same as the sampling frequency of a digital audio signal.
(2) Bit clock (BCKI, BCKO) is needed by serial-data transmission. It becomes the multiple of LR clock.
(3) Master clock (MCK) needed by A/D, D/A converter, etc. It becomes the multiple of LR clock. It is not related to serial audio data transmission.

The NJU26200 supports serial data format that includes 32(32fs) or 64(64fs) BCK clocks.

Table 5 Sampling Frequency and BCK, LR, MCK (CLK=12.288MHz)

Mode	Clock Signal	Multiple Frequency	32kHz	44.1kHz	48kHz	64kHz	88.2kHz	96kHz
DSP Slave	LRI	1fs	32kHz	44.1kHz	48kHz	64kHz	88.2kHz	96kHz
	BCKI(32Fs)	32fs	1.024MHz	1.4112MHz	1.536MHz	2.048MHz	2.822MHz	3.072MHz
	BCKI(64Fs)	64fs	2.048MHz	2.822MHz	3.072MHz	4.096MHz	5.644MHz	6.144MHz
DSP Master	LRO	1fs	32kHz	Not possible	48kHz	64kHz	Not possible	96kHz
	BCKO(32Fs)	32fs	1.024MHz		1.536MHz	2.048MHz		3.072MHz
	BCKO(64Fs)	64fs	2.048MHz		3.072MHz	4.096MHz		6.144MHz
(Common)	MCK (384/256/ 192/128Fs)	384Fs @fs=32kHz 256Fs @fs=48kHz 192Fs @fs=64kHz 128Fs @fs=96kHz	12.288MHz					

Note: Please refer to each datasheet because sampling frequency that NJU26200 series are able to operate vary with each firmware specification.

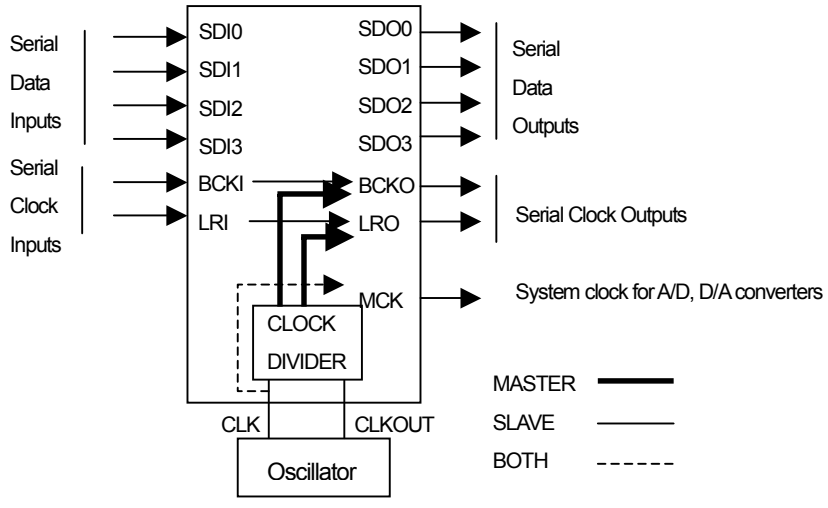


Fig. 8 MASTER / SLAVE Mode

3. Digital Audio Interface

3.1 Digital Audio Data Format

The NJU26200 Series can use three kinds of formats hereafter as industry-standard digital audio data format.
(1) I^2S : MSB is put on the 2nd bit of LR clock change rate.(1 bit is delayed to left stuffing)
(2) Left-justified : LR clock -- MSB is placed for changing.
(3) Right-justified : LSB is placed just before LR clock change rate.
The main differences among three kinds of formats are in the position relation between LR clock (LRI, LRO) and an audio data (SDI, SDO).
- In every format: : a left channel is transmitted previously.
- In Right/Left-justified : LR clock ='High' shows a left channel.
- I^2S : LR clock="Low" shows a left channel.
- The Bit clock BCK (BCKI, BCKO) is used as a shift clock of transmission data. The number of clocks more than the number of sum total transmission bits of a L/R channel is needed at least.
- One cycle of LR clock is one sample of a stereo audio data. The frequency of LR clock becomes equal to a sample rate (fs).

The NJU26200 supports serial data format that includes 32(32fs) or 64(64fs) BCK clocks.

3.2 Serial Audio Data Input/output

The NJU26200 Series audio interface includes 4 data input lines: SDI0, SDI1, SDI2 and SDI3 (Table 6).
4 data output lines: SDO0, SDO1, SDO2 and SDO3. (Table 7). Refer to each datasheet.

Table 6 Serial Audio Input Pin Description

Pin No.		Symbol	Description
LQFP48-R3	SSOP44		
47	4	SDI0	Audio Data Input 0
46	3	SDI1	Audio Data Input 1
45	2	SDI2	Audio Data Input 2
44	1	SDI3	Audio Data Input 3

Table 7 Serial Audio Output Pin Description

Pin No.		Symbol	Description
LQFP48-R3	SSOP44		
39	40	SDO0	Audio Data Output 0
38	39	SDO1	Audio Data Output 1
37	38	SDO2	Audio Data Output 2
36	37	SDO3	Audio Data Output 3

The NJU26200 Series can use three kinds of formats hereafter as industry-standard digital audio data format; (1) I^2S (2) Left-Justified (3) Right-justified and 16 / 18 / 20 / 24bits data length. (Fig.9-1 to Fig.9-12) An audio interface input and output data format become the same data format.

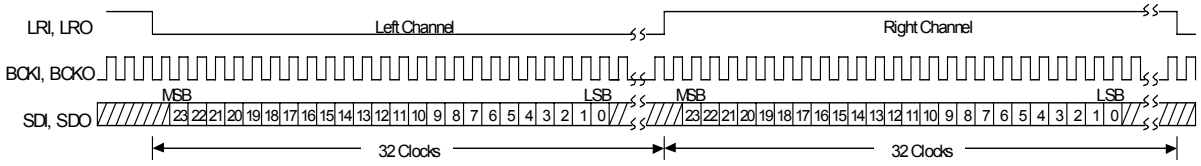


Fig.9-1 I^2S Data Format 64fs, 24bit Data

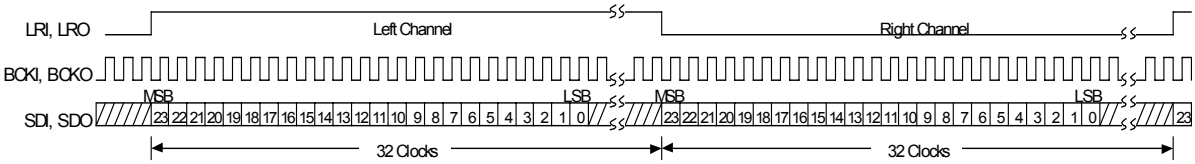


Fig.9-2 Left-Justified Data Format 64fs, 24bit Data

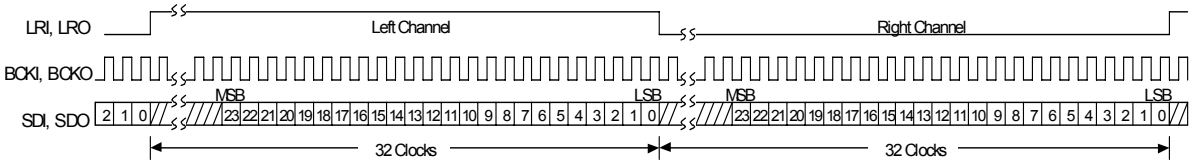


Fig.9-3 Right-Justified Data Format 64fs, 24bit Data

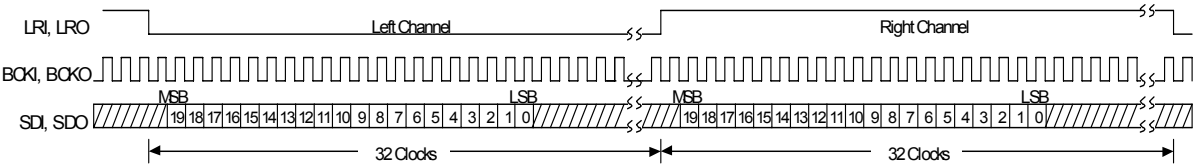


Fig.9-4 I^2S Data Format 64fs, 20bit Data

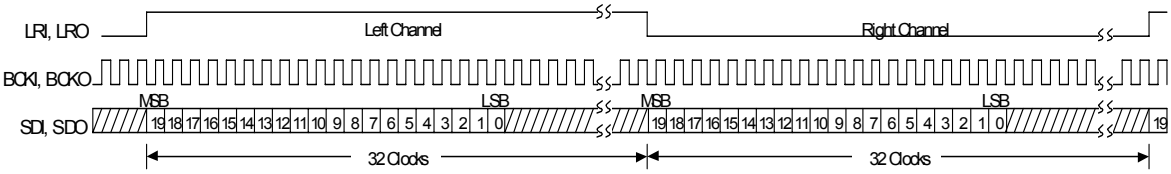


Fig.9-5 Left-Justified Data Format 64fs, 20bit Data

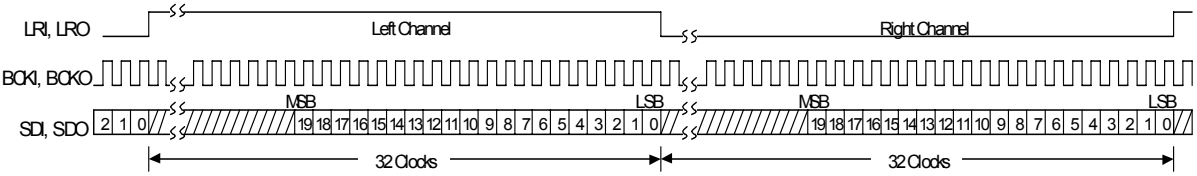


Fig.9-6 Right-Justified Data Format 64fs, 20bit Data

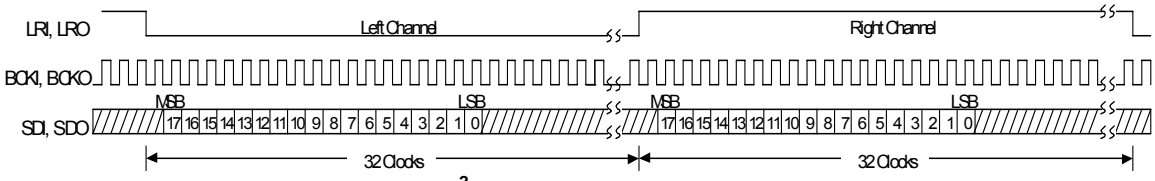


Fig.9-7 I²S Data Format 64fs, 18bit Data

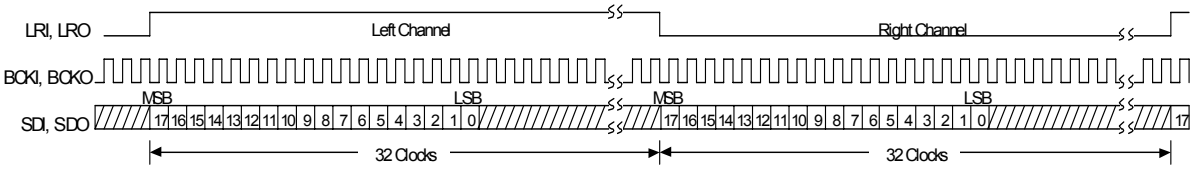


Fig.9-8 Left-Justified Data Format 64fs, 18bit Data

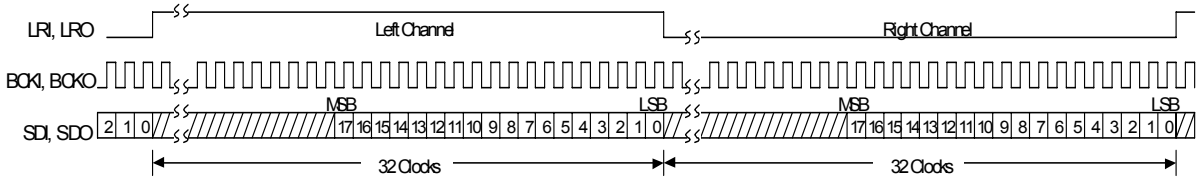


Fig.9-9 Right-Justified Data Format 64fs, 18bit Data

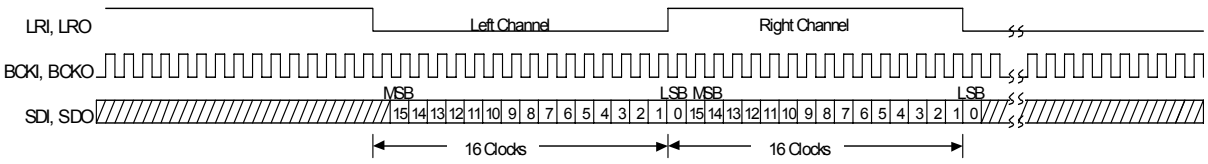


Fig.9-10 I²S Data Format 32fs, 16bit Data

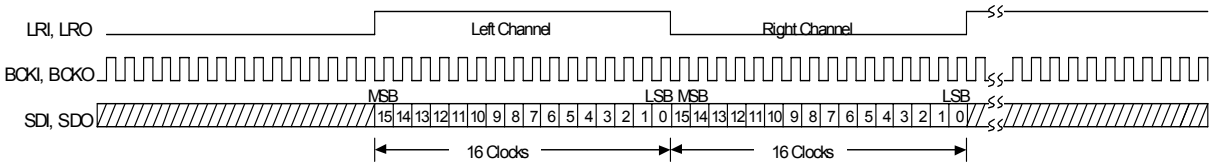


Fig.9-11 Left-Justified Data Format 32fs, 16bit Data

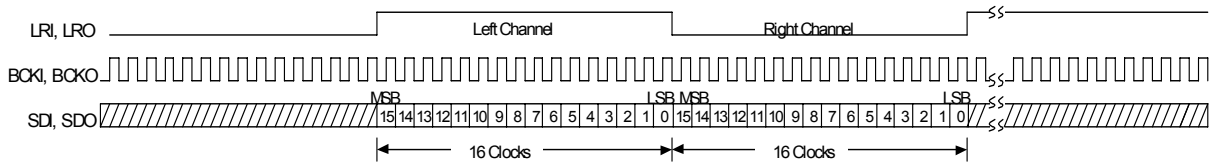


Fig.9-12 Right-Justified Data Format 32fs, 16bit Data

3.3 Serial Audio Input Timing

Table 8 Serial Audio Input Timing Parameters (V_{DD}=V_{DDPLL}=1.8V, V_{DDIO}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)

Parameter		Symbol	Test Condition	Min	Typ.	Max	Units
BCKI Frequency	*1	f_{BCKI}		-	-	6.5	MHz
BCKI Period	*1						
Low Pulse Width		t_{SIL}		75	-	-	ns
High Pulse Width		t_{SIH}		75			
BCKI to LRI Time	*1	T_{SLI}		40	-	-	ns
LRI to BCKI Time	*1	t_{LSI}		40	-	-	ns
Data Setup Time	*2	t_{DS}		15	-	-	ns
Data Hold Time	*2	t_{DH}		15	-	-	ns

*1 It is the regulation in slave mode.

*2 It is the regulation to BCKI in slave mode and to BCKO in master mode.

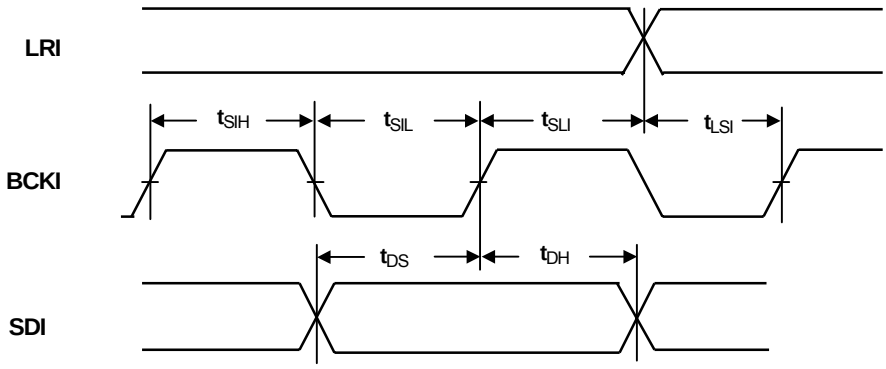


Fig.10 Serial Audio Input Timing

Table 9 Serial Audio Output Timing Parameters (V_{DD}=V_{DDPLL}=1.8V, V_{DDIO}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCKO to LRO Time *3	t_{SLO}	C_L:LRO, BCKO, SDO=25pF	-15	-	15	ns
Data Output Delay	t_{DOD}		-	-	15	ns

*3 It is the regulation in master mode.

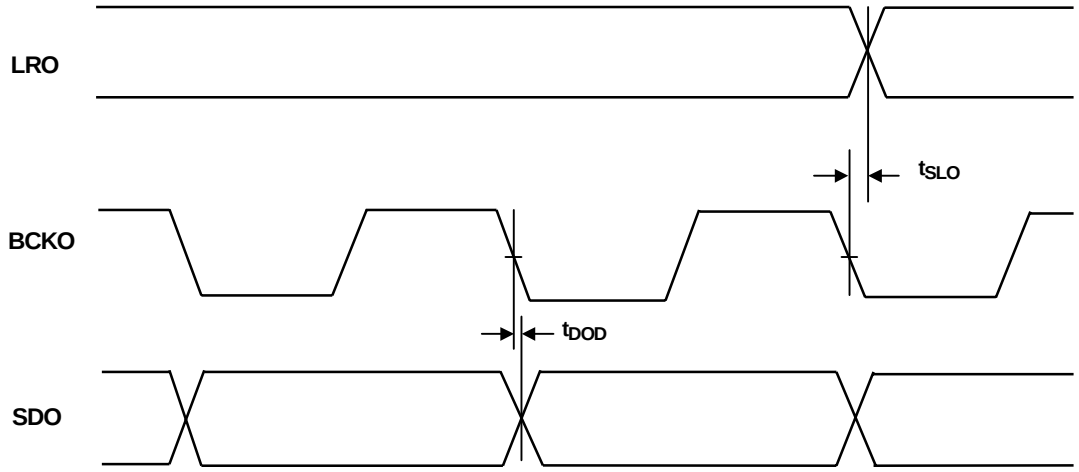


Fig.11 Serial Audio Output Timing

Table 10 Serial Audio Clock Timing Parameters (In slave mode)

(V_{DD}=V_{DDPLL}=1.8V, V_{DDIO}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
Clock Output Delay (LRI --> LRO)	t_{PDL}	C_L:LRO,BCKO, SDO=25pF	-	-	15	ns
Clock Output Delay (BCKI --> BCKO)	t_{PDB}		-	-	15	ns

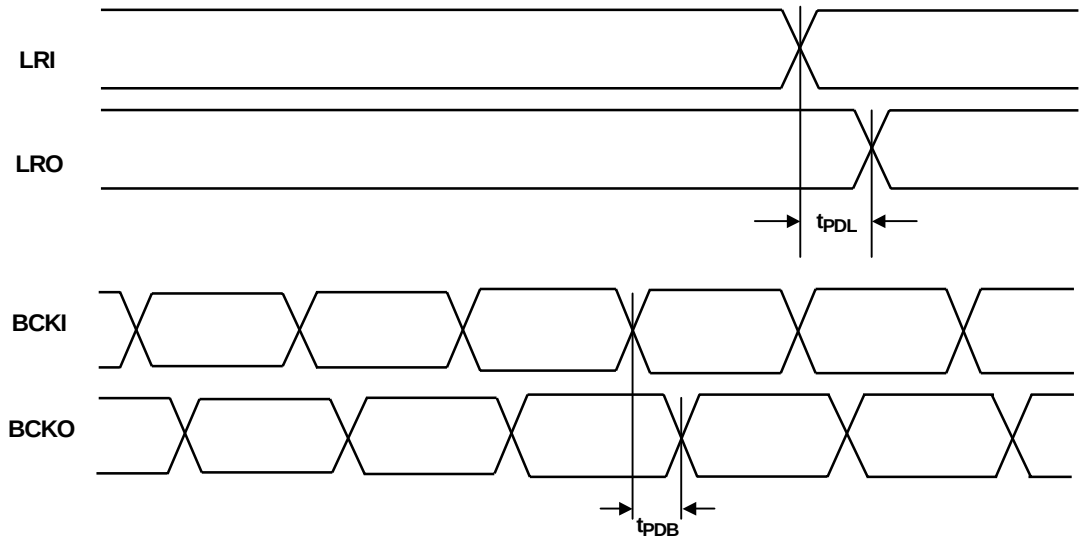


Fig.12 Serial Audio Clock Timing (In slave mode)

4. Host Interface

The NJU26200 Series can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or I²C bus.(Table 11) Data transfers are in 8 bit packets (1 byte) when using either format.
Serial Host Interface Pin Description.(Table 12)

Table 11 Host Interface setting

Pin No.		Symbol	Setting	Host Interface
LQFP48-R3	SSOP44			
12	16	SEL	"Low"	I²C bus
			"High"	4-Wire serial bus

Table 12 Host Interface Pin Description

Pin No.		Symbol (I²C bus / Serial)	I²C bus Format	4-Wire Serial bus Format
LQFP48-R3	SSOP44			
25	29	AD1 / SDIN	I²C bus address Bit1	Serial Data Input
26	30	AD2 / SSb	I²C bus address Bit2	Serial enable
27	31	SCL / SCK	Serial Clock	Serial Clock
28	32	SDA / SDOUT	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (CMOS)

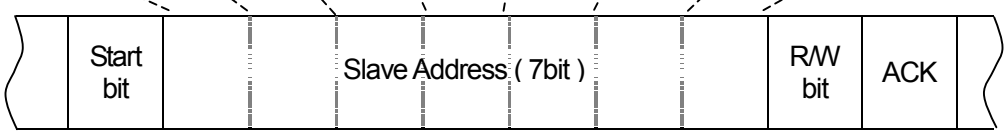
Note: When 4-Wire Serial bus is selected, The SDA/SDOUT pin is CMOS output. The SDOUT pin does not require a pull-up resistance.
When I²C Bus is selected, this pin is a bi-directional Open Drain output. This pin, which is assigned for I²C Bus, requires a pull-up resistance.
The SDA/SDOUT pin isn't +5.0V Input tolerant. Please note the voltage level (Max voltage is VDDIO).

4.1 I²C bus

When the NJU26200 Series is configured for I²C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 13)

Table 13 I²C bus SLAVE Address

bit7	bit6	*1 bit5	bit4	bit3	AD2 bit2 *2	AD1 bit1 *2	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



*1 : Refer to the software specification.
*2 : SLAVE address is 0 when AD1/AD2 is "Low". SLAVE address is 1 when AD1/AD2 is "High".

Note : The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” I^2C bus data transfer. Moreover, after sending S ("START" condition), Sr (repeated "START" condition) is not received but it becomes the waiting for the P ("STOP" condition). Therefore, please be sure to send P ("STOP" condition).

Table 14 I^2C Bus Interface Timing Parameters (V_{DD}=V_{DDPLL}=1.8V, V_{DDIO}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)

Parameters		Symbol	Min	Max	Units
SCL Clock Frequency		f_{SCL}	0	400	kHz
Start Condition Hold Time		$t_{HD:STA}$	0.6	-	µs
SCL ‘Low’ Duration		t_{LOW}	1.3	-	µs
SCL ‘High’ Duration		t_{HIGH}	0.6	-	µs
Data Hole Time	*3	$t_{HD:DAT}$	0	-	µs
Data Setup Time		$t_{SU:DAT}$	250	-	ns
Rising Time		t_R	-	1000	ns
Falling Time		t_F	-	300	ns
Stop Condition Setup Time		$t_{SU:STO}$	0.6	-	µs
Bus Release Time	*4	t_{BUF}	1.3	-	µs

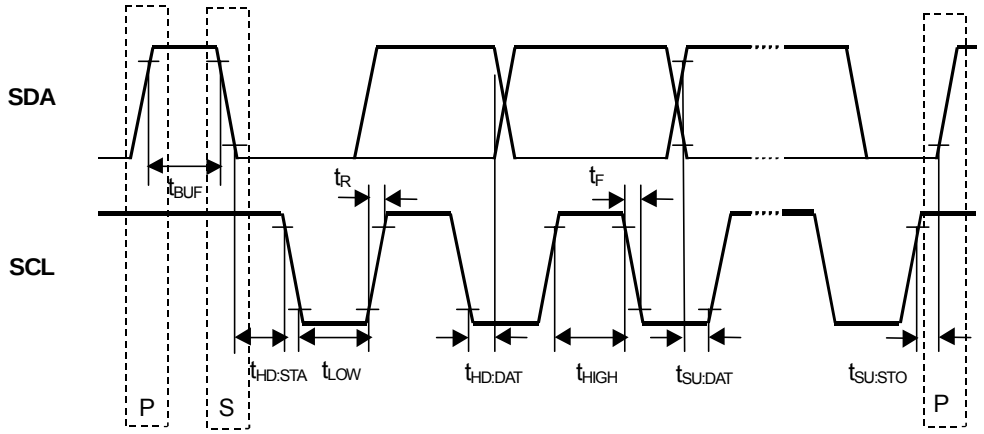


Fig.13 I^2C Bus Timing

Note:

*3 Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

*4 The interval of continuous command is accounted separately.

4.2 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) that is latched on the falling transitions of SSb. The SDOUT pin is always CMOS output. This pin does not require a pull-up resistance.

Table 15 4-Wire Serial Interface Timing Parameters (V_{DD}=V_{DDPLL}=1.8V, V_{DDIO}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Units
Input Data Rising Time	t_{MSDr}	-	-	100	ns
Input Data Falling Time	t_{MSDf}	-	-	100	ns
Serial Clock Rising Time	t_{MSCr}	-	-	100	ns
Serial Clock Falling Time	t_{MSCf}	-	-	100	ns
Serial Strobe Rising Time	t_{MSSr}	-	-	100	ns
Serial Strobe Falling Time	t_{MSSf}	-	-	100	ns
Serial Clock High Duration	t_{MSCa}	0.5	-	-	µs
Serial Clock Low Duration	t_{MSCn}	0.5	-	-	µs
Serial Clock Period	t_{MSCc}	1.0	-	-	µs
Serial Strobe Setup Time	t_{MSSs}	0.5	-	-	µs
Serial Strobe Hold Time	t_{MSSh}	0.5	-	-	µs
Serial Strobe Low Duration *5	t_{MSSa}	-	8.5	-	µs
Serial Strobe High Duration *5	t_{MSSn}	-	1.0	-	µs
Input Data Setup Time	t_{MSDis}	0.1	-	-	µs
Input Data Hold Time	t_{MSDih}	0.1	-	-	µs
Output Data Hold Time	t_{MSDoh}	-	-	0.25	µs
Output Data Turn off Time (Hi-Z)	t_{MSDov}	-	-	0.25	µs

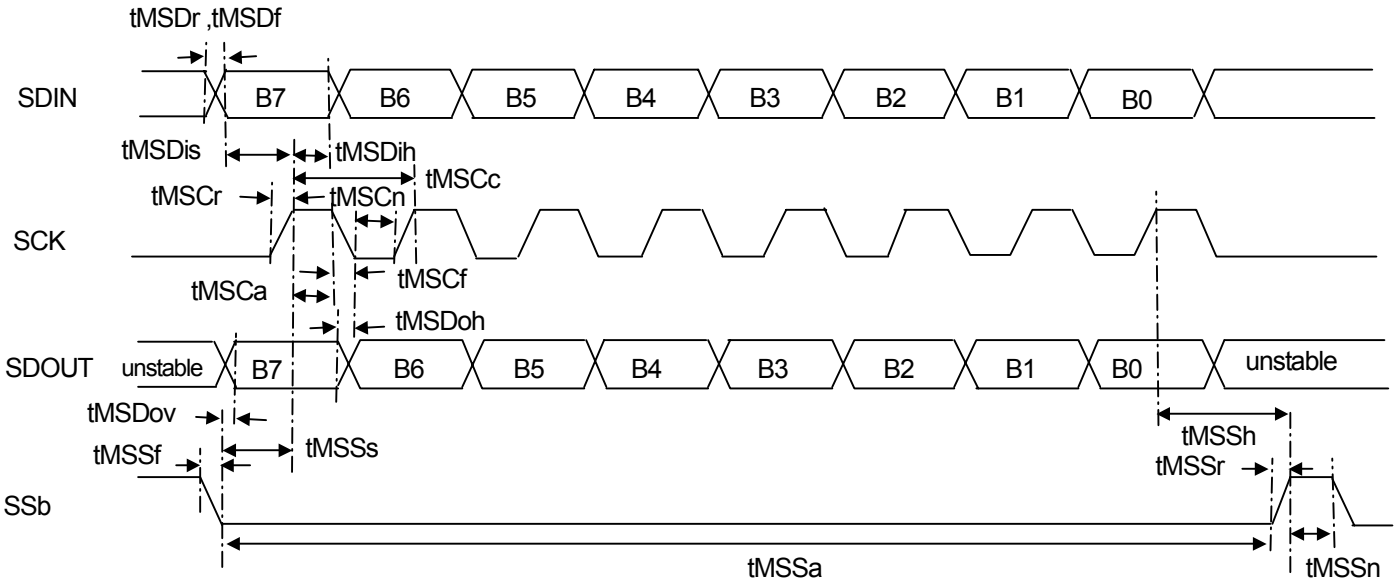


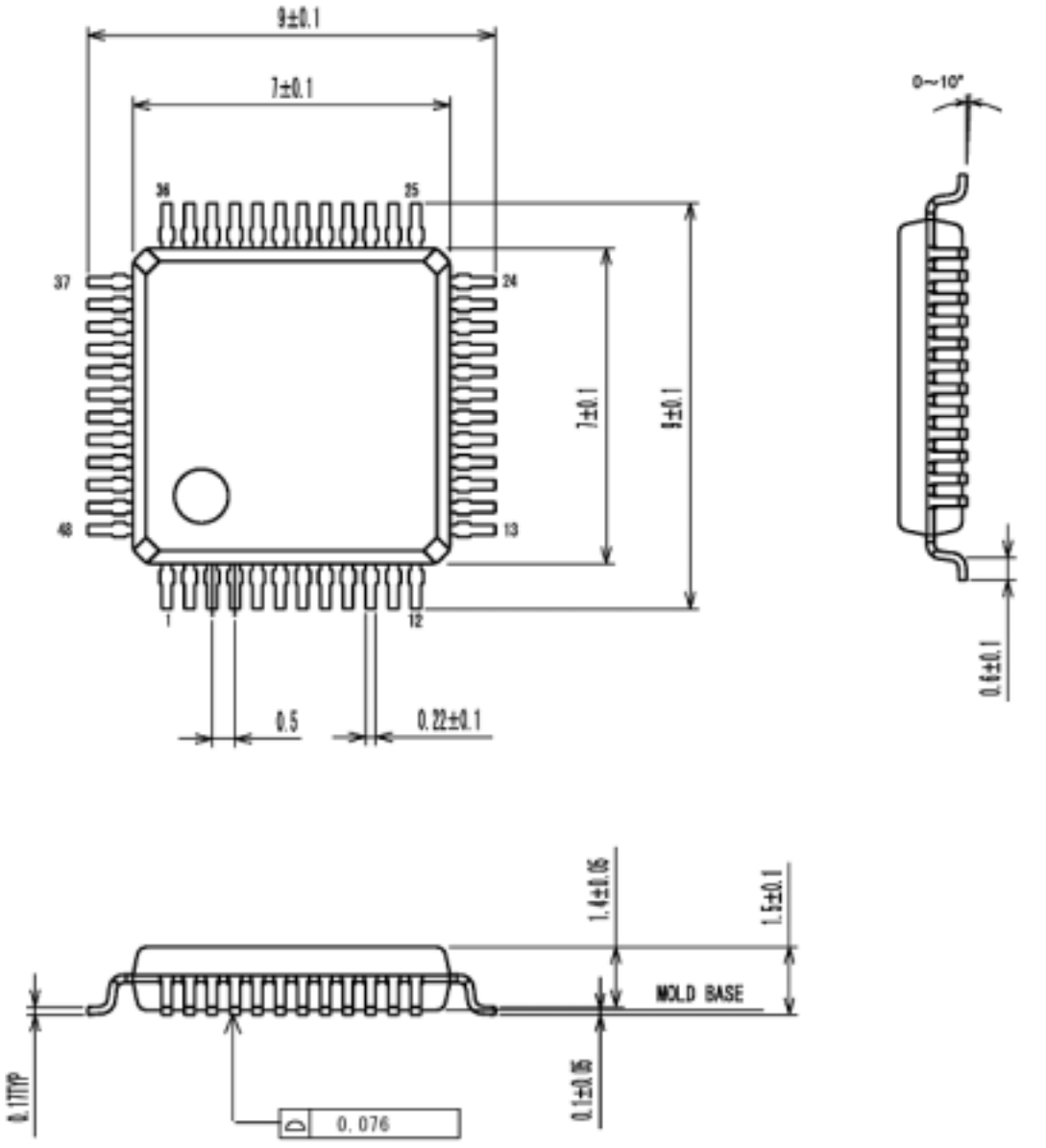
Fig.14 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High". When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.

*5 The interval of continuous command is accounted separately. Refer to each datasheet.

5. Package Dimensions

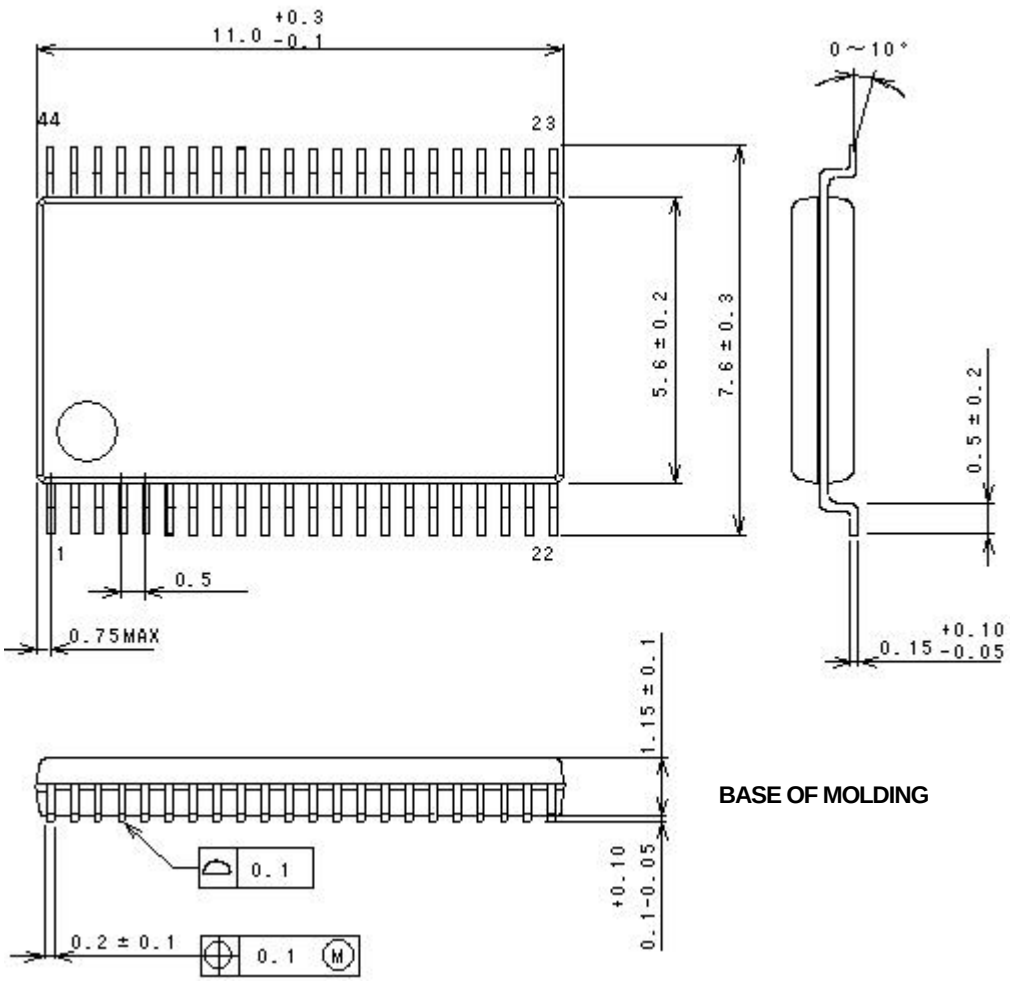
(1) LQFP48-R3, Pb-Free



MOLD MATERIAL : EPOXY RESIN

UNIT: mm

(2) SSOP44, Pb-Free



MOLD MATERIAL : EPOXY RESIN

UNIT: mm