NJU26124 Application Note

Hardware Manual

New Japan Radio Co., Ltd

Version 1.00

CONTENTS

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Hardware Manual

1.General Description

This application note describes the NJU26124 hardware applications and usages. The main items described in this document are the next three application circuits, Master/Slave mode, MCK clock, crystal oscillation circuit, reset circuit and the suggestions on the design of the NJU26124 and so on.

1) The NJU26124 application circuit with DIR and DAC (I_2C Bus)
2) The NJU26124 application circuit with ADC and DAC (I_2C Bus)
3) The NJU26124 application circuit with DIR, ADC and DAC (I_2C Bus)

2.NJU26124 Block Diagram

The NJU26124 block diagram is shown in the Figure 1.

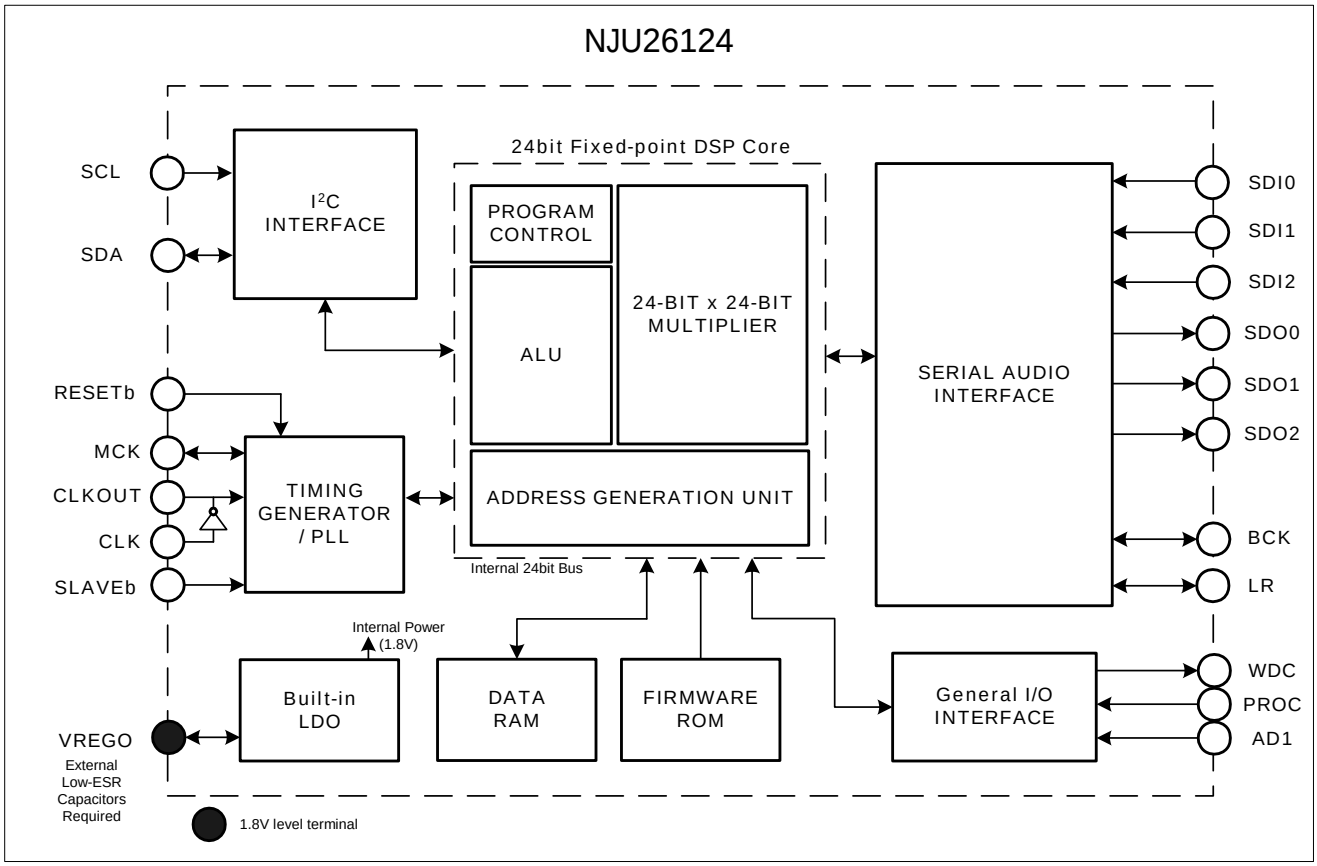

Figure 1. NJU26124 Block Diagram

Note1: The NJU26124 provides three digital audio inputs and three digital audio outputs. The application circuits do not use all inputs and outputs. The input and output circuits should be modified according to the target application.
Note2: Refer to the NJU26124 Data Sheet together with this application note.

3. Application Circuit Examples

The next three application circuits are described in this section.

1) The NJU26124 application circuit with DIR and DAC (I^2C Bus)
2) The NJU26124 application circuit with ADC and DAC (I^2C Bus)
3) The NJU26124 application circuit with DIR, ADC and DAC (I^2C Bus)

Note1: DIR: Digital Interface Receiver
ADC: Analog to Digital Converter DAC: Digital to Analog Converter
Note2: DSP denotes the NJU26124 in this document.
Note3: The ADCs and DACs operate in Slave mode in the Figure 3 to Figure 5.
Note4: The settings of SLAVEb terminal and firmware command decide Master/Slave mode of the DSP Refer to section 4.2 for detail.
Note5: A selected path after reset is described in Table1. This setting can be selected by MODE terminal. The MODE terminal should be connected to VDDIO or VSSIO through the resistor. The recommended resistor value is 3.3k-ohm.

Terminal	Symbol	Value	DSP Status After Reset
17	MODE	"High"	FIR and PEQ function are selected.
		"Low"	PEQ and time alignment are selected.

Table1. The setting of Master volume and Command operation after reset

In the application circuits of this document, the MODE terminal is "Low". After reset, NJU26124 execute the function of the DSP PEQ and time alignment.

3.1 Application circuit 1 "The NJU26124 application circuit with DIR and DAC (I^2C Bus)"

This application circuit 1 employs the digital audio signal input, for example DIR input.
The Figure 3 shows the circuit with DIR, DSP and DAC.

The DSP should operate in the Slave mode. To set up the DSP Slave mode, SLAVEb terminal should be set "Low". In case of "SLAVEb = Low", the DSP is always Slave mode regardless of the command setting (Master or Slave). Refer to the Table2.

The DIR operates as master device. Then the DIR supplies DAC with LRCK, BCK and MCK clock. Also the DIR supplies the DSP with LRCK and BCK clock.

3.2 Application circuit 2 "The NJU26124 application circuit with ADC and DAC (I^2C Bus)"

This application circuit 2 employs the analog audio signal input, for example ADC input.
The Figure 4 shows the circuit with ADC, DSP and DAC. DSP and DAC.

The DSP should operate in the Master mode. To set up the DSP Master mode, SLAVEb terminal should be set "High" and the DSP should be set Master mode by the command setting. Refer to the Table2.
In case of "SLAVEb = High", MCK terminal outputs MCK clock that is inputted to CLK terminal.

The Master-mode DSP supplies ADC and DAC with LRCK, BCK and MCK clock.

3.3 Application circuit 3 “The NJU26124 application circuit with DIR, ADC and DAC (I2C Bus)”

This application circuit 3 employs the analog audio signal input, for example ADC input, and digital audio signal input. The Figure 5 shows the circuit with DIR, ADC, DSP and DAC.

The DSP should be always set Slave mode regardless of analog or digital input.
To set up the DSP Slave mode, SLAVEb terminal should be set “High” and the DSP should be set Slave mode by the command setting. Refer to the Table2.

In case of “SLAVEb = High”, MCK terminal outputs MCK clock that is inputted to CLK terminal.
This MCK clock should be connected to the DIR.

In case of digital audio input, the PLL circuit inside the DIR generates LRCK, BCK and MCK clock.
In case of analog audio input, the divider circuit inside the DIR generates LRCK, BCK and MCK clock from the DSP MCK clock.
The DIR automatically selects clock sources (PLL or Divider) by detection of digital input.

4. Master/Slave Mode

The definition and the usage of Master/Slave mode are described in this section.

4.1 Master/Slave Mode Definition

The definition of Master mode DSP is as follows. The Master mode DSP supplies peripheral ICs with MCK, LRCK and BCK clock. The peripheral ICs process the signal synchronizing with the MCK, LRCK and BCK clock. In the above state, the DSP operates as Master mode.

The definition of Slave mode DSP is as follows. The Slave mode DSP receives LRCK and BCK clock from the *external peripheral ICs. The DSP processes the signal synchronizing with the external LRCK and BCK clock. In the above state, the DSP operates as Slave mode.
Note: External peripheral ICs denotes DIR or ADC with Master mode.

4.2 Digital audio clock

The digital audio clocks (LRCK, BCK, MCK) are described in this section. These three terminals can be set input or output. The input/output settings of these three terminals are decided by the next two parameters, SLAVEb termination and DSP-mode setting (Master or Slave) by the command.
The Table 2 shows the operation of LRCK, BCK and MCK clock.

1) In case of “SLAVEb=High”
In DSP Master-mode (command setting), the LR, BCK and MCK terminals are outputs.
In DSP Slave-mode (command setting), the LR, BCK terminals are inputs and MCK terminal is output.
Additionally, the default DSP setting (command) is Slave mode. The MCK terminal output is the buffered CLK-terminal clock.

2) In case of “SLAVEb=Low”
The DSP operates in the Slave mode regardless of Master or Slave (command setting). Therefore these LR, BCK and MCK terminals are inputs.
The DSP system clock employs the clock that is the logical addition of CLK and MCK terminals clocks.
One of the terminals should be usually connected to ground.

Terminal setting			DSP mode (Command setting)	Operating mode	Terminal attribute		
					LR	BCK	MCK
15	SLAVEb	H	Master	Master	Output	Output	Output (clock of CLK terminal)
		H	Slave	Slave	Input	Input	Output (clock of CLK terminal)
		L	Master/Slave	Slave	Input	Input	Input (DSP operating CLK)

Table 2. Operation of LR, BCK and MCK

4.3 Master/Slave Mode usages

The usages of Master/Slave Mode are described in this section.

1) In case of digital audio input, the DSP should operate in Slave mode. Refer to the application circuit 1.
2) In case of analog audio input, the DSP should operate in Master mode. Refer to the application circuit 2.
3) In case of digital/analog audio input, the DSP always should operate in Slave mode. Refer to the application circuit 3.

5. DIR MCK Clock

The MCK clock generation of DIR is described in this section.

The DIR extracts MCK clock from digital audio signal and supplies DAC or others with it. In case that the DIR cannot extract MCK clock, ADC or others are supplied with MCK clock by the next methods.

DIR MCK clock generation
1) In case of no digital audio signal, DIR generates MCK, LRCK and BCK clock by the internal oscillator.
2) In case of no digital audio signal, DIR generates MCK, LRCK and BCK clock by the DIR crystal oscillator.
3) In case of no digital audio signal, DIR buffers the externally generated MCK clock and outputs it to the next ICs. In this document, the example circuits adopt this kind of DIR.

Note: In case that DIR is adopted, the DSP should operate in Slave mode. DAC or others are supplied with the DIR MCK clock. Under this condition, the DSP system can process the digital audio signal correctly.

6. ADC/DAC MCK Clock

The set-up of ADC, DAC and Codec are described in this section.

In case of analog audio input, ADC, DAC and Codec should operate in Slave mode. The DSP should operate in Master mode. The DSP supplies ADC and DAC with MCK clock.

In case of using ADC with crystal oscillator or Codec with DIR, the DSP can operate in Slave mode. And ADC or Codec should operate in Master mode.

7. Crystal Oscillation Circuit

The Figure2 shows crystal oscillation circuit. The NJU26124 employs the PLL circuit inside that is tailored to the frequency of 12.288MHz.
The oscillation margin, frequency and application circuit depend on the crystal unit. The detail information of the crystal oscillation circuit should be asked to the crystal maker.

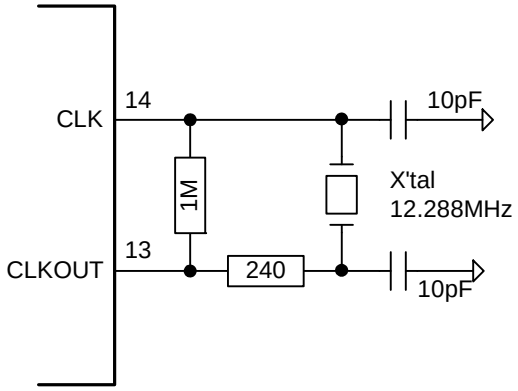

Figure 2. Crystal Oscillation Circuit

8. Reset

Suggestions to design the reset circuit are described in this section.

Suggestions to design reset circuit

1) Reset line should be connected shortly to protect it from the external noise. The next countermeasures are also effective.

- Do not layout the parts and lines that generate noise near the reset line.
- ¦Guard reset line by ground line.
- ¦Current loop space should be minimized as small as possible.

2) In case of long reset line, the next countermeasures are effective.

- Insert a several-tens-ohm resistor in reset line serially.
- Insert a several-kilos-ohm pull-up resistor between the reset terminal and power supply.
- Insert a 10pF up to 100pF capacitor between the reset terminal and ground.

9. Suggestions to design DSP circuit

Suggestions to design the DSP circuit are described in this section.

1) The DSP power supply is 3.3V. The input terminals accept 5V signal under the condition that the 3.3V is supplied to the DSP. The Figure 3 to Figure 6 circuits assumes the ICs that are connected to the DSP employ the 3.3V power supply. So the DSP can connect to the ICs directly.

2) The DSP and other ICs require 0.1uF capacitors, for example ceramic capacitor, between the power supply terminals and ground as bypass capacitors. Also the around 10uF capacitor is required between the DSP power supply and ground.

3) The analog ground and digital ground should be separated to prevent analog signal from digital noise. The analog ground and digital ground should be connected at the adequate point. And the common ground should be connected to frame ground or something.

4) The long digital signal line emits noise and also receives the influence of noise. So MCK, BCKO, LRO, DATA, RESET line should be guarded by ground line to reduce noise problem. The digital signal line should be short and wide to prevent it from noise.

5) The quantity of EMI noise depends on the current loop space of digital signal. So the digital signal line should be short, wide and also guarded by ground.

6) The EMI noise is generated by digital signal in most cases. To reduce the EMI noise, Insert a several-tens-ohm dumping-resistor at a output terminal serially. But the dumping-resistor sometimes affects the output level. So check the specification of the next IC, before inserting it.

Notice: The effects of countermeasures in this document depend on the implementation of the PCB board.

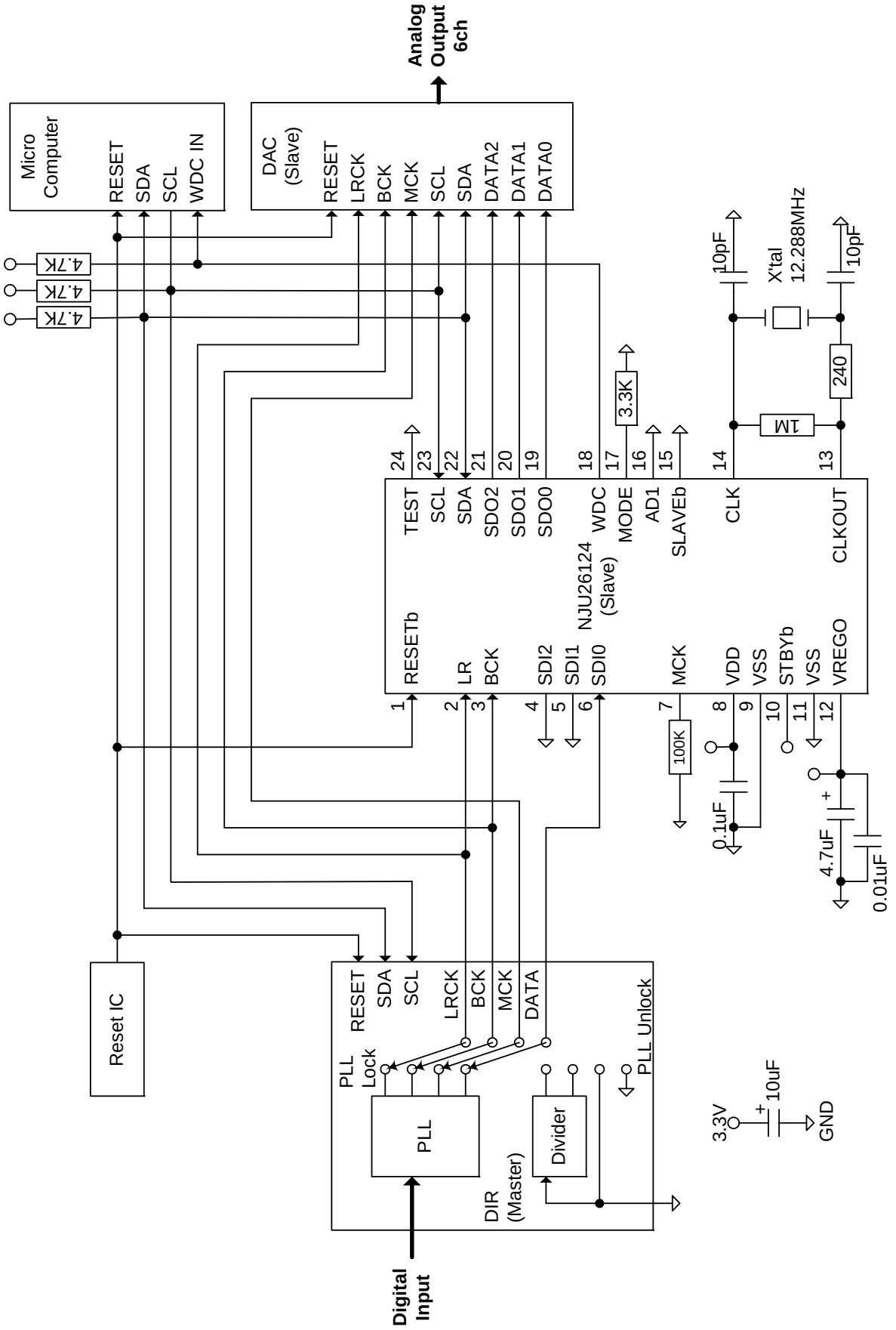

Figure 3. Application circuit 1: NJU26124 with DIR and DAC (I^2C Bus)

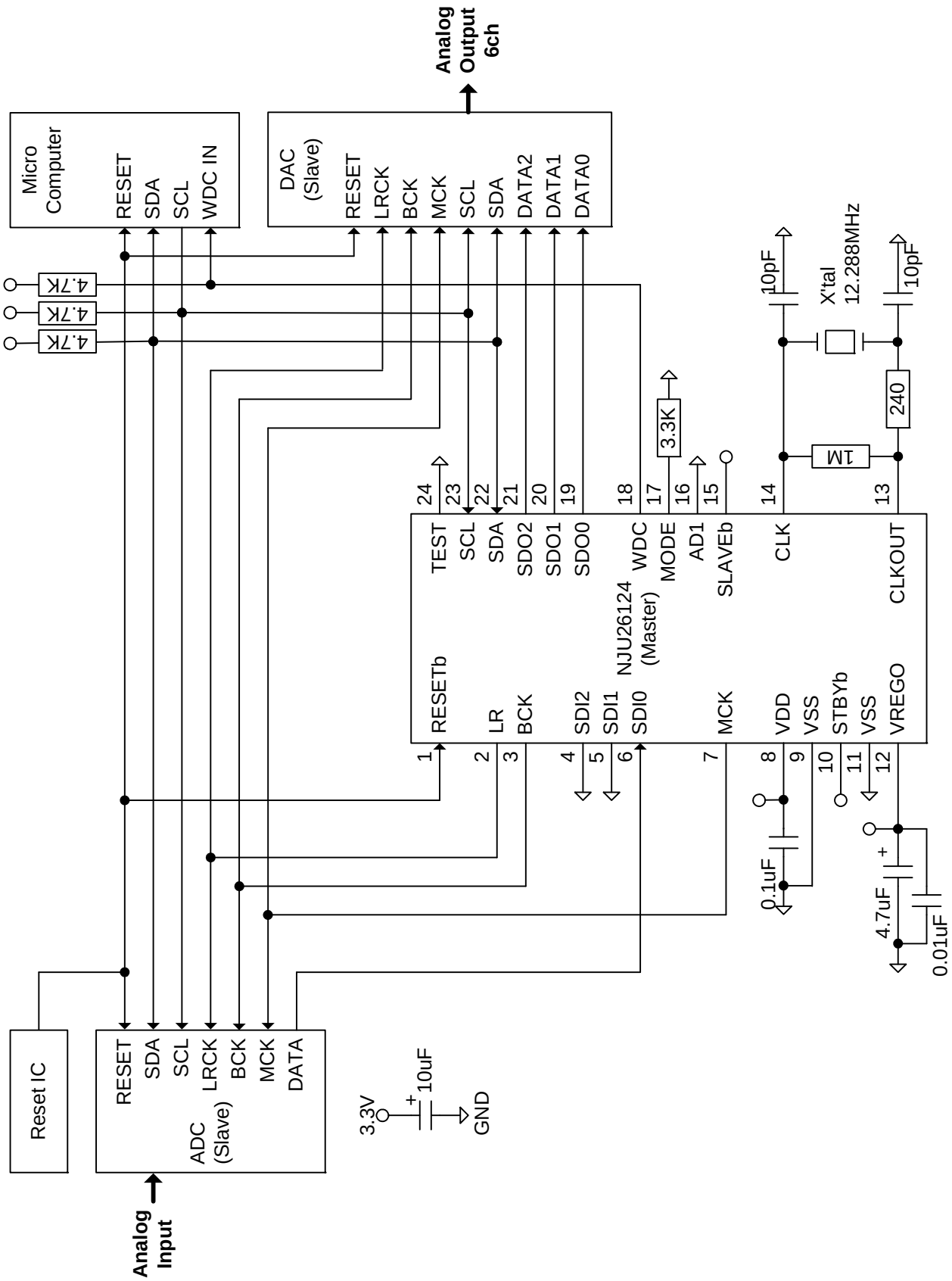

Figure 4. Application circuit 2: NJU26124 with ADC and DAC (I^2C Bus)

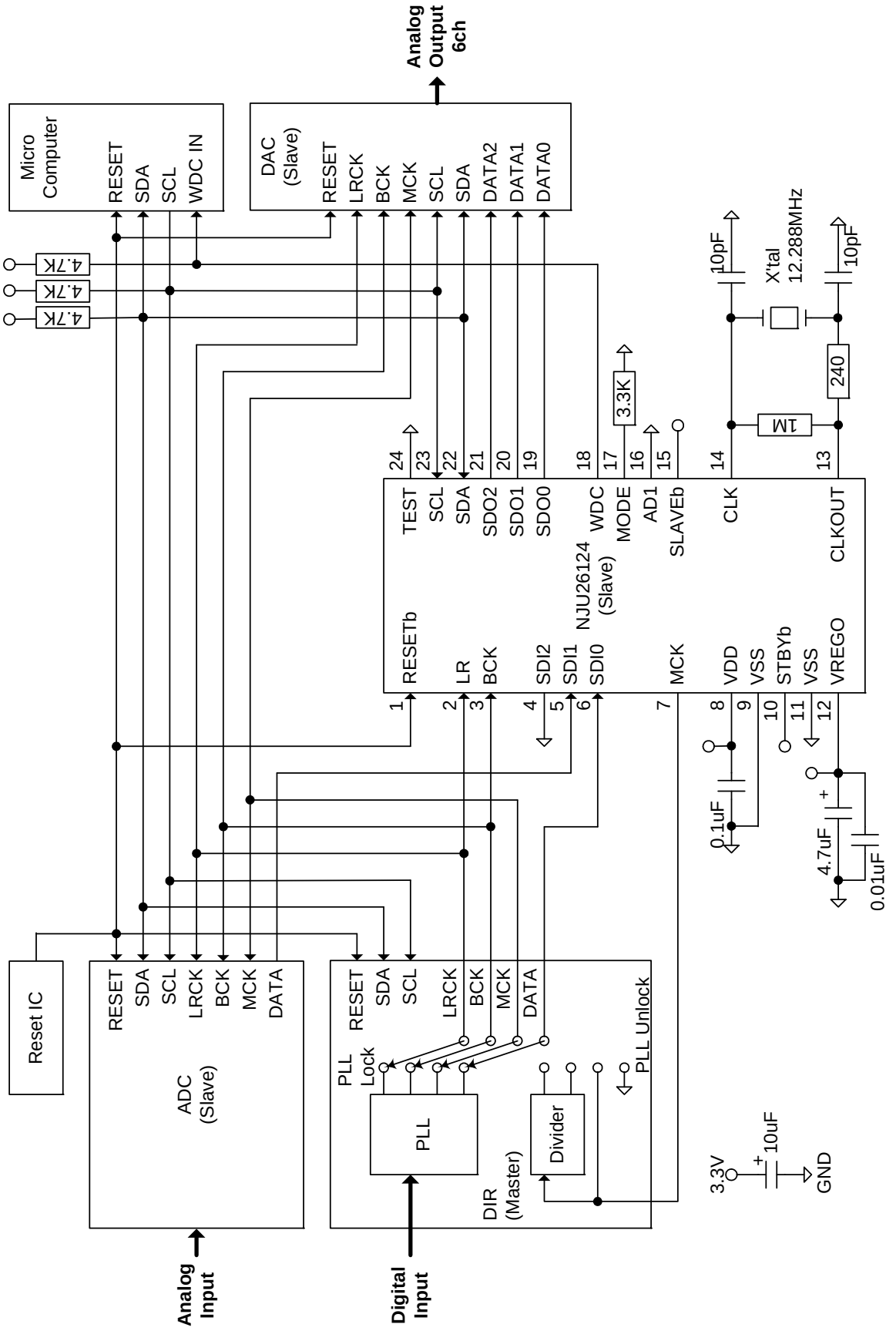

Figure 5.Application circuit 3: NJU26124 with DIR, ADC and DAC (I^2C Bus)