NJU26040 Application Note

Hardware Manual

New Japan Radio Co., Ltd

Version 1.00

CONTENTS

CAUTION

The products specifications and descriptions listed in this application note are subject to change at anytime without notice.

The specifications on this application note are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this application note are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

NJU26040 Application Note
Hardware Manual

1. General Description

This application note describes the NJU26040 hardware applications and usages. The main items described in this document are the next four application circuits, Master/Slave mode, MCK clock, crystal oscillation circuit, reset circuit and the suggestions on the design of the NJU26040 and so on.

1) The NJU26040 application circuit with DIR and DAC (I^2C Bus)
2) The NJU26040 application circuit with ADC and DAC (I^2C Bus)
3) The NJU26040 application circuit with DIR, ADC and DAC (I^2C Bus)
4) The NJU26040 application circuit with DIR, ADC and DAC (4-wire Serial Bus)

2. NJU26040 Block Diagram

The NJU26040 block diagram is shown in the Figure 1.

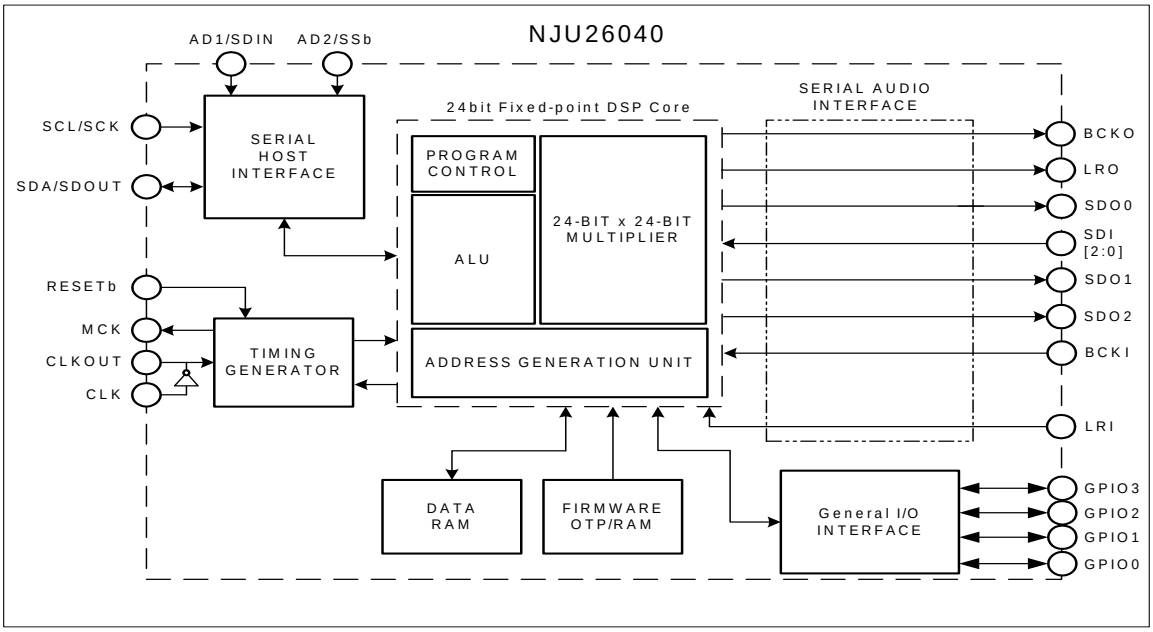

Figure 1. NJU26040 Block Diagram

Note1: The NJU26040 provides three digital audio inputs and three digital audio output. The application circuits do not use all inputs and outputs. The input and output circuits should be modified according to the target application.
Note2: Refer to the NJU26040 Data Sheet together with this application note.

3. Application Circuit Examples

The next four application circuits are described in this section.

1) The NJU26040 application circuit with DIR and DAC (I^2C Bus)
2) The NJU26040 application circuit with ADC and DAC (I^2C Bus)
3) The NJU26040 application circuit with DIR, ADC and DAC (I^2C Bus)
4) The NJU26040 application circuit with DIR, ADC and DAC (4-wire Serial Bus)

Note1: DIR: Digital Interface Receiver
ADC: Analog to Digital Converter DAC: Digital to Analog Converter
Note2: DSP denotes the NJU26040 in this document.
Note3: The ADCs and DACs operate in Slave mode in the Figure 3 to Figure 6.
Note4: The DSP command selects Master/Slave mode.

3.1 Application circuit 1 "The NJU26040 application circuit with DIR and DAC (I^2C Bus)"

This application circuit 1 employs the digital audio signal input, for example DIR input.
The Figure 3 shows the circuit with DIR, DSP and DAC. The DSP operates in the Slave mode.
The DIR supplies DAC with MCK clock.

3.2 Application circuit 2 "The NJU26040 application circuit with ADC and DAC (I^2C Bus)"

This application circuit 2 employs the analog audio signal input, for example ADC input.
The Figure 4 shows the circuit with ADC, DSP and DAC. The DSP operates in the Master mode.
The DSP supplies ADC and DAC with MCK clock.

3.3 Application circuit 3 "The NJU26040 application circuit with DIR, ADC and DAC (I^2C Bus)"

This application circuit 3 employs the analog audio signal input, for example ADC input, and digital audio signal input, for example DIR input.
The Figure 5 shows the circuit with DIR, ADC, DSP and DAC. The DSP should be set in Master mode in case of analog input. The DSP should be set in Slave mode in case of digital input.

The DSP supplies ADC and DAC with MCK clock in case of analog input. The DIR supplies ADC and DAC with MCK clock in case of digital input.

Note1: In case of digital audio input, DIR, DSP and DAC process the input signal. The DSP is set in Slave mode. The DIR supplies DAC with MCK clock. The S1 switch should be selected for DIR mode.
Note2: In case of analog audio input, ADC, DSP and DAC process the input signal. The DSP is set in Master mode. The DSP supplies ADC and DAC with MCK clock. The S1 switch should be selected for DSP mode.

3.4 Application circuit 4 "The NJU26040 application circuit with DIR, ADC and DAC (4-wire Serial Bus)"

This application circuit 4 is the example circuit to control the DSP by the 4-wire serial bus.
The Figure 6 shows the circuit with DIR, ADC, DSP and DAC.
The difference between the application circuit 3 and this application is just using the I^2C Bus or the 4-wire serial bus.

4. Master/Slave Mode

The definition and the usage of Master/Slave mode are described in this section.

4.1 Master/Slave Mode Definition

The definition of Master mode DSP is as follows. The Master mode DSP supplies peripheral ICs with MCK, LRCK and BCK clock. The peripheral ICs process the signal synchronizing with the MCK, LRCK and BCK clock. In the above state, the DSP operates as Master mode.

The definition of Slave mode DSP is as follows. The Slave mode DSP receives LRCK and BCK clock from the *external peripheral ICs. The DSP processes the signal synchronizing with the external LRCK and BCK clock. In the above state, the DSP operates as Slave mode.
Note: External peripheral ICs denotes DIR or ADC with Master mode.

4.2 DSP MCK Clock

The usages of MCK clock in Mater/Slave mode are described in this section.
After the power-on initialization, the MCK terminal outputs the following clock in Slave and Master mode. The command can select three kinds of the MCK output frequency, 256fs(divided by three), 384fs(divided by two), 768fs(original OSC frequency) or suspend. The Table 1 shows MCK output frequencies.

DSP mode	Fs related frequency (MCK Output)	MCK Output Frequency		
		CLK=24.576MHz	CLK=33.8688MHz	CLK=36.864MHz
Master/Slave	256fs (Divided by three): default	8.192MHz	11.2896MHz	12.288MHz
	384fs (Divided by two)	12.288MHz	16.9344MHz	18.432MHz
	768fs (Original OSC Frequency)	24.576MHz	33.8688MHz	36.864MHz
	Suspend	Output is fixed at “low level”		

Table 1. MCK Output Frequency

4.3 Master/Slave Mode usages

The usages of Master/Slave Mode are described in this section.

1) In case of digital audio input, the DSP should operate in Slave mode. The DIR should supply DAC with MCK clock. Refer to the application circuit 1.
2) In case of analog audio input, the DSP should operate in Master mode. The DSP should supply ADC and DAC with MCK clock. Refer to the application circuit 2.

5. DIR MCK Clock

The MCK clock generation of DIR is described in this section.
The DIR extracts MCK clock from digital audio signal and supplies DAC or others with it. In case that the DIR cannot extract MCK clock, ADC or others are supplied with MCK clock by the next methods.

DIR MCK clock generation

1) In case of no digital audio signal, DIR generates MCK, LRCK and BCK clock by the internal oscillator. In this document, the example circuits adopt this kind of DIR.

2) In case of no digital audio signal, DIR generates MCK, LRCK and BCK clock by the DIR crystal oscillator.

3) In case of no digital audio signal, DIR buffers the externally generated MCK clock and outputs it to the next ICs.

Note: In case that DIR is adopted, the DSP should operate in Slave mode. DAC or others are supplied with the DIR MCK clock. Under this condition, the DSP system can process the digital audio signal correctly.

6. ADC/DAC MCK Clock

The set-up of ADC, DAC and Codec are described in this section.

In case of analog audio input, ADC, DAC and Codec should operate in Slave mode. The DSP should operate in Master mode. The DSP supplies ADC and DAC with MCK clock.

In case of using ADC with crystal oscillator or Codec with DIR, the DSP can operate in Slave mode. And ADC or Codec should operate in Master mode.

7. Crystal Oscillation Circuit

The relation between oscillation frequency and oscillation mode is described in this section.

The crystal unit operates in the fundamental wave oscillation mode or overtone oscillation mode. These two oscillation modes are selected by the crystal characteristics or the target frequency. Generally in the frequency 10MHz to 25MHz, the crystal unit operates in the fundamental wave oscillation mode. In the frequency 25MHz to 50MHz, the crystal unit operates in the third overtone oscillation mode.

Note: There are crystals units with the fundamental wave oscillation operate in 36MHz.

The application circuits Figure 3 to Figure 6 employ the third overtone oscillation mode. The application circuit Figure 2 employs the fundamental wave oscillation mode. The Figure 2 oscillation circuit is different from Figure 3 to Figure 6.

The oscillation margin, frequency and application circuit depend on the crystal unit. The detail information of the crystal oscillation circuit should be asked to the crystal maker.

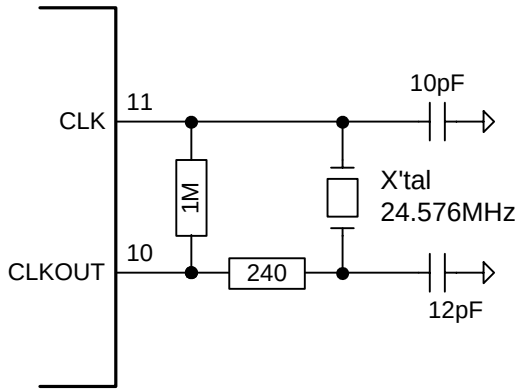

Figure 2. Crystal Oscillation Circuit

8. Reset

Suggestions to design the reset circuit are described in this section.

Suggestions to design reset circuit

1) Reset line should be connected shortly to protect it from the external noise. The next countermeasures are also effective.
   - Do not layout the parts and lines that generate noise near the reset line.
   - Guard reset line by ground line.
   - Current loop space should be minimized as small as possible.

2) In case of long reset line, the next countermeasures are effective.
   - Insert a several-tens-ohm resistor in reset line serially.
   - Insert a several-kilos-ohm pull-up resistor between the reset terminal and power supply.
   - Insert a 10pF up to 100pF capacitor between the reset terminal and ground.

9. Suggestions to design DSP circuit

Suggestions to design the DSP circuit are described in this section.

1) The DSP power supply is 3.3V. If the power is supplied to DSP, input signal 5v is acceptable to the input terminal. The Figure 3 to Figure 6 circuits assumes the ICs that are connected to the DSP employ the power supply 3.3V. So the DSP can connect to the ICs directly.

2) The DSP and other ICs require 0.1uF capacitors, for example ceramic capacitor, between the power supply terminals and ground as bypass capacitors. Also the around 10uF capacitor is required between the DSP power supply and ground.

3) The analog ground and digital ground should be separated to prevent analog signal from digital noise. The analog ground and digital ground should be connected at the adequate point. And the common ground should be connected to frame ground or something.

4) The long digital signal line emits noise and also receives the influence of noise. So MCK, BCKO, LRO, DATA, RESET line should be guarded by ground line to reduce noise problem. The digital signal line should be short and wide to prevent it from noise.

5) The quantity of EMI noise depends on the current loop space of digital signal. So the digital signal line should be short, wide and also guarded by ground.

6) The EMI noise is generated by digital signal in most cases. To reduce the EMI noise, Insert a several-tens-ohm dumping-resistor at a output terminal serially. But the dumping-resistor sometimes affects the output level. So check the specification of the next IC, before inserting it.

Notice: The effects of countermeasures in this document depend on the implementation of the PCB board.

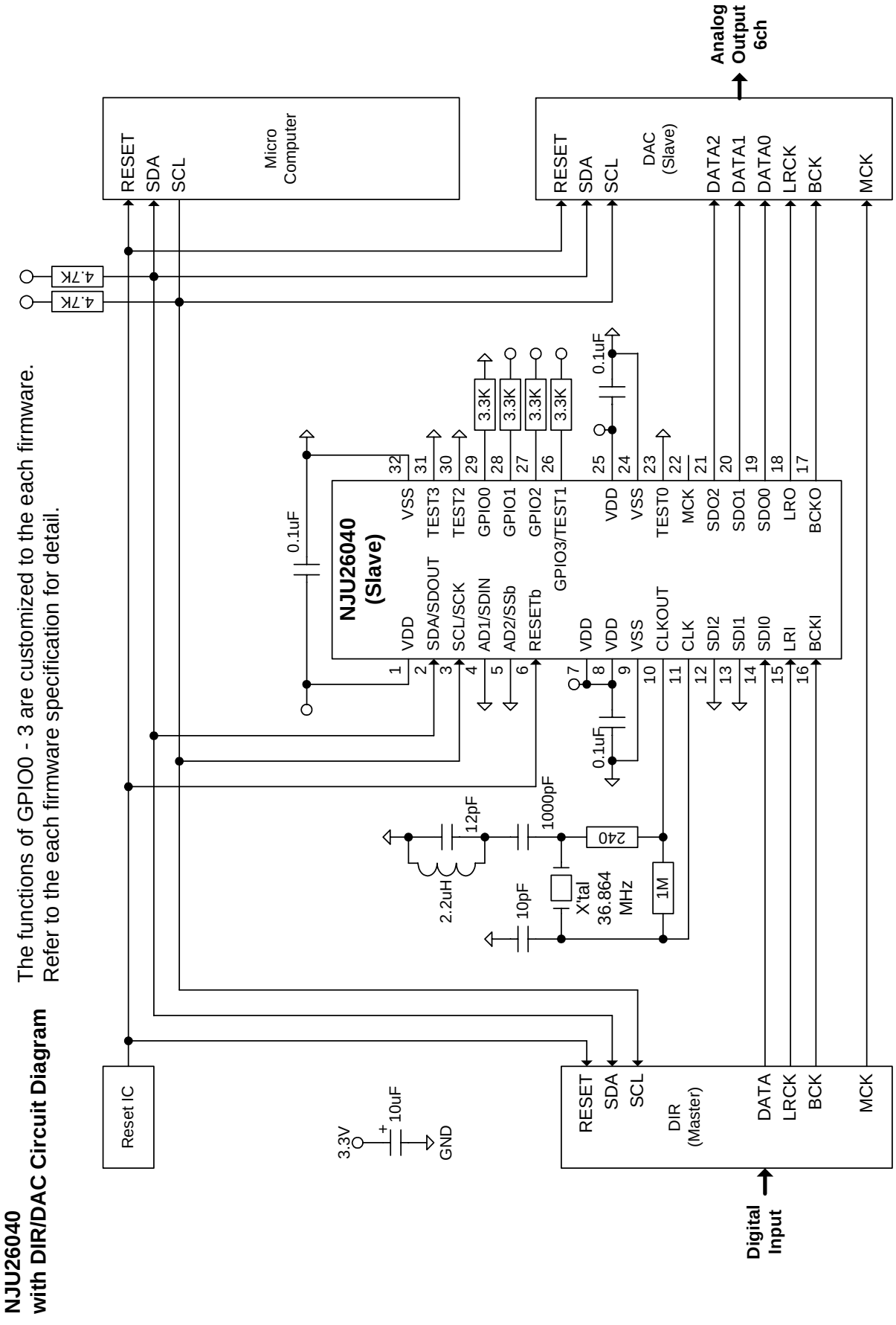

Figure 3. Application circuit 1: NJU26040 with DIR and DAC (I^2C Bus)

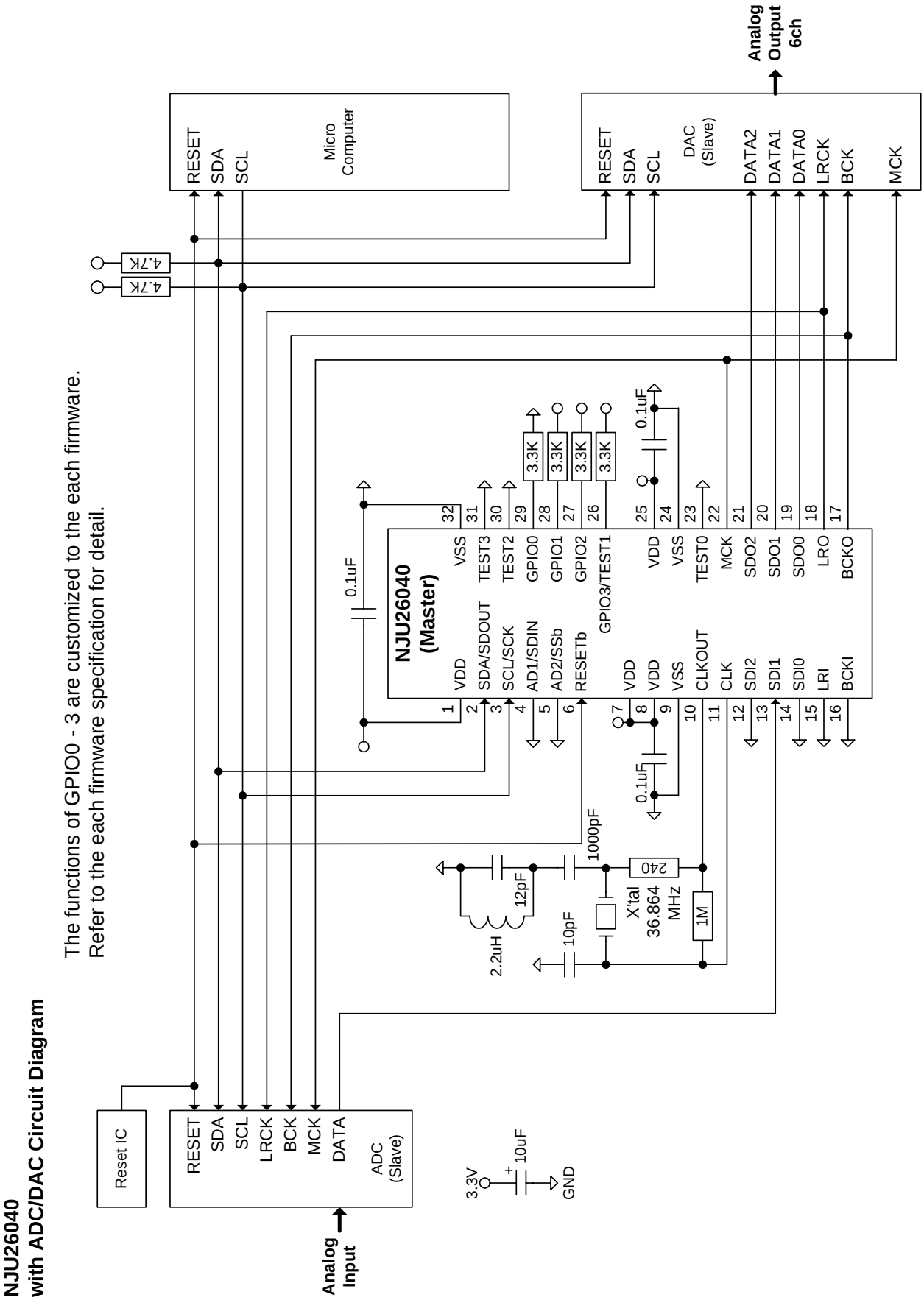

Figure 4. Application circuit 2: NJU26040 with ADC and DAC (I^2C Bus)

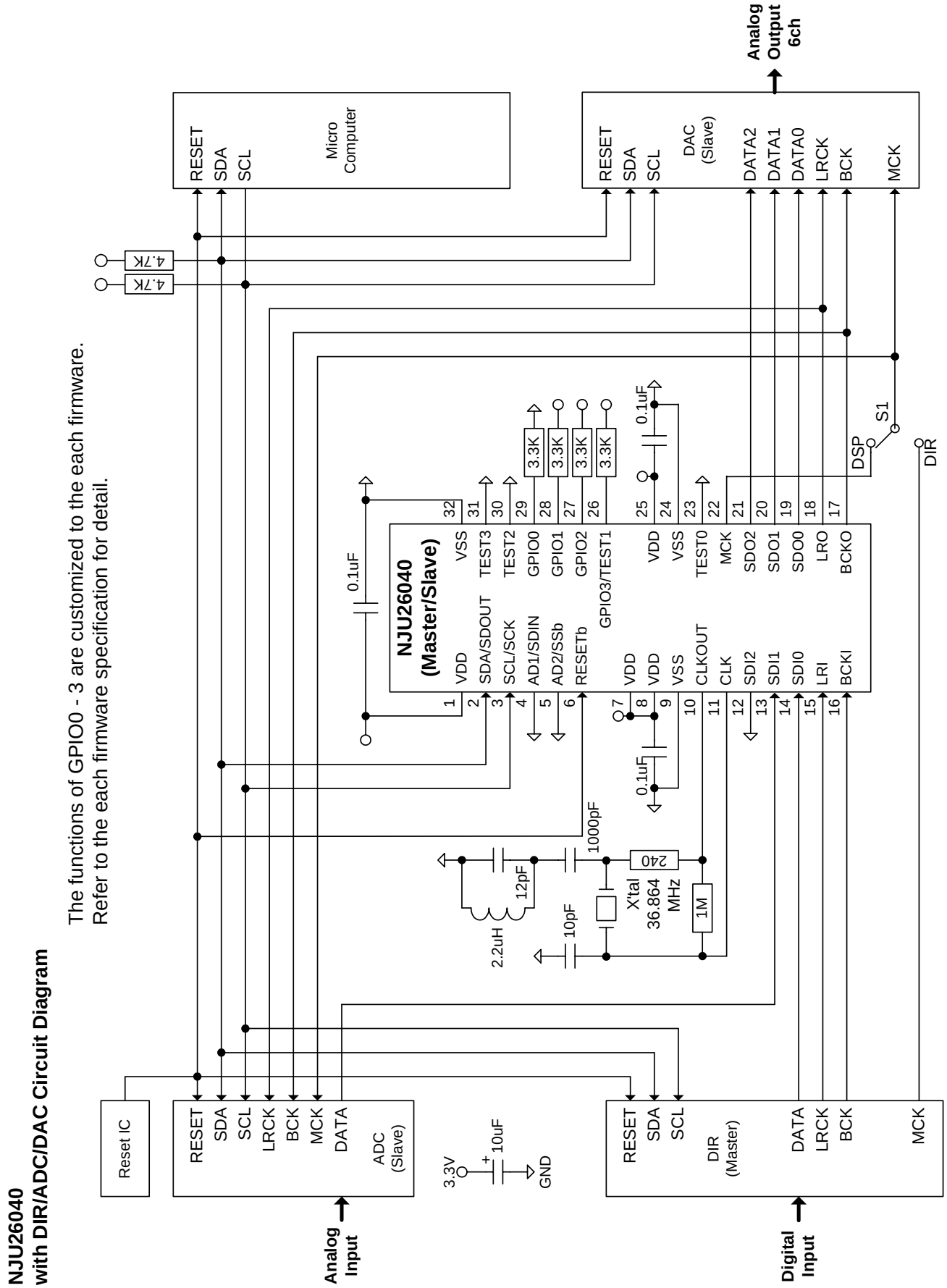

Figure 5.Application circuit 3: NJU26040 with DIR, ADC and DAC (I^2C Bus)

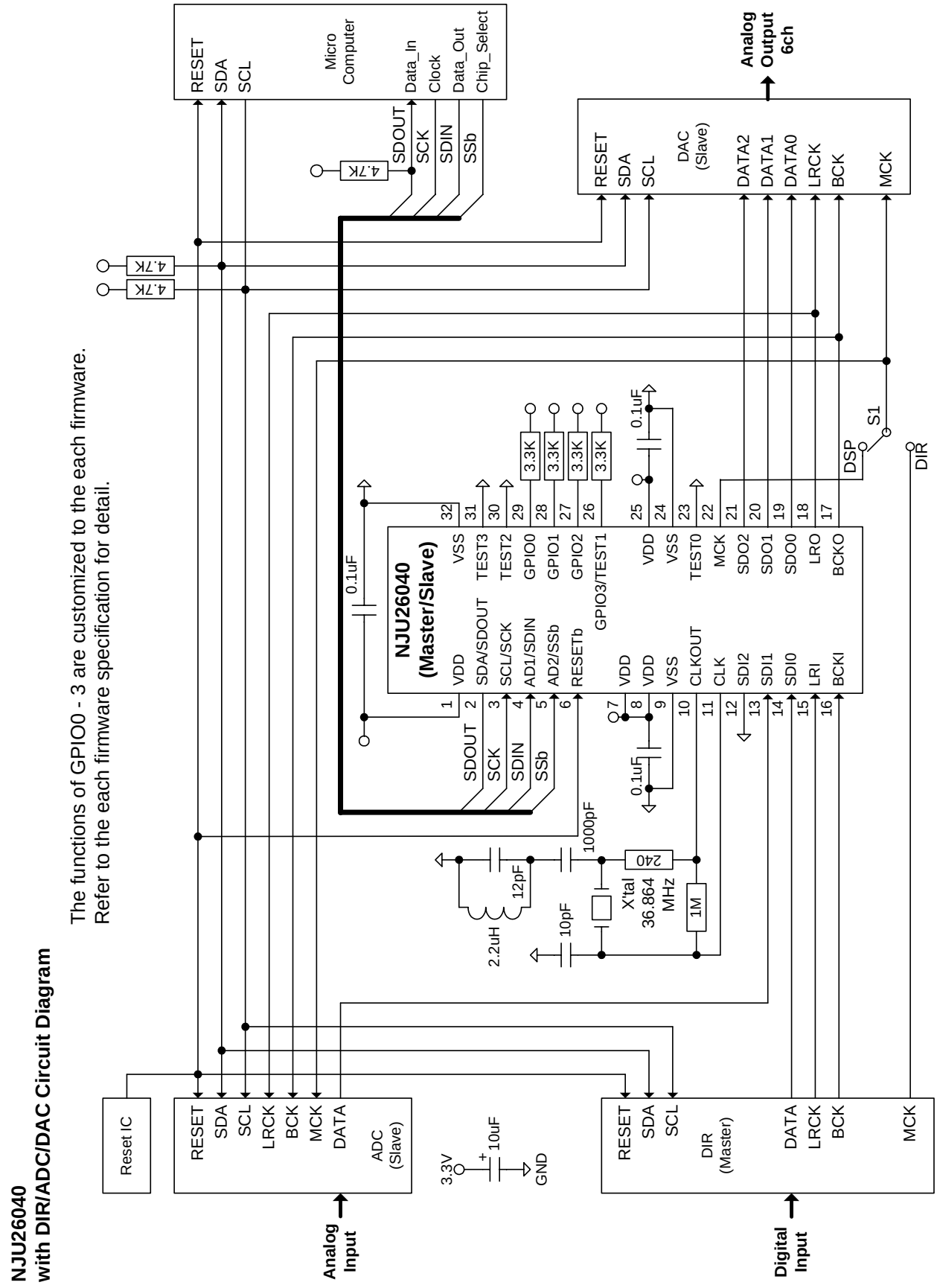

Figure 6.Application circuit 4: NJU26040 with DIR, ADC and DAC (4-wire Serial Bus)