

## Dual Half Bridge Driver

### ■ GENERAL DESCRIPTION

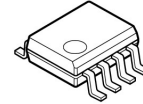
The NJW4810A is a general-purpose dual half bridge driver capable of supplying 1A current. Output duty=100% can be operated by high side P channel MOSFET. It can use as a full bridge driver by connecting VDD1 and VDD2.

The internal gate driver drives high-side/low-side power MOSFET; therefore, it is able to fast switching.

Additionally, it has protection features such as over current protection and thermal shutdown. And in the case of failure, it can output a fault flag.

It is suitable for power switching applications of DSP/micro controller.

### ■ PACKAGE OUTLINE

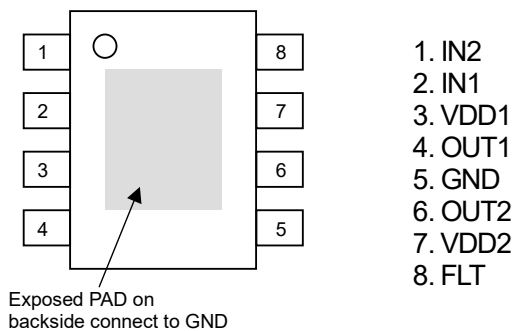


**NJW4810AGM1**

### ■ FEATURES

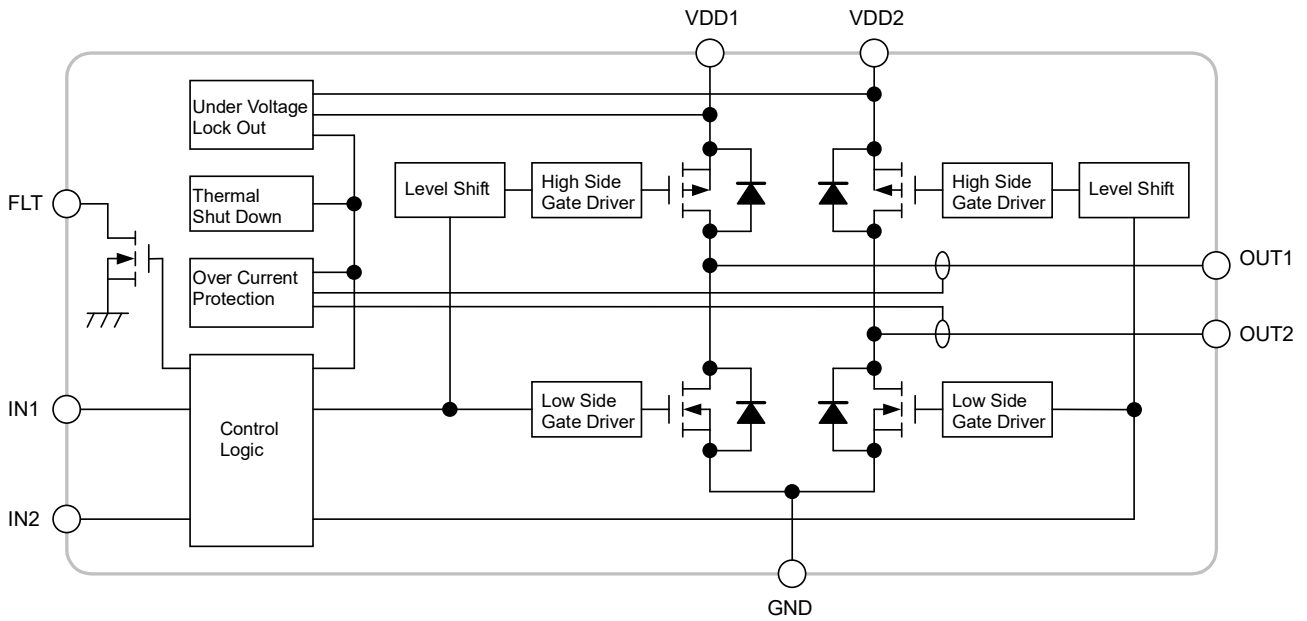
- Output Switch Current     $\pm 1A$
- Operating Voltage        8.0V to 40V
- Thermal Shut Down
- Over Current Protection
- Under Voltage Lockouts
- Fault Indicator Output
- High Heat Radiation Package
- Package Outline         HSOP8

### ■ PIN CONFIGURATION



# NJW4810A

## ■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
Supply Voltage	V <sup>+1</sup> , V <sup>+2</sup>	+45	V	VDD1-GND pin VDD2-GND pin
Input Voltage	V <sub>IN</sub>	-0.3 to +6	V	IN1-GND pin IN2-GND pin
FLT pin Voltage	V <sub>FLT</sub>	-0.3 to +6	V	FLT-GND pin
FLT pin Current	I <sub>FLT</sub>	1	mA	
Power Dissipation	P <sub>D</sub>	0.9 (*1) 3.1 (*2)	W	-
Operating Junction Temperature	T <sub>j</sub>	-40 to +150	°C	-
Operating Temperature Range	T <sub>opr</sub>	-40 to +85	°C	-
Storage Temperature Range	T <sub>stg</sub>	-50 to +150	°C	-

(\*1): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 2Layers)

(\*2): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Voltage	V <sup>+1</sup> V <sup>+2</sup>	8	-	40	V	VDD1-GND pin VDD2-GND pin
Output Switch Current	I <sub>OM</sub>	0	-	1	A	OUT1, OUT2 pin
Input Voltage	V <sub>IN</sub>	0	-	5.5	V	IN1-GND pin, IN2-GND pin
FLT pin Voltage	V <sub>FLT</sub>	0	-	5.5	V	FLT-GND pin

# NJW4810A

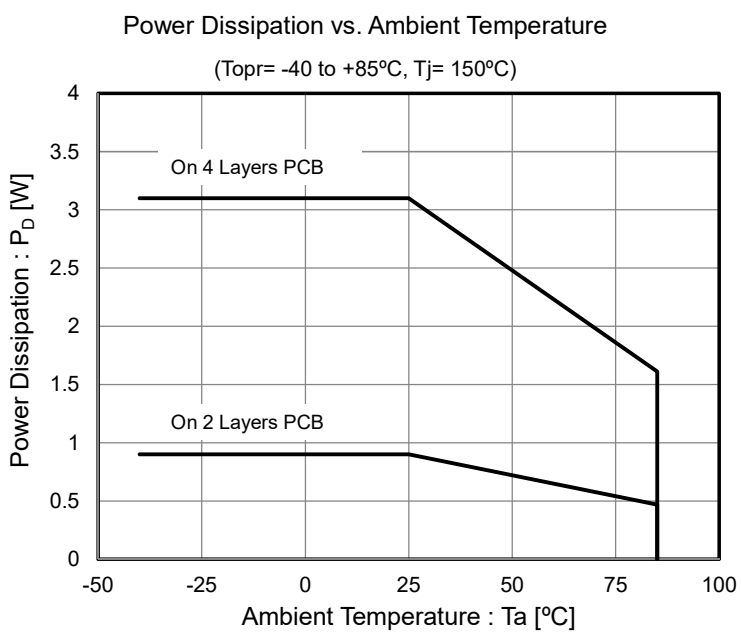
## ■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-Ambient Temperature	$\theta_{ja}$	139 (*1)	°C/W
		40 (*2)	
Junction-to-Case	$\psi_{jt}$	19 (*1)	°C/W
		3.7 (*2)	

(\*1): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 2Layers)

(\*2): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)



## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+1=V^+2=12V$ ,  $T_a=25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
General Characteristics							
Quiescent Current 1 (Operating)	$I_{Q1}$	$V_{IN1}=V_{IN2}=0V$	$V^+1$	–	0.9	1.7	mA
			$V^+2$	–	0.3	0.8	
Quiescent Current 2 (Switching)	$I_{Q2}$	$V_{IN1}=V_{IN2}=0V$ to $3V$ , $f_{IN1}=f_{IN2}=750kHz$ antiphase 50% Duty Cycle	$V^+1$	–	3.7	5.5	mA
			$V^+2$	–	3.2	5.0	

### Output Block

High-side SW ON Resistance	$R_{DSH}$	$I_{OSOURCE}=600mA$	–	1.0	1.8	$\Omega$
Low-side SW ON Resistance	$R_{DSL}$	$I_{OSINK}=600mA$	–	0.75	1.3	$\Omega$
Over Current Limit (*3)	$I_{LIMIT}$	High-side and Low-side	1	2	3	A
Over Current Limit Protection Time (*3)	$t_{OCP}$	High-side and Low-side $R_{FLT}=47k\Omega$ , $V_{FLT}=5V$	15	30	80	ms
Output Rise Time	$t_r$	$V_{IN1}=V_{IN2}=0$ to $3V$	–	3	–	ns
Output Fall Time	$t_f$	$V_{IN1}=V_{IN2}=3$ to $0V$	–	5	–	ns
Dead Time	$Dt$	$V_{IN1}=V_{IN2}=0$ to $3V$	–	50	–	ns
Output Rise Delay Time	$t_{d\_ON}$	$V_{IN1}=V_{IN2}=0$ to $3V$	–	120	–	ns
Output Fall Delay Time	$t_{d\_OFF}$	$V_{IN1}=V_{IN2}=3$ to $0V$	–	120	–	ns
High-side SW Leak Current at OFF state	$I_{OLEAKOUTH}$	$V^+1=V^+2=5.5V$ , $V_{OUT1}=V_{OUT2}=0V$	–	–	1	$\mu A$
Low-side SW Leak Current at OFF state	$I_{OLEAKOUTL}$	$V^+1=V^+2=5.5V$ , $V_{OUT1}=V_{OUT2}=5.5V$	–	–	1	$\mu A$
OUT pin – VDD pin Potential Difference	$V_{PDOV}$	$I_{ORH}=1A$ , $V^+1=V^+2=5.5V$	–	0.9	1.5	V
GND pin – OUT pin Potential Difference	$V_{PDGO}$	$I_{ORL}=1A$ , $V^+1=V^+2=5.5V$	–	0.9	1.5	V

(\*3): The overcurrent detection time may take  $1\mu s$  (max). During this time overcurrent protection circuit does not detect an overcurrent. Therefore, you should control the pulse width and frequency of IN1/IN2 pin to prevent a continuous over-current in short-term.

### Input Circuit Block

Input pin High Voltage	$V_{IHIN}$		2.0	–	5.5	V
Input pin Low Voltage	$V_{ILIN}$		0	–	0.8	V
Input pin sink current	$I_{IIN}$	$V_{IN1}=V_{IN2}=5.5V$	–	0.01	1	$\mu A$

### Under Voltage Lockout (UVLO) Block

UVLO Release Voltage (*4)	$V_{UVLO2}$	$V^+1=V^+2=L \rightarrow H$	6.3	7.0	7.7	V
UVLO Operation Voltage (*4)	$V_{UVLO1}$	$V^+1=V^+2=H \rightarrow L$	6.0	6.7	7.4	V
UVLO Hysteresis Voltage	$\Delta V_{UVLO}$	$V_{UVLO2}-V_{UVLO1}$	–	0.3	–	V

(\*4): UVLO operates at each line ( $V^+1$  and  $V^+2$ )

### Fault Function (FLT pin)

Low Level Output Voltage	$V_{LFLT}$	$I_{FLT}=500\mu A$	–	0.25	0.5	V
OFF Leak Current	$I_{OLEAKFLT}$	$V^+1=V^+2=5.5V$ , $V_{FLT}=5.5V$	–	–	1	$\mu A$

# NJW4810A

## ■ PIN OPERATION TABLE

INPUT			OUTPUT					Mode
IN1	IN2	VDD1, VDD2	FLT	OUT1 High-side SW	OUT1 Low-side SW	OUT2 High-side SW	OUT2 Low-side SW	
L	L	$V^{+1}$ and $V^{+2} \geq V_{UVLO2}$	ON	OFF	ON	OFF	ON	Normal
L	H	$V^{+1}$ and $V^{+2} \geq V_{UVLO2}$	ON	OFF	ON	ON	OFF	Normal
H	L	$V^{+1}$ and $V^{+2} \geq V_{UVLO2}$	ON	ON	OFF	OFF	ON	Normal
H	H	$V^{+1}$ and $V^{+2} \geq V_{UVLO2}$	ON	ON	OFF	ON	OFF	Normal
—	—	$V^{+1}$ or $V^{+2} < V_{UVLO1}$	OFF	OFF	OFF	OFF	OFF	UVLO

INPUT			OUTPUT					Mode
Tj	I <sub>OUT1</sub>	I <sub>OUT2</sub>	FLT	OUT1 High-side SW	OUT1 Low-side SW	OUT2 High-side SW	OUT2 Low-side SW	
Tj > 150°C	—	—	OFF	OFF	OFF	OFF	OFF	TSD (*5)
—	I <sub>OUT1</sub> ≥ I <sub>LIMIT</sub>	—	OFF	OFF	OFF	OFF	OFF	OCP (*6)
—	—	I <sub>OUT2</sub> ≥ I <sub>LIMIT</sub>	OFF	OFF	OFF	OFF	OFF	OCP (*6)

(\*5): After the TSD function operation, when the junction temperature becomes less than 125°C, NJW4810A returns to normal mode.

(\*6): NJW4810A returns to normal mode after the elapse of a certain period of time after the OCP function operating.

■ TIMING CHART

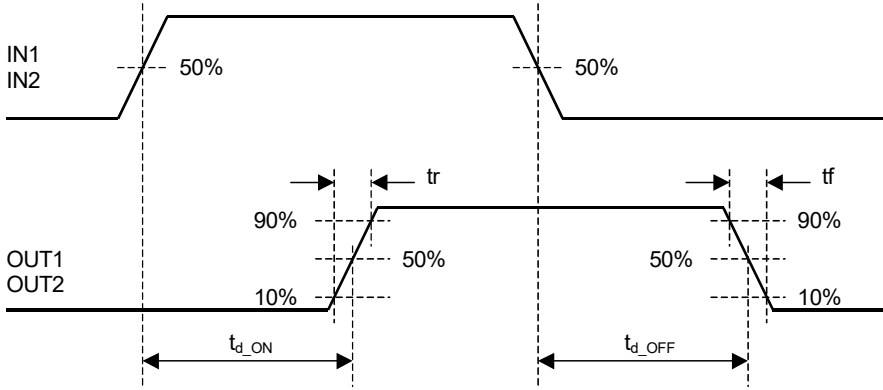


Fig1. Output Rise/Fall Time, PWM Rise/Fall Delay Time

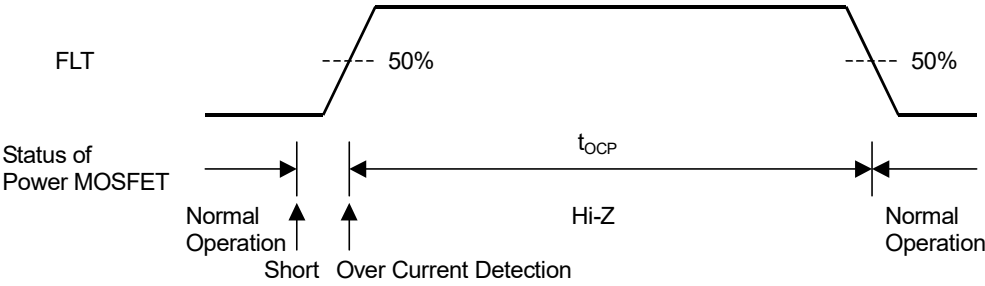


Fig2. Over Current Limit Protection Time

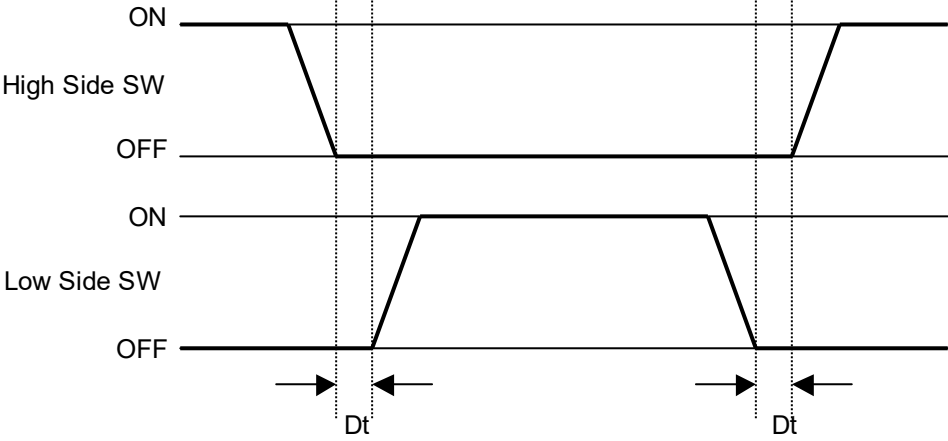
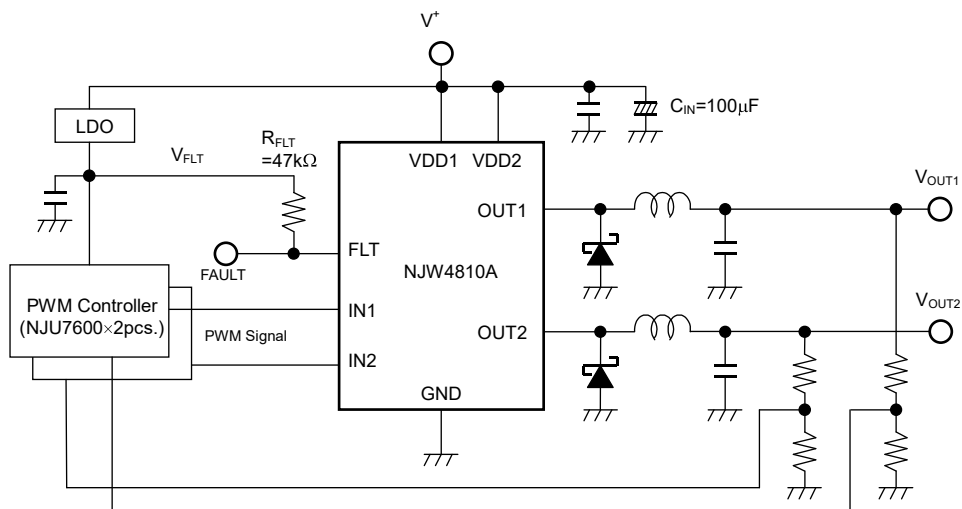


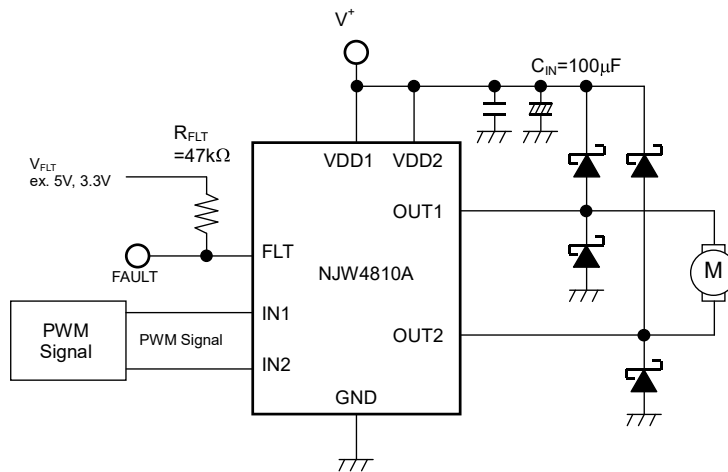
Fig3. SW Operation and Dead Time

# NJW4810A

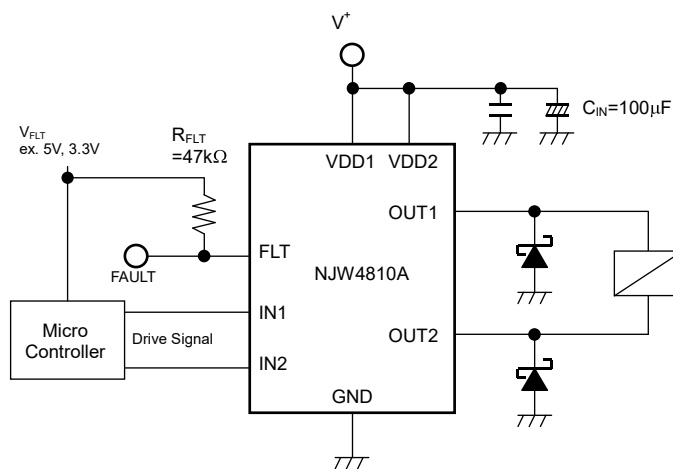
## ■ TYPICAL APPLICATIONS



2ch Synchronous PWM step down switching regulator



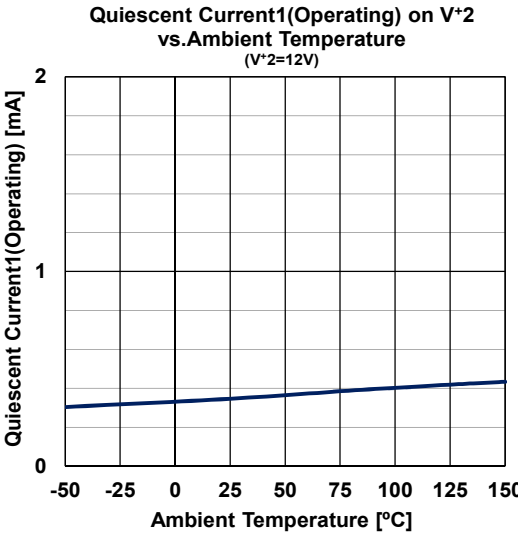
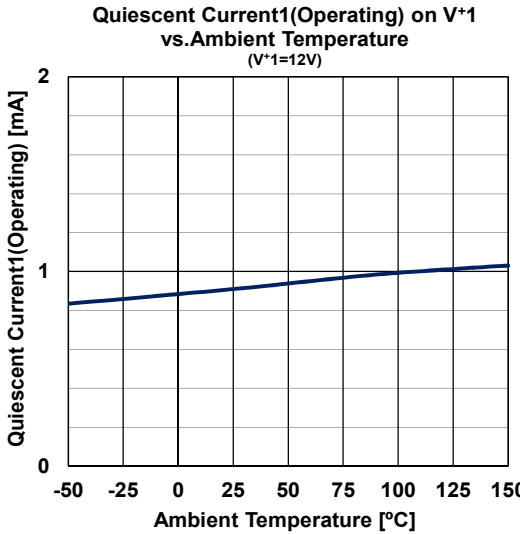
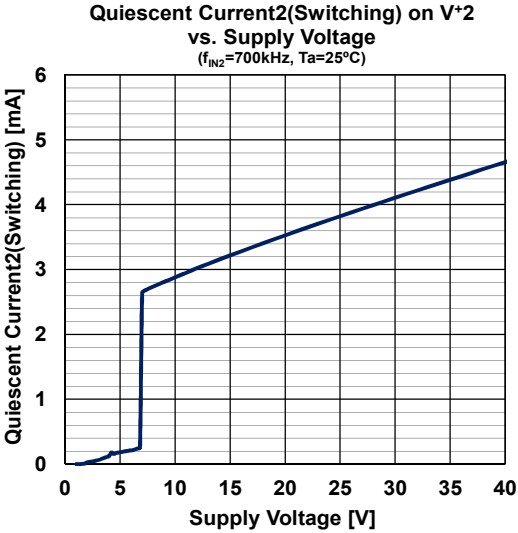
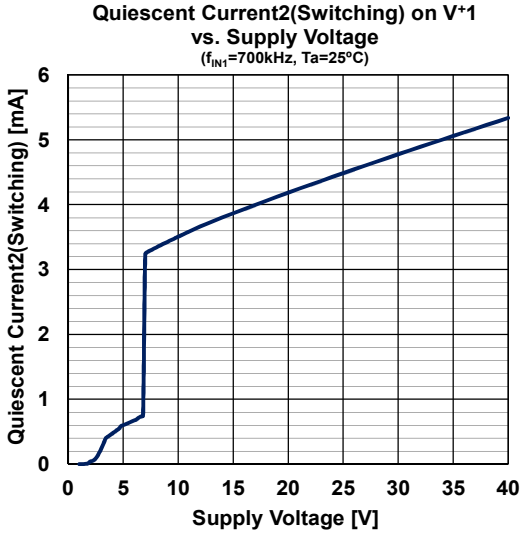
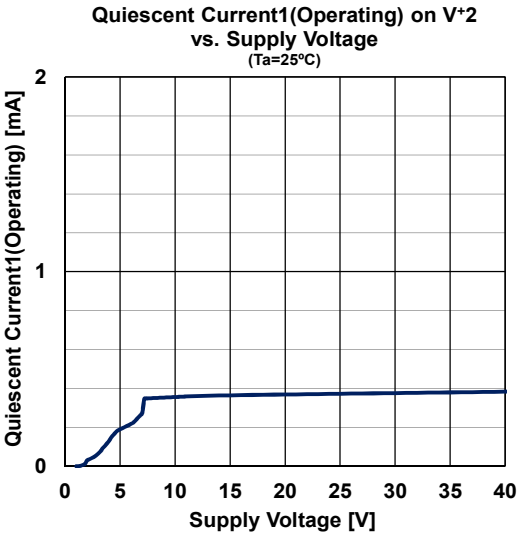
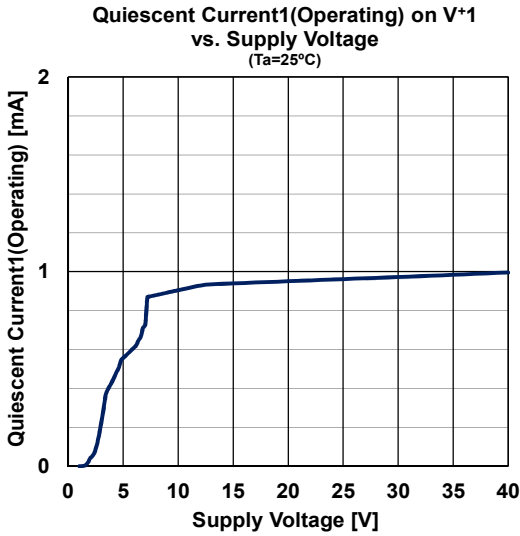
Full bridge motor driver



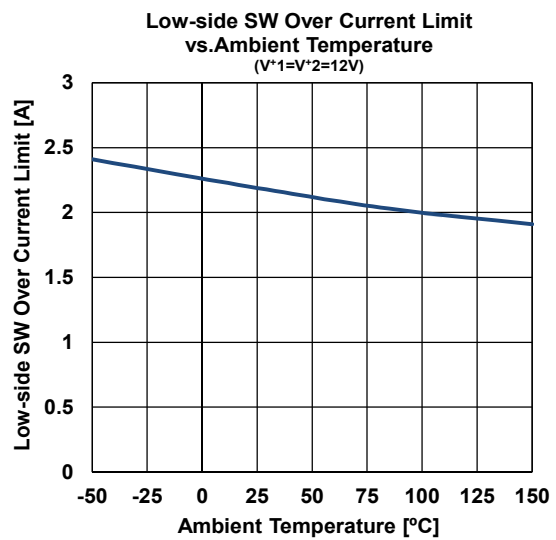
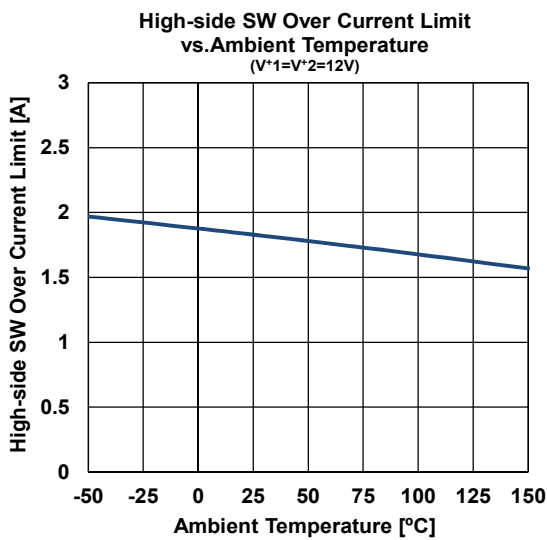
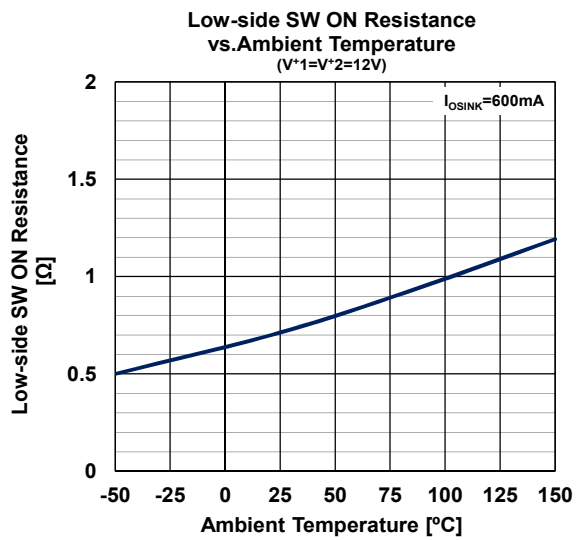
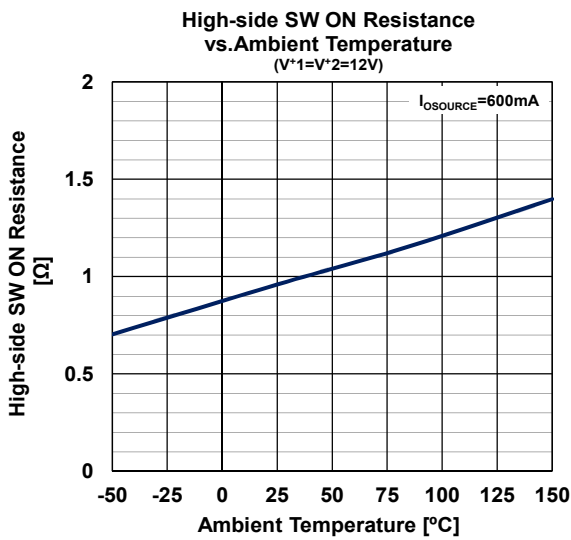
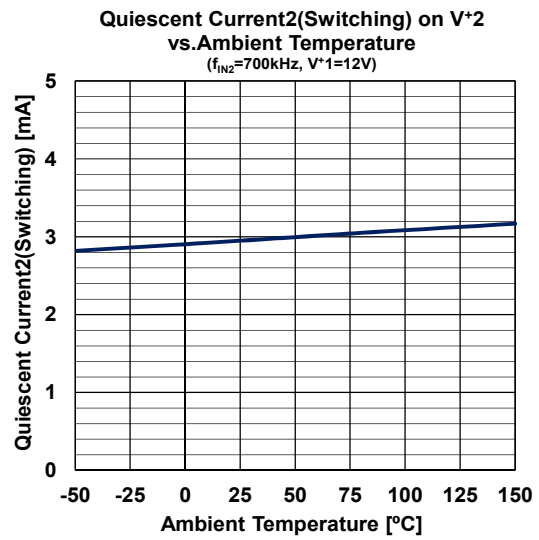
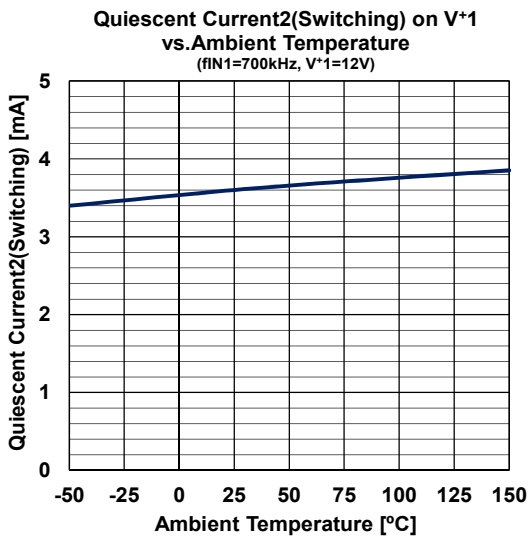
Latch type solenoid driver



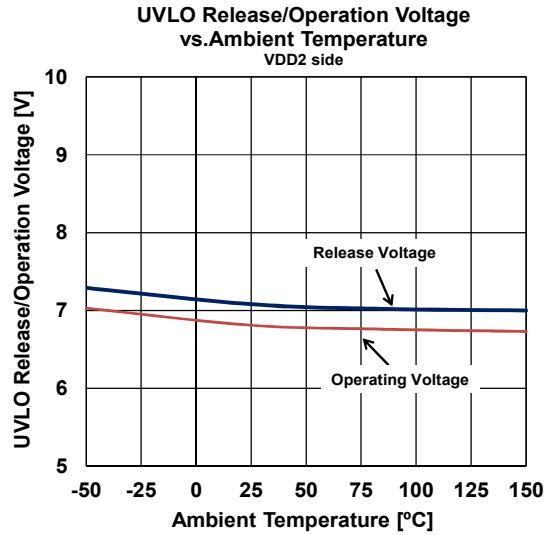
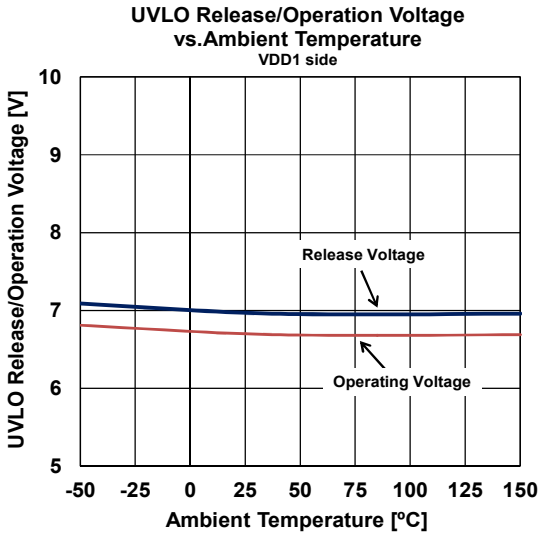
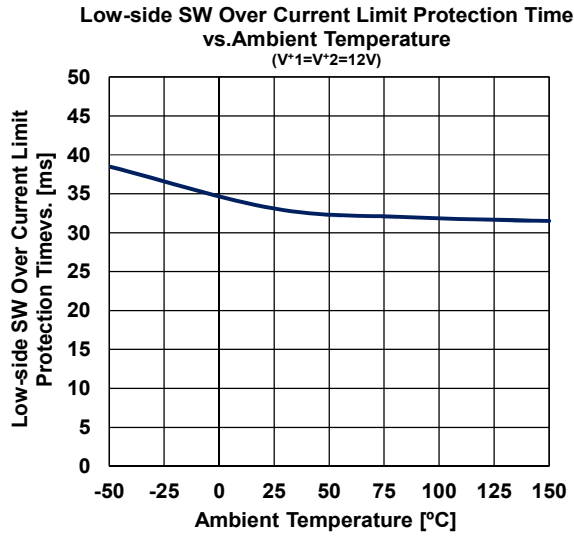
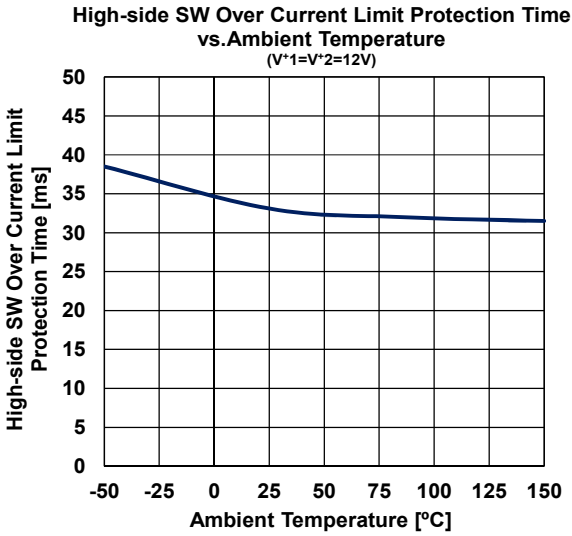
■ TYPICAL CHARACTERISTICS



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■ TYPICAL CHARACTERISTICS



## MEMO

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