

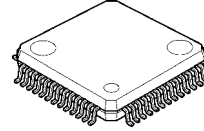
## Multi Input Wide Band Video Interface with I<sup>2</sup>C Control

### ■ GENERAL DESCRIPTION

**NJW1329** is a multi input wide band video interface IC with I<sup>2</sup>C control. Also the **NJW1329** includes 7-input 2 channel video switch for CVBS, 3-input 1 channel video switch for Component Video Signal, 2 channel 75-ohm driver for CVBS and 1 channel 75-ohm driver for Component Video Signal.

**NJW1329** is suitable for video equipment that has multi input and multi output.

### ■ PACKAGE OUTLINE

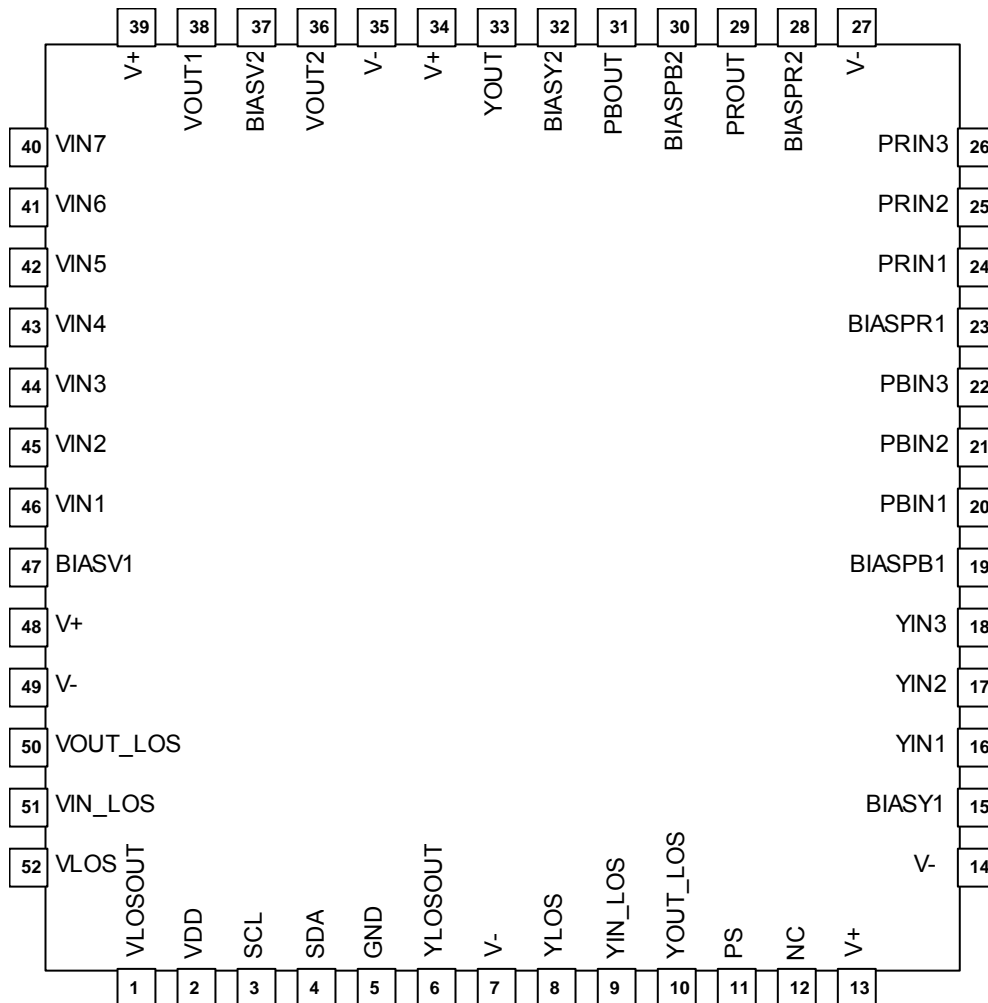


**NJW1329FH3**

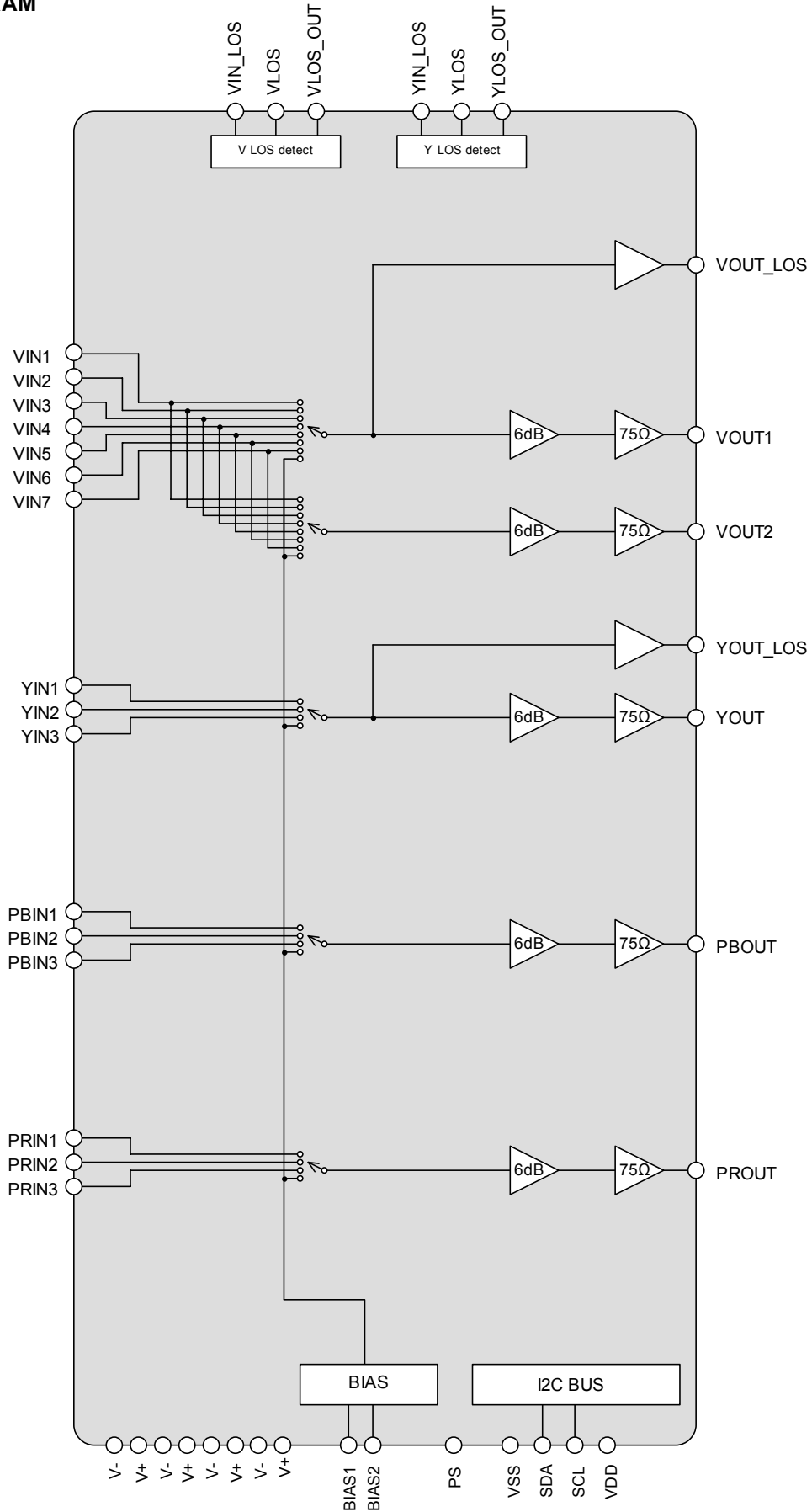
### ■ FEATURES

- Operating Voltage Dual Supply V+ +3.0 to +3.45V, V- -3.0 to -5.5V
- 7-input 2 channel video switch for CVBS
- 3-input 1 channel video switch for Component Video Signal
- 2 channel 75-ohm driver for CVBS
- 1 channel 75-ohm driver for Component Video Signal
- 1 channel LOS (Loss Of Signal) detector for each CVBS and Component Video Signal
- I<sup>2</sup>C BUS control
- LQFP52-H3

### ■ PIN CONFIGURATION



## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	3.5	V
Supply Voltage	V <sup>-</sup>	-6.0	V
Power Dissipation	Pd	1800 <sup>NOTE)</sup>	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstr	-40 to +125	°C

(Note) At on a board of EIA/JDAC specification. ( 114.3 x 76.2 x 1.6mm Two layers,FR-4)

## ■ RECOMMEND OPERATING VOLTAGE

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage 1	Vopr1	V <sup>+</sup> - GND	3.0	3.3	3.45	V
Operating Voltage 2	Vopr2	V <sup>-</sup> - GND	-5.5	-3.3	-3.0	V

## ■ ELECTRICAL CHARACTERISTICS

### ● Power Supply Characteristics

(TEST CONDITION: Ta=25°C, V<sup>+</sup> = 3.3V, VDD= 0V, V<sup>-</sup> = -5.0V VSS= -5.0V all controls unless otherwise specified)

### ● DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current1	I <sub>CC</sub>	V <sup>+</sup> , No Signal	-	45	70	mA
Operating Current2	I <sub>EE</sub>	V <sup>-</sup> , No Signal	-70	-45	-	mA
Operating Current at power save mode 1	Isave1	V <sup>+</sup> , Power Save Mode	-	1.0	4.0	mA
Operating Current at power save mode 2	Isave2	V <sup>-</sup> , Power Save Mode	-4.0	-1.0	-	mA

### ● AC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Output Voltage	V <sub>OM</sub>	Input sine signal voltage (100kHz), THD=1%	3.8	-	-	Vp-p
Voltage Gain	Gv	Input sine signal (100kHz, 1.0Vp-p)	5.5	6.0	6.5	dB
Frequency Characteristic 1	Gf1	Input sine signal (12MHz/100kHz, 1.0Vp-p) V input terminal	-3.0	0.0	-	dB
Frequency Characteristic 2	Gf2	Input sine signal (100MHz/100kHz, 1.0Vp-p) Y/PB/PR input terminal	-	-3.0	-	dB
Frequency Characteristic 3	Gf3	Input sine signal (150MHz/100kHz, 100mVp-p) Y/PB/PR input terminal	-	-3.0	-	dB
Cross Talk between Input terminals	CT	Input sine signal (3.58MHz, 1.0Vp-p)	-	-60	-50	dB
Differential Gain	DG	Input Video signal (1.0Vp-p, 10step)	-	0.5	-	%
Differential Phase	DP	Input Video signal (1.0Vp-p, 10step)	-	0.5	-	deg
Signal Detective Voltage	Vdet	Input Square pulse (16kHz, 4.7μs)	-	200	-	mVp-p
Output/output voltage difference on mute mode	dVDo	On mute mode	-0.4	-	0.4	V
S/N ratio	SNv	Input White Video signal (1.0Vp-p, 100%) for V/Y/PB/PR input terminal	-	75	-	dB

## ● AC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Switch Change Over Voltage (H level)	VthH		2.0	-	V <sup>+</sup>	V
Switch Change Over Voltage (L level)	VthL		0	-	1.0	V
Maximum inflow current on Switch ON	IthH	V=3.3V	-	-	120	uA
Maximum inflow current on Switch OFF	IthL	V=0.3V	-	-	8	uA

## ■ POWER SAVE CONTROL

NJW1329 performs Power Save mode with PS terminal.

PS TERMINAL VOLTAGE	OPERATION
<VthL	Power Save Mode, enable I2C control for Power Save
>VthH	Normal Mode, disenable I2C control for Power Save

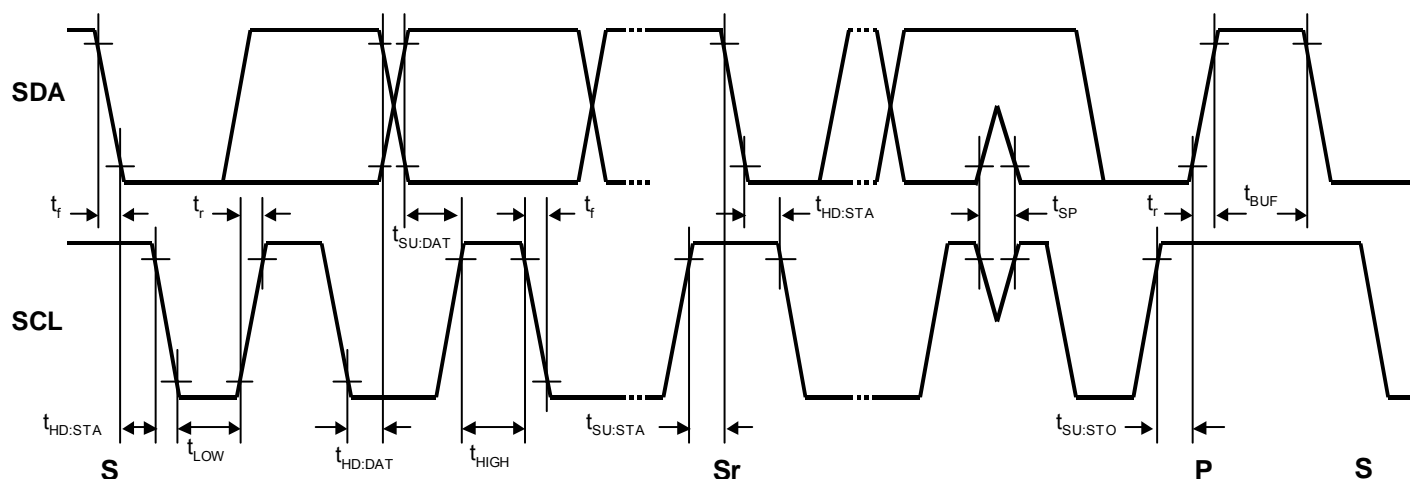
## ■ SIGNAL DETECTION

NJW1329 detects a signal that is larger than Signal Detective Voltage (SDV).

INPUT SIGNAL VOLTAGE	LOS_OUT	CONDITION
Vdet > V <sub>IN</sub>	H	Signal is smaller than SDV
Vdet < V <sub>IN</sub>	L	Signal is larger than SDV

NOTE) If you input a signal except for video signal with sync, there is the case that output of LOS\_OUT terminal is not stable.

## ■ TIMING on the I<sup>2</sup>C BUS (SDA, SCL)



## ■ CHARACTERISTICS OF I/O STAGES FOR I<sup>2</sup>C BUS (SDA, SCL)

I<sup>2</sup>C BUS Load Conditions

STANDARD MODE: Pull up resistance 4kΩ (Connected to V<sup>+</sup>), Load capacitance 200pF (Connected to GND)

HIGH-SPEED MODE: Pull up resistance 4kΩ (Connected to V<sup>+</sup>), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	STANDARD MODE			HIGH-SPEED MODE			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V <sub>IL</sub>	0.0	-	0.3V <sup>+</sup>	0.0	-	0.3V <sup>+</sup>	V
High Level Input Voltage	V <sub>IH</sub>	0.7V <sup>+</sup>	-	5.5	0.7V <sup>+</sup>	-	5.5	V
Low Level Output Voltage (3mA at SDA pin)	V <sub>OL</sub>	0	-		0	-	0.4	V
Input current each I/O pin with an input voltage between 0.1V <sup>+</sup> and 0.9V <sup>+</sup>	I <sub>i</sub>	-10	-	10	-10	-	10	μA

## ■ CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I<sup>2</sup>C BUS DEVICES

PARAMETER	SYMBOL	STANDARD MODE			HIGH-SPEED MODE			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	$f_{SCL}$	-	-	100	-	-	400	kHz
HOLD time	$t_{HD:STA}$	4.0	-	-	0.6	-	-	$\mu$ s
Low period of the SCL clock	$t_{LOW}$	4.7	-	-	1.3	-	-	$\mu$ s
High period of the SCL clock	$t_{HIGH}$	4.0	-	-	0.6	-	-	$\mu$ s
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	$\mu$ s
Data Hold Time <sup>NOTE)</sup>	$t_{HD:DAT}$	0	-	-	0	-	-	$\mu$ s
Data set-up Time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	$t_r$	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	$t_f$	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	$\mu$ s
Bus free time between a STOP and START condition	$t_{BUF}$	4.7	-	-	1.3	-	-	$\mu$ s
Capacitive load for each bus line	$C_b$	-	-	400	-	-	400	pF
Noise margin at the Low level	$V_{nL}$	0.5	-	-	0.5	-	-	V
Noise margin at the High level	$V_{nH}$	1	-	-	1	-	-	V

$C_b$  ; total capacitance of one bus line in pF

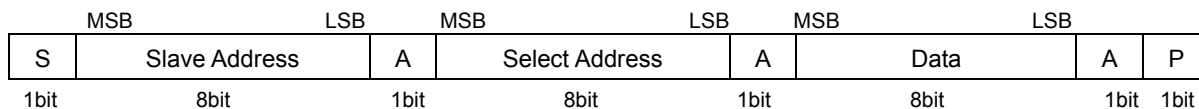
NOTE) Data hold time:  $t_{HD:DAT}$

Please hold the Data Hold Time ( $t_{HD:DAT}$ ) to 300ns or more to avoid status of unstable at SCL falling edge.

## ■ DEFINITION OF I<sup>2</sup>C REGISTER

You can send and transmit address by I<sup>2</sup>C REGISTER with SDA input and SCL input.

### • I<sup>2</sup>C BUS FORMAT



S: Starting term

A: Acknowledge bit

P: Ending term

### • SLAVE ADDRESS

Slave Address								Hex
MSB				LSB				-
1	0	0	1	0	1	1	0	96(h)

NJW1329 is not suitable for read mode.

### • CONTROL REGISTER TABLE

The auto increment function cycles the select address as follows.

00H → 01H → 00H

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOUT1 Select			VOUT2 Select			Power Save	-
01H	YOUT/PBOUT/ PROUT Select		-	-	-	-	-	-

### ■ CONTROL REGISTER INITIAL VALUE

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0

## ■ INSTRUCTION CODE

a)

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOUT1 Select			VOUT2 Select			Power Save	-

### •VOUT1 SIGNAL SELECT TABLE

VOUT1 Select			VOUT1
D7	D6	D5	
0	0	0	Mute*
0	0	1	VIN1
0	1	0	VIN2
0	1	1	VIN3
1	0	0	VIN4
1	0	1	VIN5
1	1	0	VIN6
1	1	1	VIN7

\*Default Value

### •VOUT2 SIGNAL SELECT TABLE

VOUT2 Select			VOUT2
D4	D3	D2	
0	0	0	Mute*
0	0	1	VIN1
0	1	0	VIN2
0	1	1	VIN3
1	0	0	VIN4
1	0	1	VIN5
1	1	0	VIN6
1	1	1	VIN7

\*Default Value

### •POWER SAVE SELECT TABLE

Power Save	Power Save
D1	
0	Power Save Mode*
1	Normal Mode

\*Default Value

Please connect the PS terminal with GND when you control the Power Save with I<sup>2</sup>C.



**■ INSTRUCTION CODE**

b)

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
01H	YOUT/PBOUT/ PROUT Select		-	-	-	-	-	-

**•YOUT/PBOUT/PROUT SIGNAL SELECT TABLE**

YOUT/PBOUT/ PROUT Select		YOUT	PBOUT	PROUT
D7	D6			
0	0	Mute*	Mute*	Mute*
0	1	YIN1	PBIN1	PRIN1
1	0	YIN2	PBIN2	PRIN2
1	1	YIN3	PBIN3	PRIN3

\*Default Value

## ■ APPLICATION NOTE

Please input the recommendation voltage on each power supply terminal.

When impressing the voltage of the recommendation outside, there is a possibility to destroying by latch up of the inner device.

When not making IC move, please use a power save mode. Or please don't input the voltage on any power supply terminals.

### •Power supply sequence

When input V- (-5V) first, V+ (3.3V) power supply terminal will be the negative voltage. There is a possibility that a regulator of V+ power supply doesn't move in that case.

When V-power supply is impressed at the state that a regulator of V+ power supply doesn't move, an excessive electric current flows to IC. And the worst in case of is destroyed.

Please input V+ power supply and V- power supply at the same time. Or please input V+ power supply first.

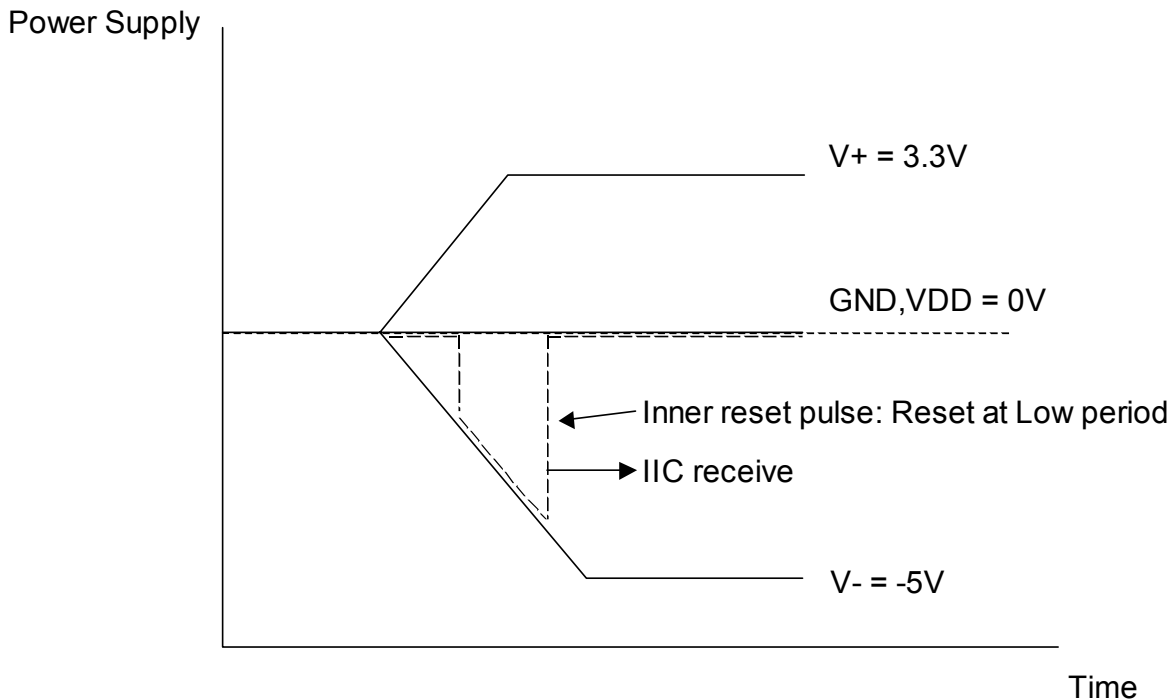
Please turn off V-power supply first at the time at power supply off. Or please turn off V+ power supply and V- power supply at the same time.

After the inner reset pulse stood up in High from Low, please do the timing to which IIC is sent. (Figure 1 referring)

The inner reset pulse is when V- terminal was about -2.5V in ambient temperature at time to stand up in High from Low. Therefore time of the reset pulse is proportional to the rising rate of the V- power supply.

The above fluctuates by variability of the temperature and variability of a device.

Therefore please send IIC after it'll be by V- power supply less than -3.0 V.



(Figure 1)

■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
46 45 44 43 42 41 40	VIN1 VIN2 VIN3 VIN4 VIN5 VIN6 VIN7	Input for CVBS		0V
16 17 18 20 21 22 24 25 26	YIN1 YIN2 YIN3 PBIN1 PBIN2 PBIN3 PRIN1 PRIN2 PRIN3	Input for component video		0V

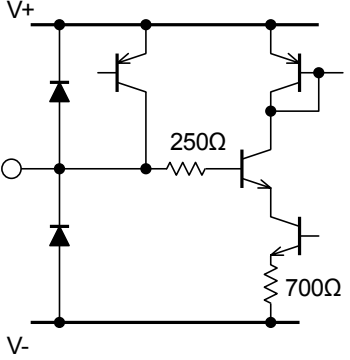
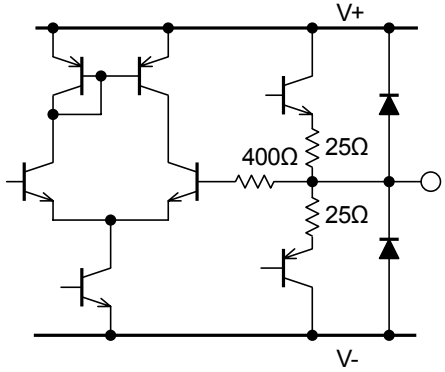
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
47	BIASV1	Bias voltage for CVBS	<p>The circuit diagram for BIASV1 shows a differential amplifier structure. It consists of two input transistors with their emitters connected to a common emitter node. This node is connected to a 250Ω resistor leading to the V- supply. The bases of the input transistors are connected to a 180Ω resistor and a 25kΩ resistor, which are both connected to the V+ supply. The collector of the right input transistor is connected to a 500Ω resistor leading to the V- supply. The output is taken from the collector of the right input transistor. There are also two diodes connected to the V+ supply and two diodes connected to the V- supply, forming a clamp circuit.</p>	0V
15 19 20	BIASY1 BIASPB1 BIASPR1	Bias voltage for component vided	<p>The circuit diagram for BIASY1, BIASPB1, and BIASPR1 shows a differential amplifier structure similar to BIASV1. It consists of two input transistors with their emitters connected to a common emitter node. This node is connected to a 200Ω resistor leading to the V- supply. The bases of the input transistors are connected to a 200Ω resistor and a 25kΩ resistor, which are both connected to the V+ supply. The collector of the right input transistor is connected to a 720Ω resistor leading to the V- supply. The output is taken from the collector of the right input transistor. There are also two diodes connected to the V+ supply and two diodes connected to the V- supply, forming a clamp circuit.</p>	0V

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
13 34 39 48	V+	Positive power supply		3.3V
7 14 27 35 49	V-	Negative power supply		-5V
5	GND	Ground		0V
2	VDD	Power supply for logical circuit		0V
3	SCL	I <sup>2</sup> C Clock Input		-
4	SDA	I <sup>2</sup> C Data Input		-

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
11	PS	Power Save		0V
33	YOUT	Y Output For 75Ω Drive		0V
31 29	PBOUT PROUT	Pb Output Pr Output For 75Ω Drive		0V
38 36	VOUT1 VOUT2	V Output For 75Ω Drive		0V

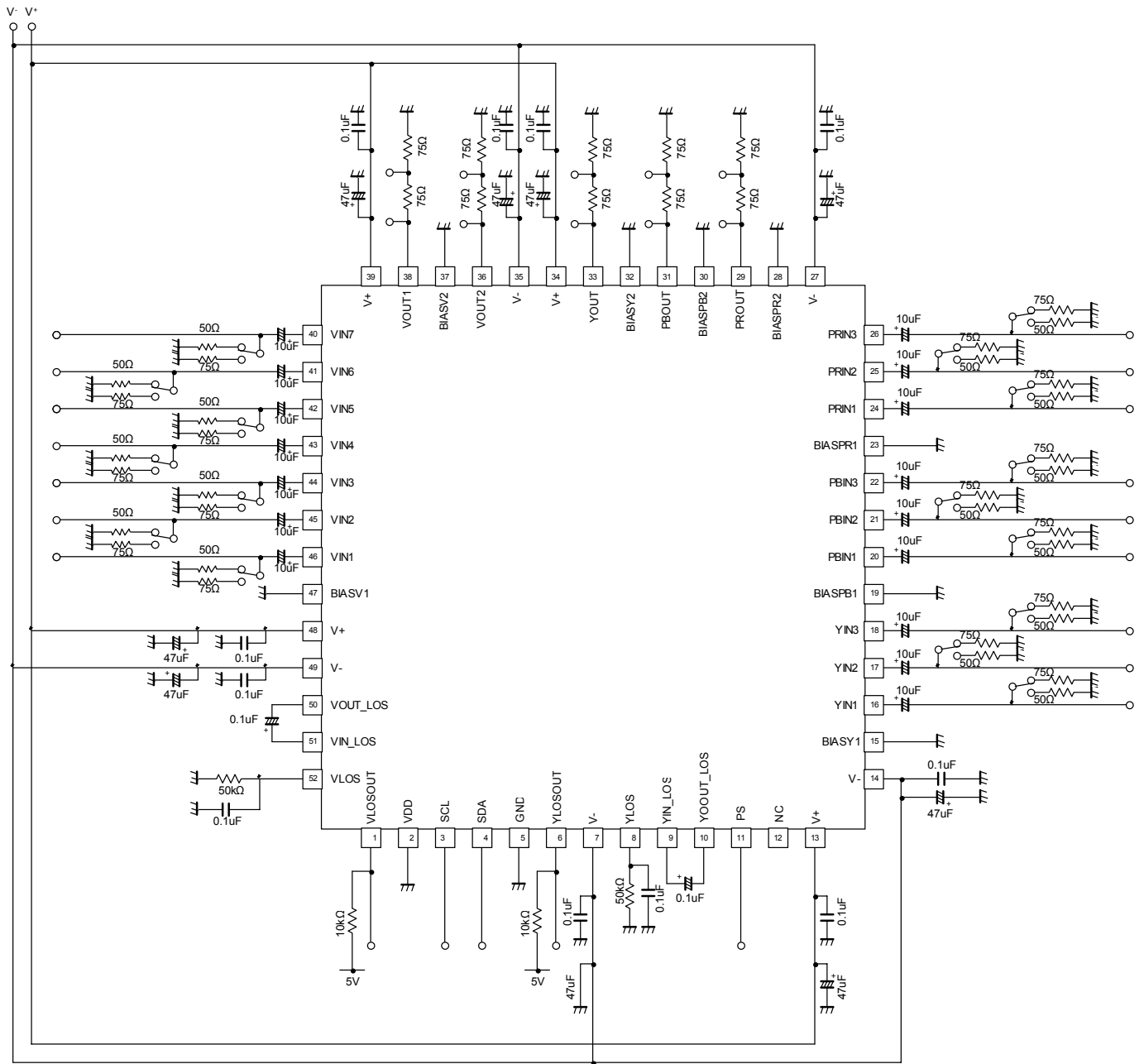
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
32 30 28	BIASY2 BIASPB2 BIASPR2	Bias voltage for component video		0V
37	BIASV2	Bias voltage for CVBS		0V
1 6	VLOSOUT YLOSOUT	VLOS Output YLOS Output		-
8 52	YLOS VLOS	V LOS Detect Filter Y LOS Detect Filter		-

# NJW1329

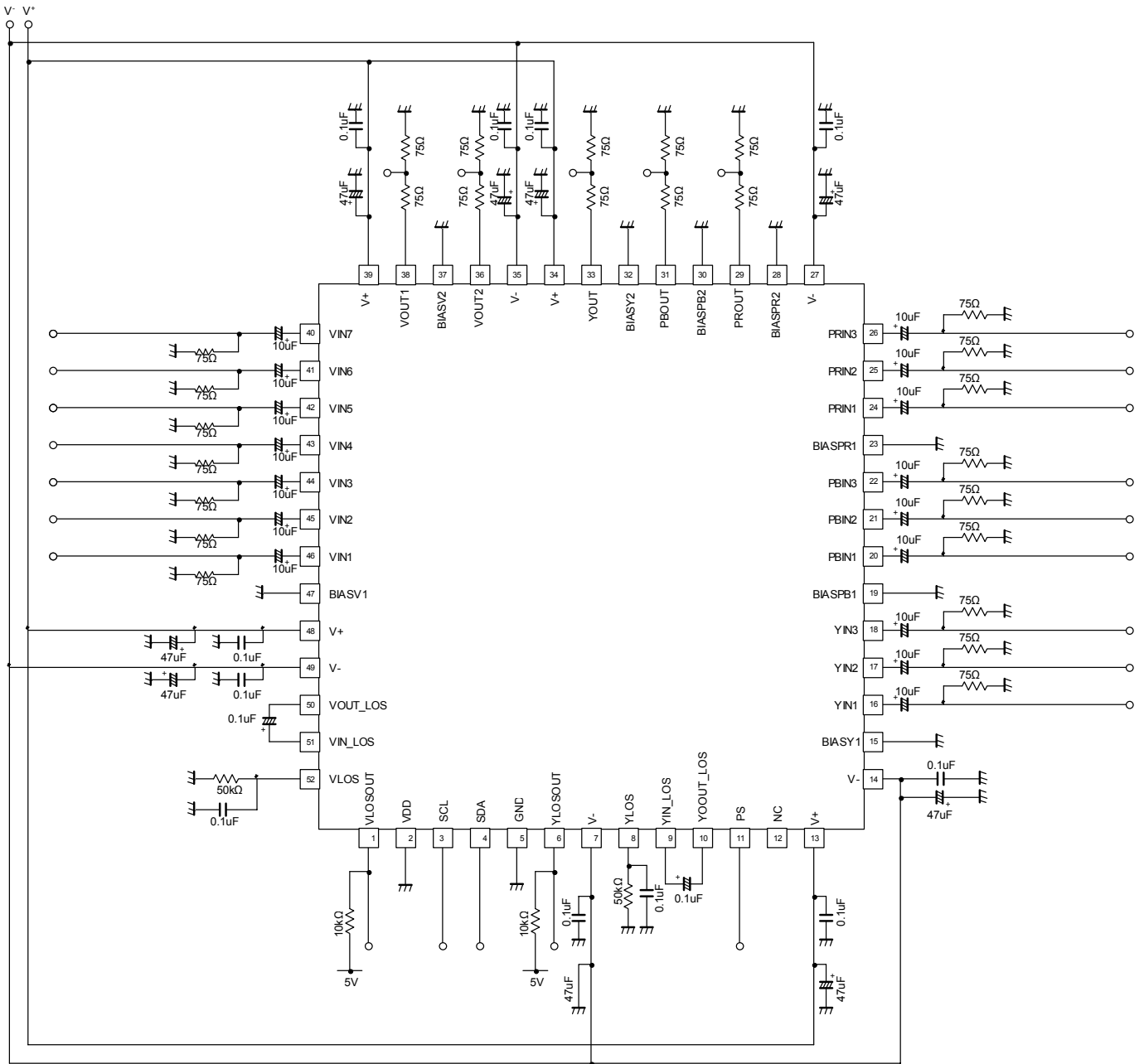
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
9 51	YIN_LOS VIN_LOS	Y Input for LOS V Input for LOS		1.4V
10 50	YOUT_LOS VOUT_LOS	Y output for LOS V output for LOS		0V



## TEST CIRCUIT



## APPLICATION CIRCUIT



**[CAUTION]**  
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