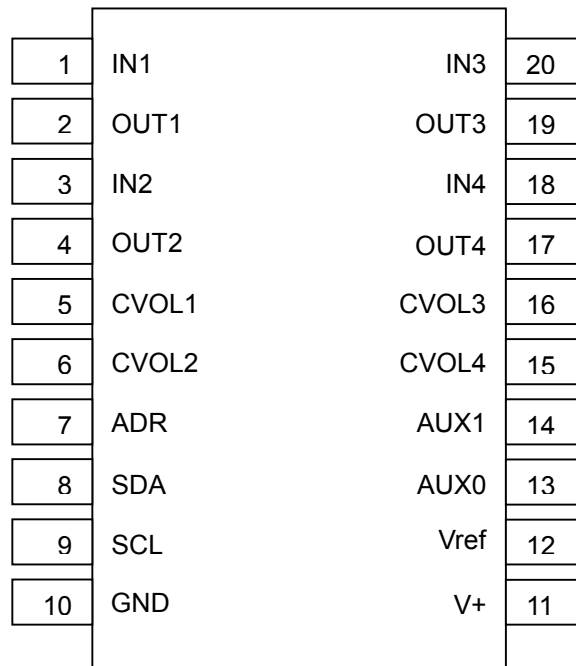


■PIN CONFIGURATION



No.	Symbol	Function	No.	Symbol	Function
1	IN1	Input 1	11	V+	Power Supply Pin
2	OUT1	Output 1	12	Vref	Reference Voltage
3	IN2	Input 2	13	AUX0	Auxiliary Output0
4	OUT2	Output 2	14	AUX1	Auxiliary Output1
5	CVOL1	DAC Output for Volume 1	15	CVOL4	DAC Output for Volume 4
6	CVOL2	DAC Output for Volume 2	16	CVOL3	DAC Output for Volume 3
7	ADR	Slave Address Setting	17	OUT4	Output 4
8	SDA	SDA Data Input (I ² C BUS)	18	IN4	Input 4
9	SCL	SCL Data Input (I ² C BUS)	19	OUT3	Output 3
10	GND	GND	20	IN3	Input 3

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V ⁺	15	V
Maximum Input Voltage	V _{IM}	0 to V ⁺ (*)	V
Power Dissipation	P _D	DMP20 : 350	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(*) For the maximum input voltage less than 0 to V⁺

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V+=9V, R_L=47kΩ, Vin=100mVrms/1kHz, unless otherwise specified)

● POWER SUPPLY

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		7.5	9.0	13.0	V
Supply Current	I _{CC}	No Signal	-	4	10	mA
Reference Voltage	V _{REF}	No Signal	4.0	4.5	5.0	V

● VOLUME

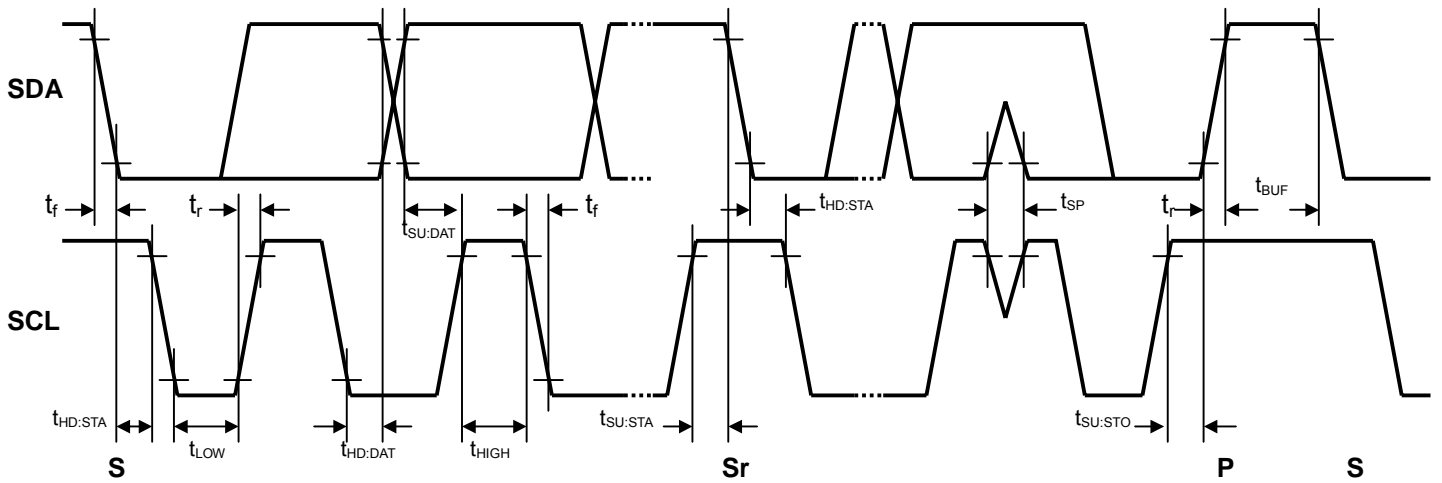
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Voltage	V _{IM}	VOL=-20dB, THD=1%	2.8	3.0	-	Vrms
Maximum Output Voltage	V _{OM}	OUTPUT VOL=0dB, THD=1%	-	2.5	-	Vrms
Channel Balance	G _{CB}	VOL=0dB	-1.0	0.0	1.0	dB
Total Harmonic Distortion	THD	Vo=0.5Vrms BW=400Hz to 30kHz	-	-	0.3	%
Maximum Gain	G _{VMAX}	VOL= 0dB	-2.0	0.0	2.0	dB
Minimum Gain	G _{VMIN}	VOL= MUTE, Vin=2Vrms	-	-100	-90	dB
Channel Separation	CS	Vin = 1Vrms A-weighting	-	-80	-70	dB
Output Noise 1	V _{NO1}	VOL = 0dB A-weighting	-	-90 (31.6)	-85 (56.2)	dBV (μVrms)
Output Noise 2	V _{NO2}	VOL = MUTE A-weighting	-	-106 (5.0)	-96 (15.8)	dBV (μVrms)
Input Impedance	R _i		-	20	-	kΩ
AUX Output Voltage	V _{AUX}	Logic Output: High	4.5	-	5.5	V
		Logic Output: Low	0	-	0.5	

BW: Band Width

● CONTROL

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V _{ADRH}	High : Slave Address 82H	V ⁺ /2	-	-	V
Low Level Input Voltage	V _{ADRL}	Low : Slave Address 80H	-	-	1.0	V

■TIMING ON THE I²C BUS (SDA,SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA,SCL)

I²C BUS Load Conditions

STANDARD MODE : Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

FAST MODE : Pull up resistance 4kΩ (Connected to +5V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V _{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V _{IH}	2.7	-	5.0	2.7	-	5.0	V
Low level output voltage (3mA at SDA pin)	V _{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between 0.1V _{DD} and 0.9V _{DDmax}	I _i	-10	-	10	-10	-	10	μA

■ CHARACTERISTICS OF BUS LINES (SDA,SCL) FOR I²C-BUS DEVICES

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f _{SCL}	-	-	100	-	-	400	kHz
Hold time (repeated) START condition.	t _{HD:STA}	4.0	-	-	0.6	-	-	μs
Low period of the SCL clock	t _{LOW}	4.7	-	-	1.3	-	-	μs
High period of the SCL clock	t _{HIGH}	4.0	-	-	0.6	-	-	μs
Set-up time for a repeated START condition	t _{SU:STA}	4.7	-	-	0.6	-	-	μs
Data hold time ^(NOTE)	t _{HD:DAT}	0	-	-	0	-	-	μs
Data set-up time	t _{SU:DAT}	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t _r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t _f	-	-	300	-	-	300	ns
Set-up time for STOP condition	t _{SU:STO}	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t _{BUF}	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C _b	-	-	400	-	-	400	pF
Noise margin at the Low level	V _{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High level	V _{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

NOTE). Data hold time : t_{HD:DAT}

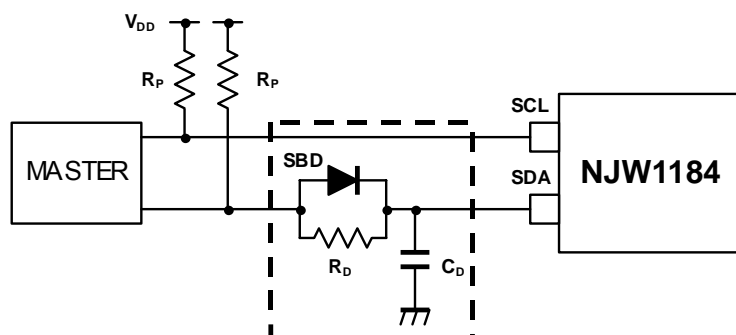
Please hold the Data Hold Time (t_{HD:DAT}) to 300ns or more to avoid status of unstable at SCL falling edge.

The SDA block in the NJW1184 does not hold data. Add external data-delay-circuit of the SDA terminal, in case of not providing a hold time of at least 300nsec for the SDA in the master device.

The time-consists of the data-delay-circuit of the SDA terminal are as follows.

- (a) Low level → High level : $T_{LH} \approx R_p \cdot C_D$
- (b) High level → Low level : $T_{HL} \approx R_D \cdot C_D$

In addition, Schottky barrier diode (SBD) influences a Low level at the Acknowledge. Therefore choose the low forward voltage (V_f) as much as possible.



■ TERMINAL DESCRIPTION

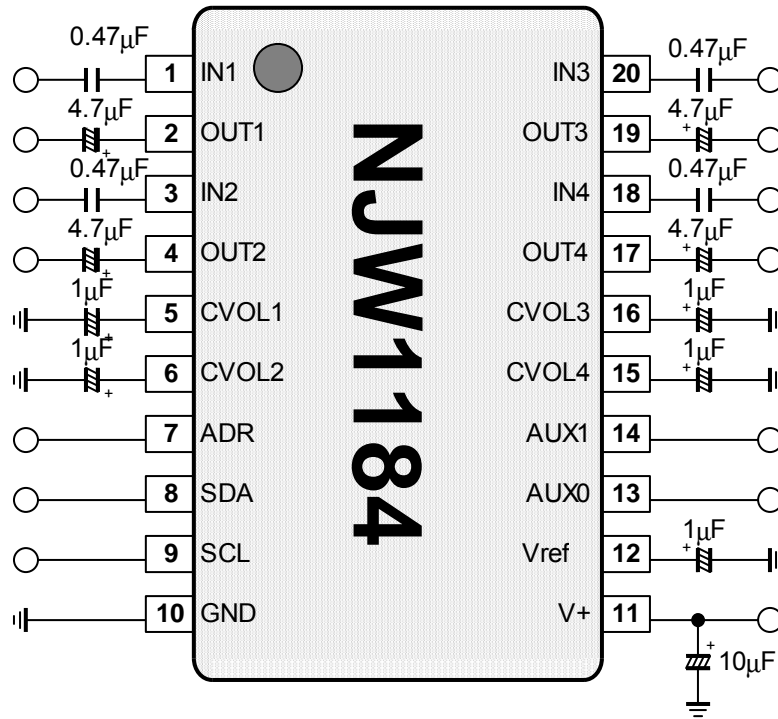
PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
1 3 20 18	IN1 IN2 IN3 IN4	Input 1 Input 2 Input 3 Input 4		$V^+/2$
2 4 19 17	OUT1 OUT2 OUT3 OUT4	Output 1 Output 2 Output 3 Output 4		$V^+/2$
5 6 16 15	CVOL1 CVOL2 CVOL3 CVOL4	DAC Output for Volume 1 DAC Output for Volume 2 DAC Output for Volume 3 DAC Output for Volume 4		$V^+/2 - 0.7V$ (0dB setting)
7	ADR	Slave Address Setting		82(h) $V_{ADR} > V^+/2$ 80(h) $V_{ADR} \leq 1.0V$

■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
8 9	SDA SCL	SDA Data Input (I ² C BUS) SCL Data Input (I ² C BUS)	<p style="text-align: center;">SCL:GND SDA:ACK</p>	-
12	Vref	Reference Voltage		$V^+/2$
13 14	AUX0 AUX1	Auxiliary Output 0 Auxiliary Output 1		0V / 5V

NJW1184

APPLICATION CIRCUIT



■ DEFINITION OF I²C REGISTER

● I²C BUS FORMAT



S: Starting Term
A: Acknowledge Bit
P: Ending Term

● SLAVE ADDRESS



ADR: Hardware pin programmable address bits
80(h), 82(h)

R/W=0: Write mode for register setting
R/W=1: Not available

● CONTROL REGISTER TABLE

The select address sets each function (Volume, Aux).
The auto-increment function cycles the select address as follows.
00H→01H→02H→03H→04H→00H

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOL-1							
01H	VOL-2							
02H	VOL-3							
03H	VOL-4							
04H	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	AUX1	AUX0

● CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0
02H	0	0	0	0	0	0	0	0
03H	0	0	0	0	0	0	0	0
04H	0	0	0	0	0	0	0	0

■ I²C CONTROL COMMAND DESCRIPTION

a) Master Volume (Select Address: 00H, 01H, 02H, 03H) Volume level : 0 to -100dB(0.5dB/step), MUTE

Gain(dB)	HEX	VOL-1 / VOL-2 / VOL-3 / VOL-4							
		D7	D6	D5	D4	D3	D2	D1	D0
0	FF	1	1	1	1	1	1	1	1
-0.5	FE	1	1	1	1	1	1	1	0
-1.0	FD	1	1	1	1	1	1	0	1
-1.5	FC	1	1	1	1	1	1	0	0
-2.0	FB	1	1	1	1	1	0	1	1
-2.5	FA	1	1	1	1	1	0	1	0
-3.0	F9	1	1	1	1	1	0	0	1
-3.5	F8	1	1	1	1	1	0	0	0
-4.0	F7	1	1	1	1	0	1	1	1
-4.5	F6	1	1	1	1	0	1	1	0
-5.0	F5	1	1	1	1	0	1	0	1
-5.5	F4	1	1	1	1	0	1	0	0
-6.0	F3	1	1	1	1	0	0	1	1
-6.5	F2	1	1	1	1	0	0	1	0
-7.0	F1	1	1	1	1	0	0	0	1
-7.5	F0	1	1	1	1	0	0	0	0
-8.0	EF	1	1	1	0	1	1	1	1
-8.5	EE	1	1	1	0	1	1	1	0
-9.0	ED	1	1	1	0	1	1	0	1
-9.5	EC	1	1	1	0	1	1	0	0
-10.0	EB	1	1	1	0	1	0	1	1
-10.5	EA	1	1	1	0	1	0	1	0
-11.0	E9	1	1	1	0	1	0	0	1
-11.5	E8	1	1	1	0	1	0	0	0
-12.0	E7	1	1	1	0	0	1	1	1
-12.5	E6	1	1	1	0	0	1	1	0
-13.0	E5	1	1	1	0	0	1	0	1
-13.5	E4	1	1	1	0	0	1	0	0
-14.0	E3	1	1	1	0	0	0	1	1
-14.5	E2	1	1	1	0	0	0	1	0
-15.0	E1	1	1	1	0	0	0	0	1
-15.5	E0	1	1	1	0	0	0	0	0
-16.0	DF	1	1	0	1	1	1	1	1
-16.5	DE	1	1	0	1	1	1	1	0
-17.0	DD	1	1	0	1	1	1	0	1
...
-99.5	38	0	0	1	1	1	0	0	0
-100.0	37	0	0	1	1	0	1	1	1
...
Mute	00	0	0	0	0	0	0	0	0

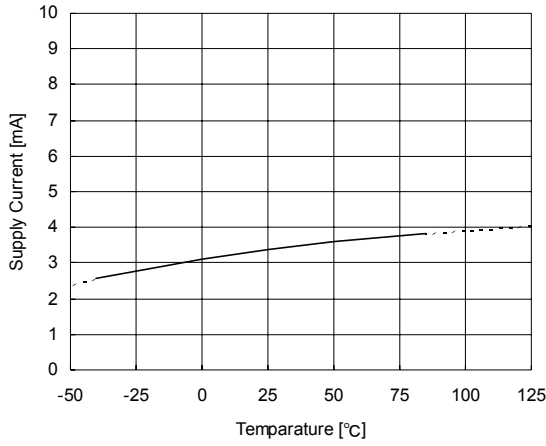
b) AUXILIARY SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
04H	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	AUX1	AUX0

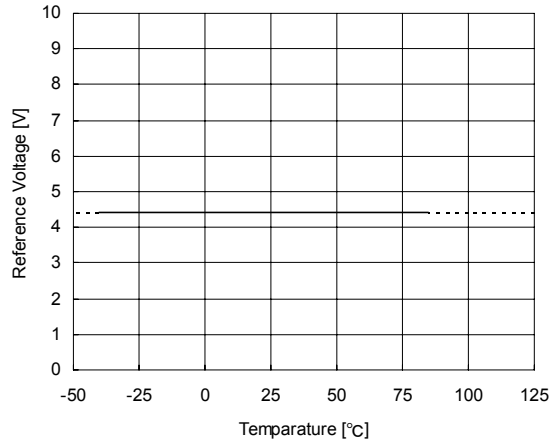
- AUX1/AUX0: Auxiliary port High/Low
 - “0” : Logic output "Low"
 - “1” : Logic output "High"

■ TYPICAL CHARACTERISTICS

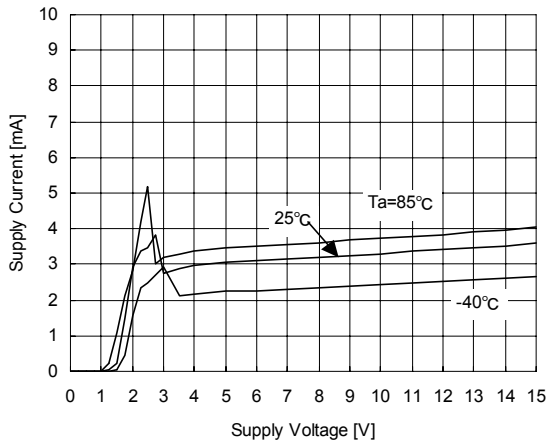
Supply Current vs Temperature
 $V+=9V$, V_{in} =No Signal, Volume=0dB



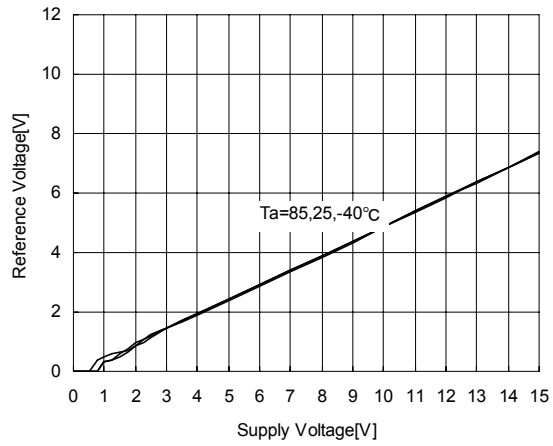
Reference Voltage vs Temperature
 $V+=9V$, V_{in} =No Signal, Volume=0dB



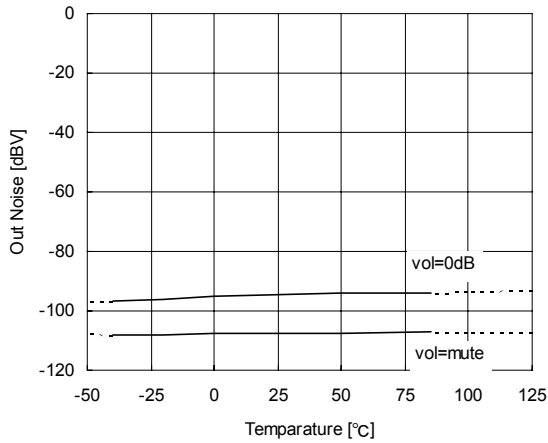
Supply Current vs Supply Voltage
 V_{in} =No Signal, Volume=0dB



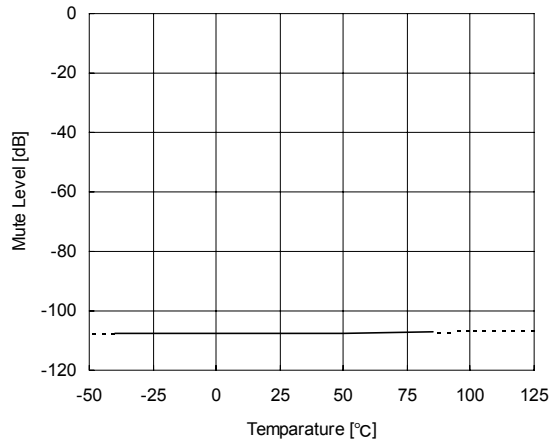
Reference Voltage vs Supply Voltage
 V_{in} =No Signal, Volume=0dB



Out Noise vs Temperature
 $V+=9V$, $R_g=600\Omega$, A-Weighting



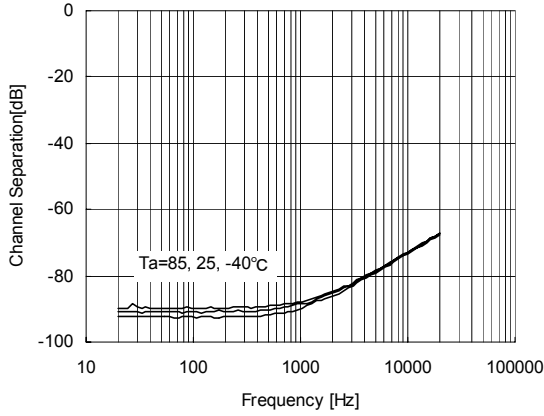
Mute Level vs Temperature
 $V+=9V$, $R_g=600\Omega$, $V_{in}=1V_{rms}$, A-Weighting



TYPICAL CHARACTERISTICS

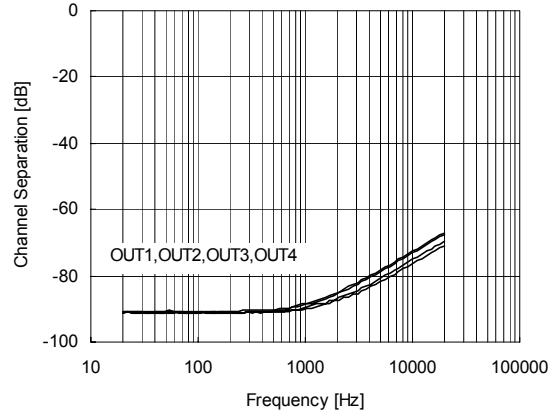
Channel Separation vs Frequency

V+=9V, Vin=1Vrms, A-Weighting, Rg=600Ω
Vin:IN2+IN3+IN4, Vout:OUT1



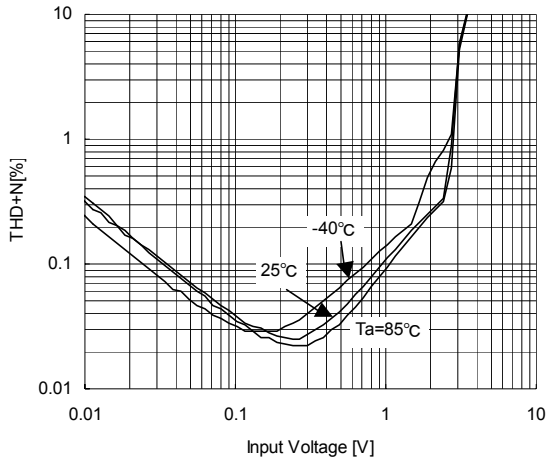
Channel Separation vs Frequency

V+=9V, Vin=1Vrms, A-Weighting, Ta=25°C
Rg=600Ω



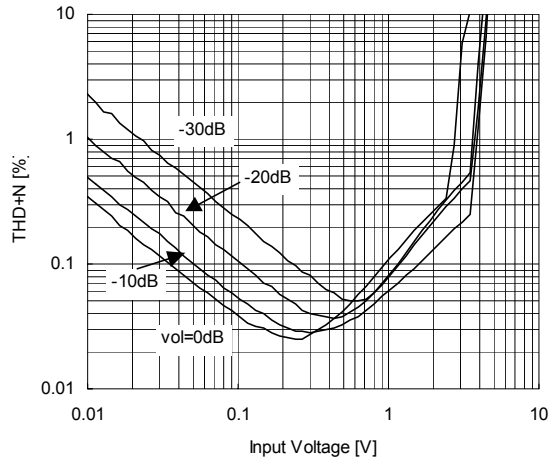
THD+N vs Input Voltage (Temperature)

V+=9V, Vin=CH1, f=1kHz, volume=0dB
Rg=600Ω, BW=400Hz-30kHz, Vout=OUT1



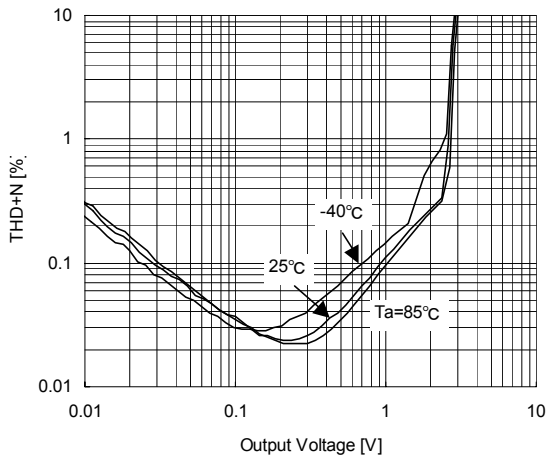
THD+N vs Input Voltage (Volume Control)

V+=9V, Vin=CH1, f=1kHz, Ta=25°C
Rg=600Ω, BW=400Hz-30kHz, Vout=OUT1



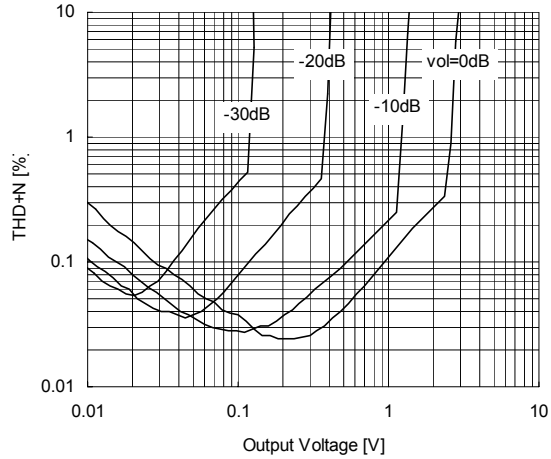
THD+N vs Output Voltage (Temperature)

V+=9V, Vin=CH1, f=1kHz, volume=0dB
Rg=600Ω, BW=400Hz-30kHz, Vout=OUT1



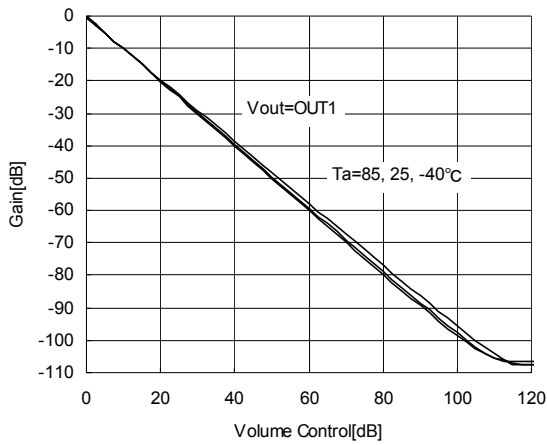
THD+N vs Output Voltage (Volume Control)

V+=9V, Vin=CH1, f=1kHz, Ta=25°C
Rg=600Ω, BW=400Hz-30kHz, Vout=OUT1

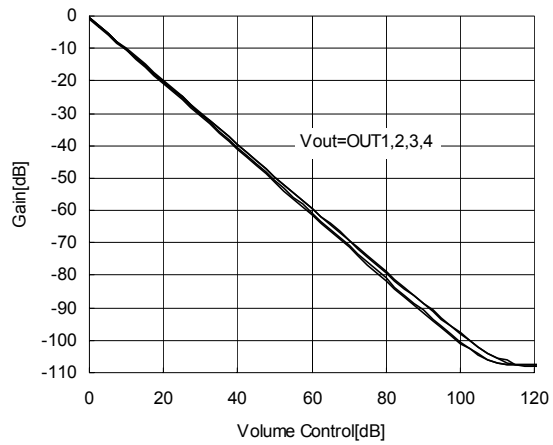


■ TYPICAL CHARACTERISTICS

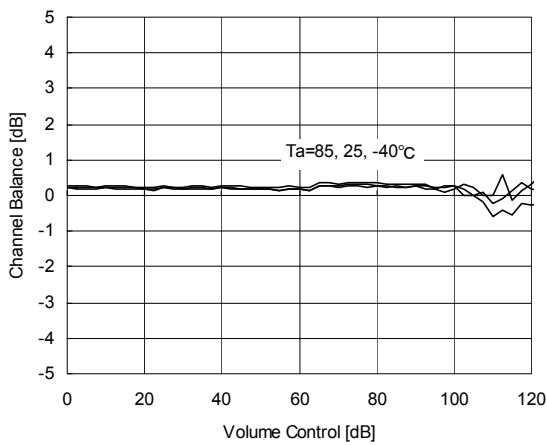
Gain vs Volume Control (Temperature)
 $V+=9V, R_g=600\Omega, V_{in}=1V_{rms}, V_{in}=IN1$



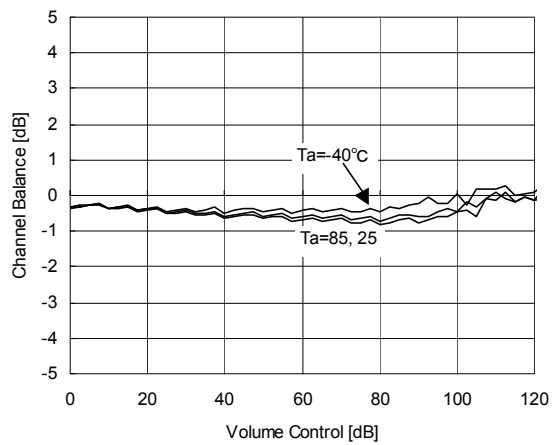
Gain vs Volume Control
 $V+=9V, R_g=600\Omega, V_{in}=1V_{rms}, T_a=25^\circ C$



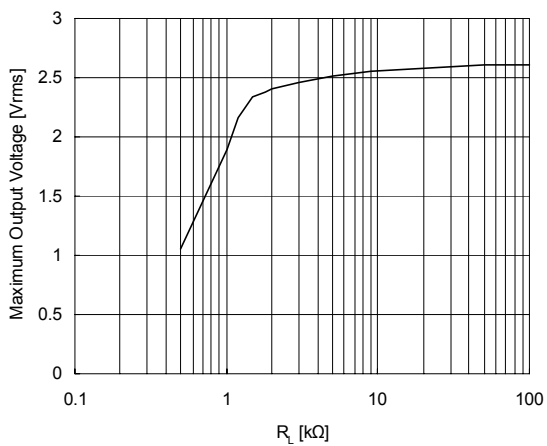
Channel Balance vs Volume Control (CH1-CH2)
 $V_{in}=1V_{rms}, V+=9V$



Channel Balance vs Volume Control (CH3-CH4)
 $V_{in}=1V_{rms}, V+=9V$



Maximum Output Voltage vs RL
 $V+=9V, THD=1\%$



[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.