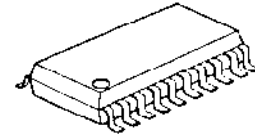


1200 bps MSK Modem for Data Communication

■ GENERAL DESCRIPTION

The NJU7512 is a 1200bps MSK (Minimum Shift Keying) modem IC, which operates from 1.8V power supply. It includes 14.7456MHz oscillator and selectable OSC buffer for an external output, and a frame detector for receiving. MSK modem is especially used for low power data communication, which requires high receiving sensitivity and noise susceptibility characteristics.

■ PACKAGE OUTLINE



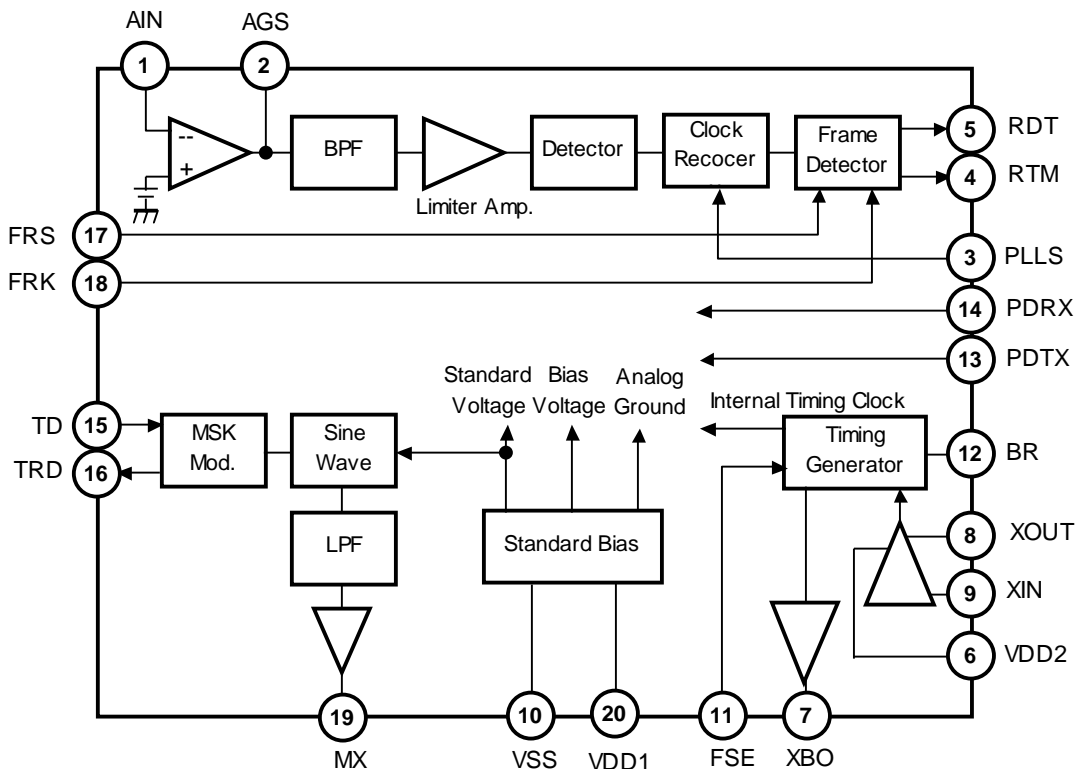
NJU7512VT

■ FEATURES

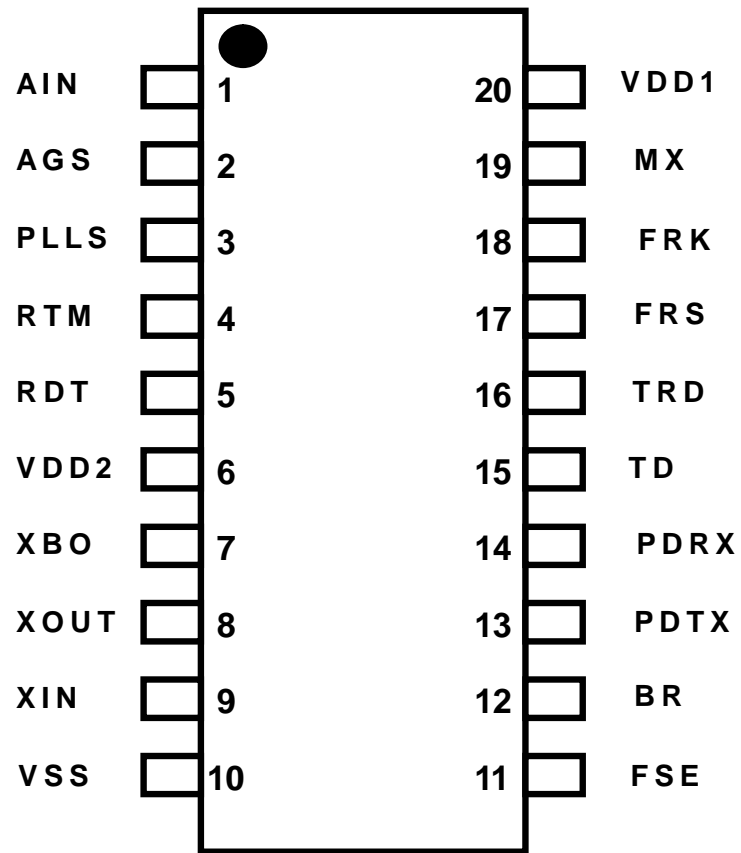
- | | |
|------------------------------------|---|
| ● Low Operating Current | 1.9mA (Modulation and Demodulation operation, VDD=1.8V) |
| ● Wide Operating Voltage range | 1.8 to 5.5V |
| ● Baud Rate | 1200 bps |
| ● Oscillating Frequency | 14.7456 MHz |
| ● Selectable OSC Buffer Output | 14.7456 MHz or 3.6864 MHz |
| ● Built-in Frame Detector | 2 types of frame data or disable |
| ● Power Save Function | Power control for Modulator and Demodulator blocks respectively |
| ● Easy to use modem function | A few external parts required |
| ● Wide Operating Temperature range | - 40 to +105 °C |
| ● CMOS Technology | |
| ● Package Outline | SSOP20 6.5mm x 6.4mm, t=0.65mm |

Please refer the IC Package information about the Package outline and Packing.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

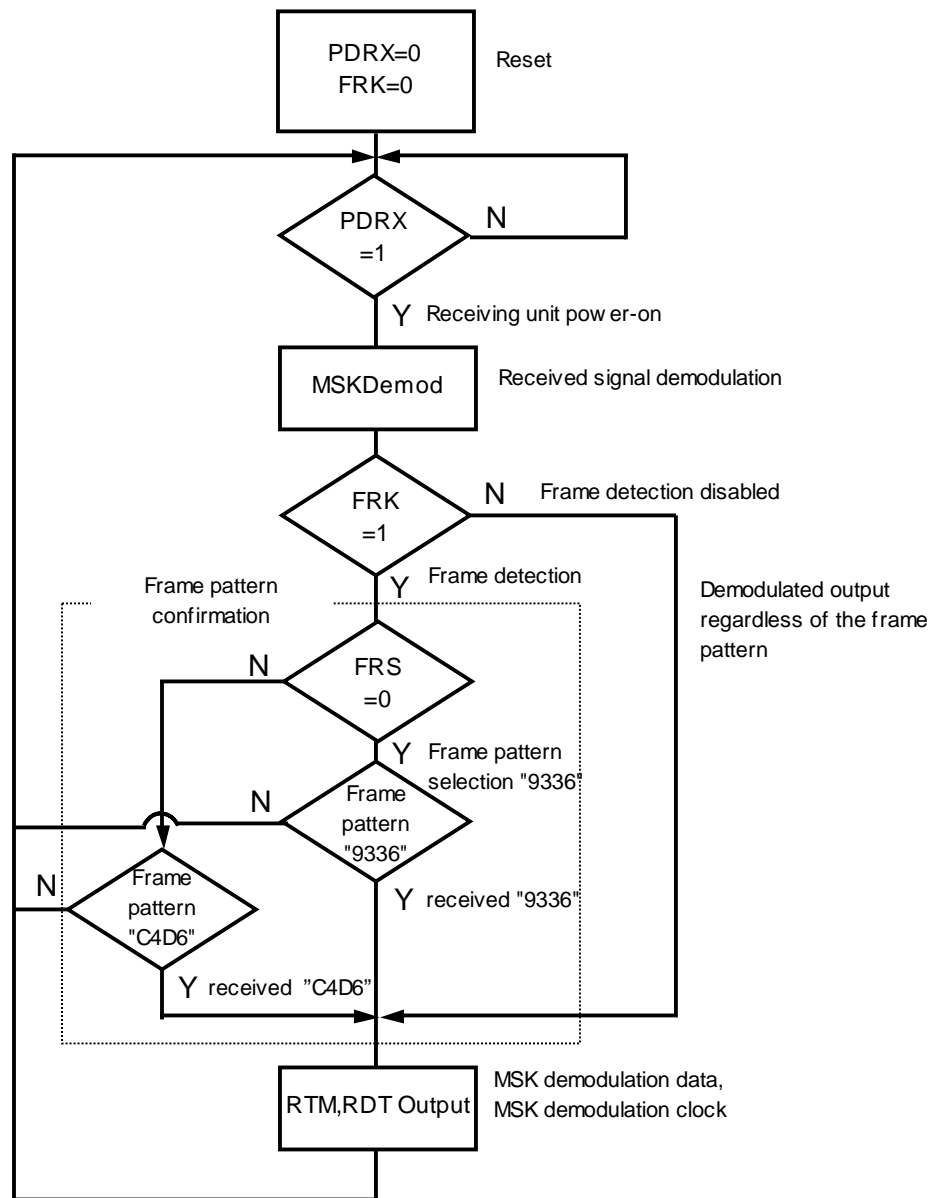


NJU7512VT

■ TERMINAL DESCRIPTION

Pin No.	SYMBOL	Function	In Power Down					
			PDTX = Low	PDRX = Low				
1	AIN	Input terminal of the Input buffer amplifier	-	-				
2	AGS	Output terminal of the input buffer amplifier	-	Low				
3	PLLS	PLL control input terminal Selection of the phase correction speed of PLL of the detector, either low-speed or high-speed correction.	PLLS	Phase correction speed	-	-		
			High	Low-speed phase correction				
			Low	High-speed phase correction				
4	RTM	MSK demodulation synchronous clock output terminal	-	High				
5	RDT	MSK demodulation data output terminal It synchronizes with falling of the MSK demodulation synchronous clock.	-	-				
6	VDD2	Oscillator circuit power supply terminal	-	-				
7	XBO	Output of oscillator circuit buffer This is the output terminal of the oscillator circuit buffer to supply to external circuits.	High	-				
8	XOUT	Oscillator circuit output terminal A crystal oscillator is connected between this pin and XIN terminals. When using an external clock, This terminal doesn't need to connect (no connection).	High	-				
9	XIN	Oscillator circuit input terminal A crystal oscillator is connected between this pin and XOUT terminals. When using an external clock, it becomes an input terminal for it.	-	-				
10	VSS	Grand terminal	-	-				
11	FSE	Selection of the buffer output frequency Select either oscillating frequency or 1/4 frequency for buffer output frequency. * A frequency of the crystal oscillator is 14.7456 MHz.	FSE	Output Frequency (MHz)	-	-		
			High	3.6864				
			Low	14.7456				
12	BR	Transmission-speed control terminal Always Logical High	BR	speed (bps)	Career frequency (Hz)		-	-
			High	1200	Data 1	Data 0		
					1200	1800		
13	PDTX	Control terminal of the modulation block for power down function.	PDTX	Operation		-	-	
			High	Modulation block power-on				
			Low	Modulation block power-off				
14	PDRX	Control terminal of the demodulation block for power down function.	PDRX	Operation		-	-	
			High	Demodulation block power-on				
			Low	Demodulation block power-off				
15	TD	MSK modulation data input terminal The modulation data is red at the rise timing of TRD signal.	-	-				
16	TRD	MSK modulation data read-timing output terminal The data of TD terminal is red in synchronizing with a rise edge.	Low	-				
17	FRS	Selection of the frame data 16 bits, 2 types of the frame data When the selected frame data is received, RTM and RDT are output.	FRS	Frame Data		-	-	
			High	1100010011010110 B (C4D6 H)				
			Low	1001001100110110 B (9336 H)				
18	FRK	Select enable or disenable of the flame detection	FRK	Operation		-	-	
			High	Enable				
			Low	Disenable				
19	MX	Digital output of MSK modulation signal	Low	-				
20	VDD1	Supply voltage	-	-				

■ DEMODULATION OPERATION FLOW CHART



The basic structure of the analog MSK modulating signal inputted into AIN is as follows.

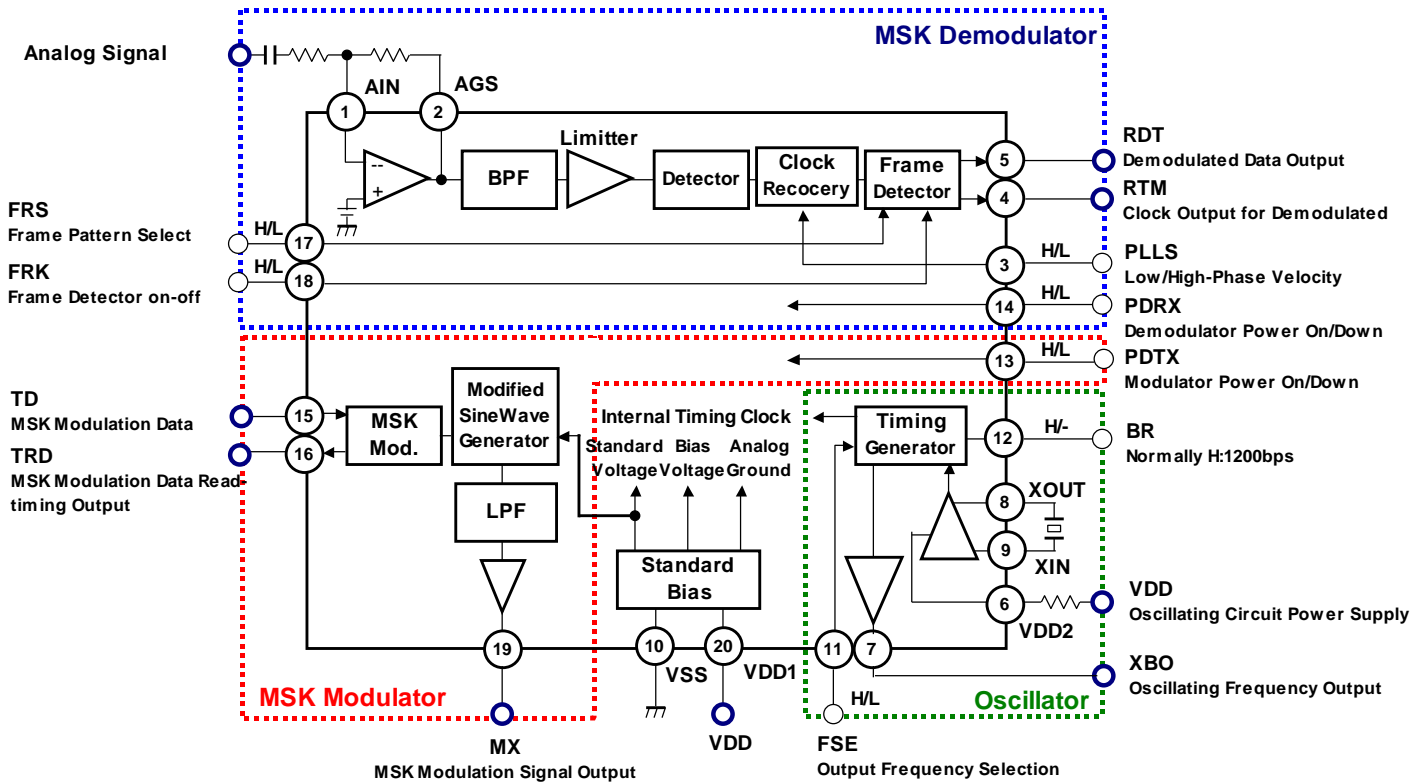
- 1, With a selection frame pattern (Set FRK = 1):
Preamble pattern + 16 bits frame pattern + Received Data
- 2, Without a selection frame pattern (Set FRK = 0):
Received Data (It may include preamble and frame patterns.)

The preamble patterns are repetition of "1" and "0" such as 101010 --, and it is required for PLL synchronization, and the number of bits recommends 12 bits or more than 50 bits by setup of a PLLS terminal (Pin 3).

In the case of setting FRK = 0, the all received signal are demodulated and output from RDT terminal (Pin 5), even if the data has frame pattern.

In the case of setting FRK = 1, the received data is demodulated and it is outputted from a RDT terminal (Pin 5).

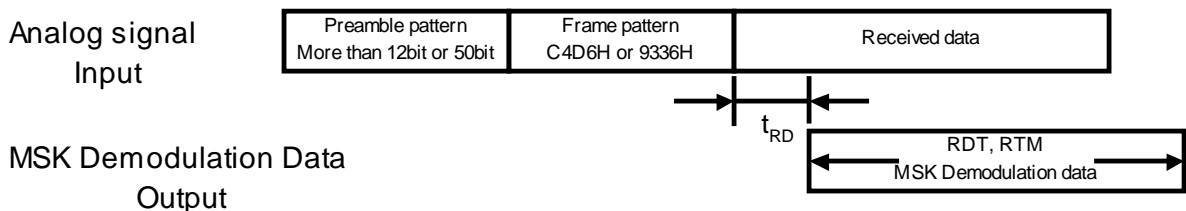
■ DETAILS OF THE TERMINALS AND BLOCKS DESCRIPTION



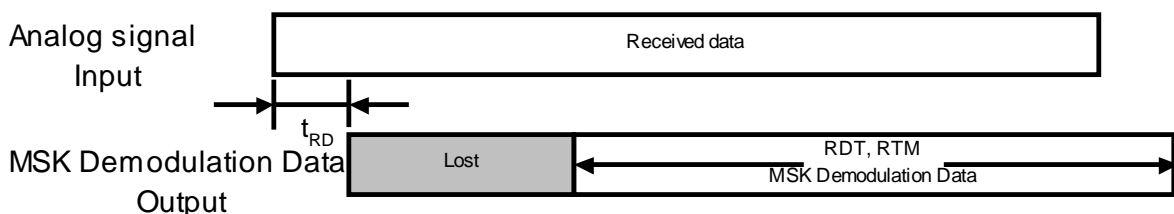
[MSK DEMODULATION CIRCUIT]

● ANALOG RECEIVED SIGNAL INPUT

The analog signal is inputted which is changed to a logical high data from 1200Hz tone (1 cycle / bit, 833.3usec) and to a logical low data from 1800Hz (1.5 cycles / bit, 833.3usec) tone. The maximum speed of digital data is 1200 bps. A received analog signal can be identified with one of two kinds of 16-bit frame pattern signals (C4D6H or 9336H). When performing the frame signal detection, the FRK terminal (Pin 18) is set to logical high. The frame pattern to distinguish is specified by setting FRS terminal (Pin 17) to a logical high or low. The data composition of the input signal with a frame pattern serves as data for a preamble pattern + frame pattern + received data. The demodulated data are outputted from a RDT terminal (Pin 5) without a preamble and frame data. If the preamble pattern is less length than the recommended value, normal demodulation data may not be obtained.



The frame pattern can be disabled with setting a logical low of FRK (Pin 18). If the frame pattern is disabled, all received data output from RDT (Pin 5), but the output from RDT (Pin 5) may have a lack of information at beginning of the receiving.

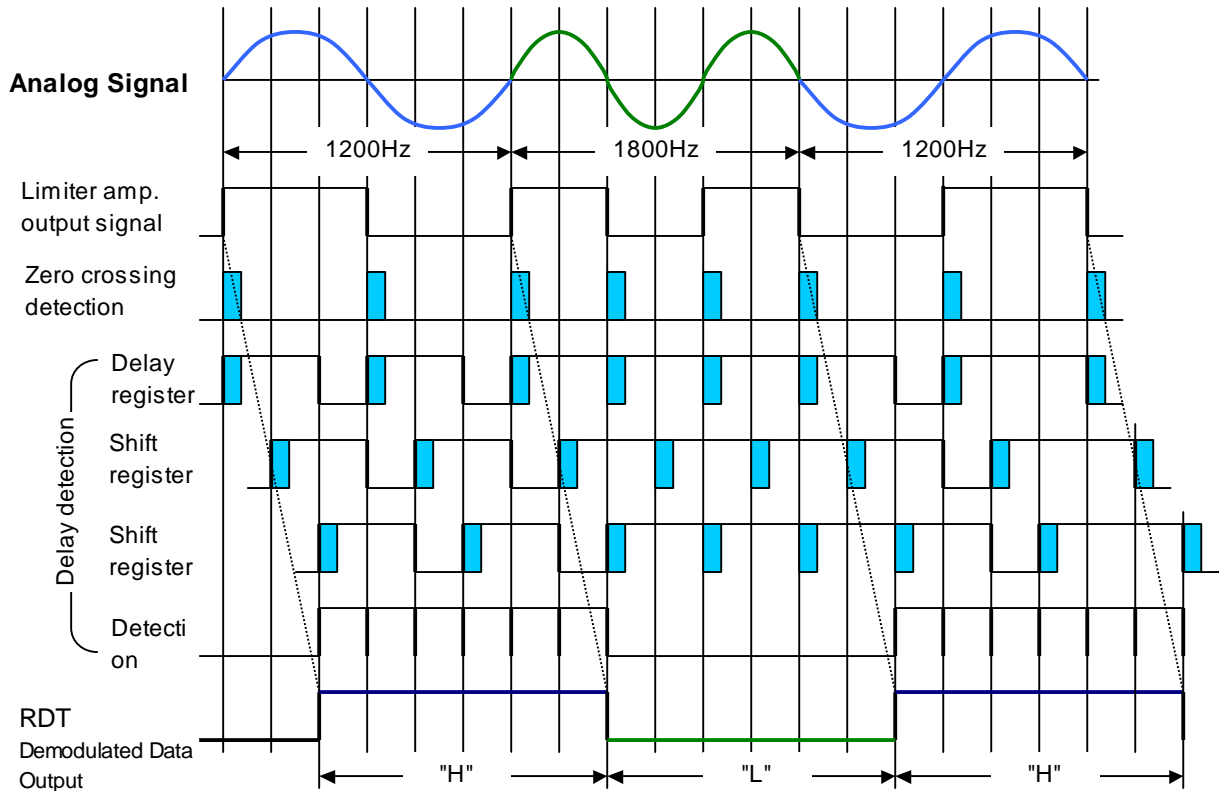


● GAIN CONTROL

An analog signal amplifier is placed between AIN (Pin 1) and AGS (Pin 2). The open loop gain of this amplifier is 60dB min. Extra resistors can fix the gain of this amplifier to optimize the level of the output of AGS terminal (Pin 2) to get the best BER. Refer to [Demodulation bit error rate] of the example of the characteristics for optimal level of an AGS terminal (Pin 2).

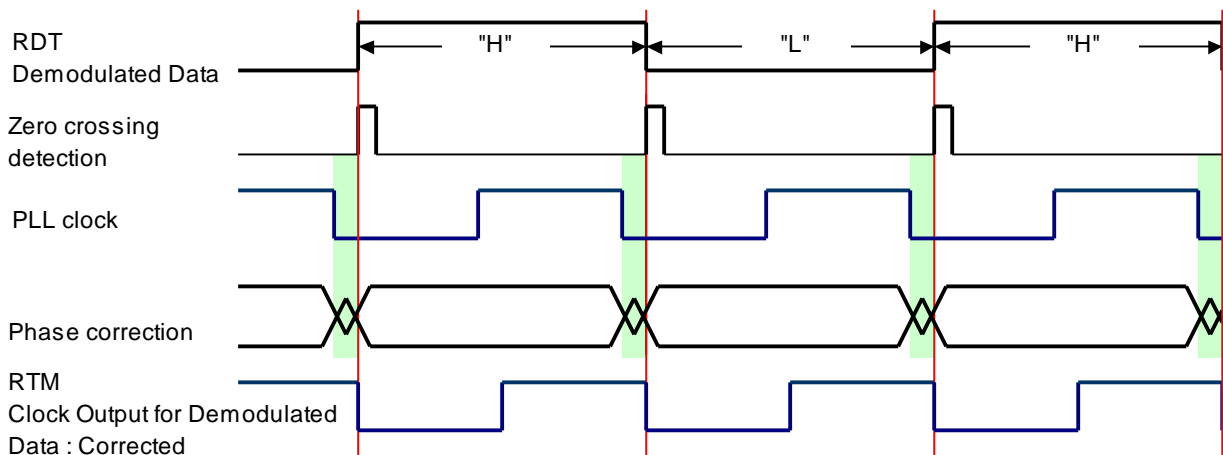
● MSK DEMODULATION DATA OUTPUT TERMINAL (RDT)

It outputs digital data which are demodulated from a received signal. Output voltage is High: VDD to VDD-0.4V and Low: VSS to 0.4V. Data is outputted synchronizing with falling of the signal of RTM.



● MSK DEMODULATION SYNCHRONOUS CLOCK OUTPUT TERMINAL (RTM)

The synchronous clock (RTM, Pin 4) of the demodulated data (RDT, Pin 5) is output. RDT is synchronized with the falling edge of the RTM signal.



• CONTROL TERMINAL (FRS, FRK, PLLS, PDRX)

1. SELECTION OF FRAME PATTERN (FRS)

One from two kinds of 16-bit frame patterns is chosen.

FRS	Selection frame pattern
High	1100010011010110 B (C4D6 H)
Low	1001001100110110 B (9336 H)

2. SELECTION OF FRAME DETECTION (FRK)

Enabled the frame detection or disabled is chosen. When not using the frame detection, all received analog signals serve as data for demodulation.

FRK	Operation
High	Frame detection function enabled
Low	Frame detection function disabled

3. SELECTION OF PHASE CORRECTION SPEED OF CLOCK REPRODUCTION (PLLS)

It is a terminal which controls the pull-in bits of PLL. In order to make a synchronous clock, phase correction is applied to the internal clock, but the maximum phase correction angle is 3.75 degrees in slow mode, and is 30 degrees in fast mode. The length of the preamble pattern (repetition of "1" and "0", such as 101010--) is recommended to 50 bits and more for the slow mode, and to 12 bits and more for the fast mode.

PLLS	Phase correction speed
High	Low-speed phase correction
Low	High rank phase correction

4. MSK demodulating circuit unit power-on / power down selection (PDRX)

The MSK demodulation circuit becomes operational mode in PDRX power-on function, and becomes non-operational mode in the power down function. Moreover, the frame detection circuit is reset by power down.

PDRX	Operation
High	Demodulation block power-on
Low	Demodulation block power-off

[IMPORTANT] When the state of a FRK terminal (Pin 18) and a FRS terminal (Pin 17) is changed or after power supplied, please once choose a power down to prevent any malfunction.

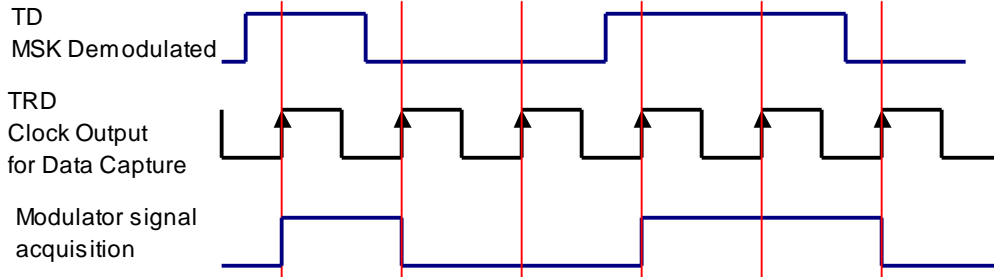
[MSK MODULATION CIRCUIT]

● READ TIMING OF MODULATION DATA (TRD)

A clock signal, one cycle is 833.3usec, is outputted. The digital data of TD terminal (Pin 15) for modulation is red at rising edge of the clock signal.

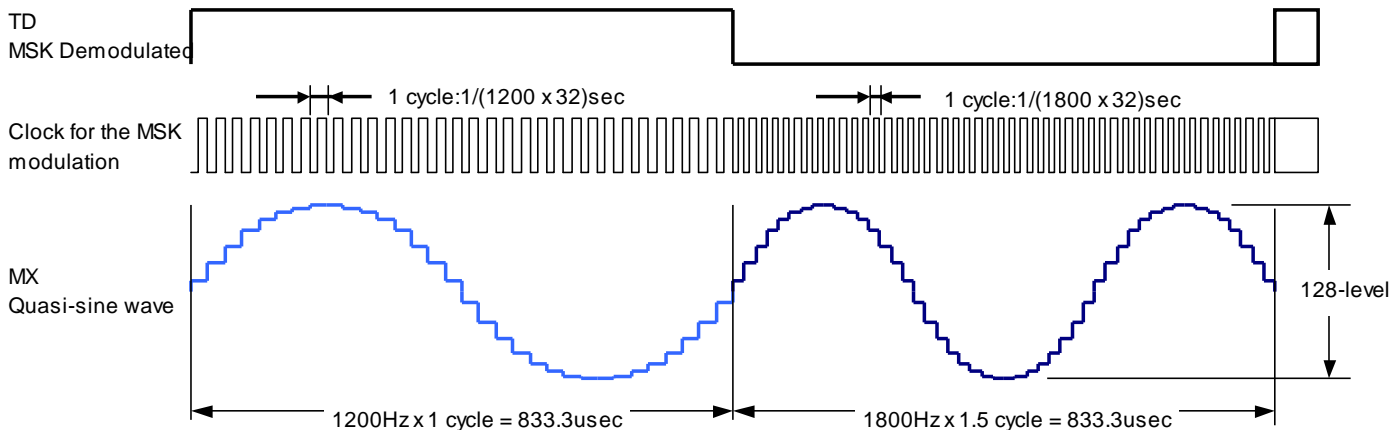
● MODULATION DATA INPUT (TD)

The modulation data are synchronized with the clock signal of TRD (Pin 16) and red.



● MODULATION SIGNAL OUTPUT (MX)

The digital data red from TD terminal (Pin 15) is outputted to the analog signal such as a logical high data converts to 1200Hz tone (1 cycle / bit, 833.3usec) and a Logical Low data converts to 1800Hz (1.5 cycles / bit, 833.3usec) tone. The output level is -6dBV (typical value, load is 30kΩ //50pF). It is referred to as 0dBV = 1Vrms. In addition, in order to remove the harmonics distortion of a quasi sine wave generating circuit, it is outputted through a second order butterworth low pass filter (cut-off frequency of 16 kHz).



● MODULATION BLOCK POWER DOWN CONTROL TERMINAL (PDTX)

The MSK modulation circuit becomes operational mode by PDTX power-on, and becomes non-operational mode by power down. The internal circuit unit is reset by power down. Please once choose a power down to prevent any malfunction at power supply starting. If the power down function is occurred while modulation, the modulation doesn't finish properly. Please refer to a [Timing diagram] for prevention of any malfunction. After PDTX power-on, the internal circuit delay of power-up time tPU occurs. Please refer to a [timing diagram] MSK demodulation timing chart for details.

PDTX	Operation
High	Modulation block power-on
Low	Modulation block power-off

[REFERENCE] TERMINAL CONNECTION OF NOT USING

When not using a modulation circuit, they are connected such as PDTX terminal (Pin 13) = VSS, TD terminal (Pin 15) = High (VDD) or Low (VSS), TRD terminal (Pin 16) = no connection, and the MX terminal (Pin 19) = no connection.

[OSCILLATOR CIRCUIT]

● OSCILLATOR CIRCUIT INPUT TERMINAL (XIN)

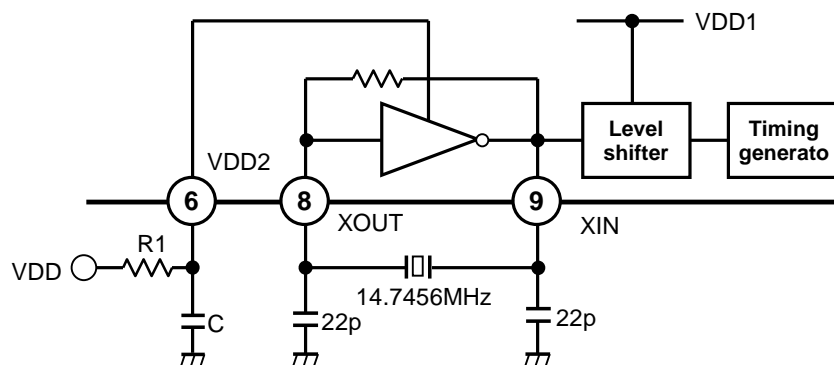
A crystal oscillator is connected between XOUT terminals (Pin 8) (recommended). 14.7456 MHz should be used for the frequency of a crystal oscillator. When using an external clock signal instead of a crystal oscillator, it becomes an input terminal of an external clock signal.

● OSCILLATOR CIRCUIT OUTPUT TERMINAL (XOUT)

A crystal oscillator is connected between XIN terminals (Pin 9). Please use opening, when you use an external clock signal instead of a crystal oscillator.

● OSCILLATOR CIRCUIT POWER SUPPLY TERMINAL (VDD2)

VDD2 is used for the main oscillator circuit, and VDD1 is used for the output stage of an oscillator circuit level shifter. Please set the voltage of VDD2 less than VDD1 (VDD2 =< VDD1). The excitation level of an oscillator circuit can be downed by lower VDD2 voltage from VDD1. Please adjust VDD2 and do not exceed the maximum excitation electric power of the crystal oscillator to be used.



● OSCILLATOR CIRCUIT BUFFER OUTPUT TERMINAL (XBO)

It is an inverter output terminal. This terminal must be high impedance. The square wave of the frequency selected by FSE is outputted. Although it can be used as a clock of an external device, the specification of an external device is checked enough in this case.

● CONTROL TERMINAL (FSE, BR)

1. OSCILLATOR CIRCUIT BUFFER OUTPUT FREQUENCY CHANGE TERMINAL (FSE)

About the frequency of the signal outputted from XBO, one of $f_x = 14.7456\text{MHz}$ and the $f_x/4 = 3.6864\text{MHz}$ is chosen.

FSE	Output frequency
Hi	3.6864MHz
Lo	14.7456MHz

2. TRANSMISSION SPEED CONTROL TERMINAL (BR)

It always sets to a logical high.

■ PARAMETER DESCRIPTION

SYMBOL	PARAMETER	TERMINAL	DESCRIPTION
I_{DD1}	Current Consumption in modulation and demodulation	VDD1, VDD2	Total current which flows into VDD1 and VDD2 terminals at the time of transceiver operation
I_{DD2}	Current Consumption in power down	VDD1, VDD2	Total current which flows into VDD1 and VDD2 terminals at the time of a transceiver power down
I_{DD3}	Current Consumption in only modulation	VDD1, VDD2	Total current which flows into VDD1 and VDD2 terminals at the time of transmitting operation
I_{DD4}	Current Consumption in only demodulation	VDD1, VDD2	Total current which flows into VDD1 and VDD2 terminals at the time of reception operation
V_{IH}	High level input voltage of control input terminal	All control terminals	High level voltage which is supplied to each control terminal.
V_{IL}	Low level input voltage of control input terminal	All control terminals	Low level voltage which is supplied to each control terminal
V_{HS}	Control hysteresis voltage width of input terminal	All control terminals	The voltage of the difference between the logical Low -> High and the High -> Low situations
V_{OL}	Low level output voltage of digital output terminal	TRD, RTM, RDT	Low level voltage outputted from each digital signal output terminal
V_{OH}	High level output voltage of digital output terminal	TRD, RTM, RDT	High level voltage outputted from each digital signal output terminal
I_i	Control input terminal current	All control terminals	It is outflow / inflow current to each control terminal
I_{IA}	Analog input terminal current	AIN	Current which flows into AIN terminal
V_{B1}	AGS terminal bias voltage	AGS	DC bias voltage of AGS terminal
V_{B2}	MX terminal bias voltage	MX	DC bias voltage of MX terminal
V_{OS1}	AGS terminal offset voltage	AGS	DC offset voltage of AGS terminal
V_{OS2}	MX terminal offset voltage	MX	DC offset voltage of MX terminal
G_O	Open-loop gain	AIN - AGS	Open gain of input buffer amplifier
f_T	Input buffer amplifier bandwidth	AIN - AGX	Frequency bandwidth of input buffer amplifier
V_{OM}	MX terminal modulating signal level	MX	Quasi-sine wave signal level outputted from MX terminal
E_{BR1}	Demodulation bit error rate1	RDT	BER (Bit Error Rate) of demodulation output data
E_{BR2}	Demodulation bit error rate2	RDT	BER of demodulation output data
E_{BR3}	Demodulation bit error rate3	RDT	BER of demodulation output data
N_{LH}	PLL Pull-in Bit 1	RTM	The number of bits until it pull in less than 22.5 phase difference at the time of a low-speed phase velocity setup
N_{LL}	PLL Pull-in Bit 2	RTM	The number of bits until it pull in less than 22.5 phase difference at the time of a high-speed phase velocity setup
D_F	The number of demodulation data synchronization gap bits	RTM	The gap with demodulation data and a PLL synchronized signal.
MXd	MX terminal modulating signal distortion	MX	Waveform distortion by the setting load conditions of the quasi-sine wave signal outputted from MX terminal
F_{CK}	Crystal oscillating frequency	XBO	Oscillating frequency accuracy of a crystal oscillator circuit
t_{DA}	Transmitting hold time		Refer to the timing chart.
t_{DS}	Data setup time		
t_{DH}	Data hold time		
t_{OM}	Modulation output delay time		
t_{FR}	Frame reset time		
t_{PU}	Power up time		
t_{TC}	Transmitting cycle time		
t_{RD}	Demodulation delay time		
t_{CY}	Receiving clock period		
t_{TH}	Receiving clock high level width		
t_{TL}	Receiving clock low level width		
t_{DD}	Data output delay time		
t_{PD}	Power down delay time		
t_{FR}	Frame reset time		

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VDD	7.0	V
Power Dissipation	P _D	375	mW
Input Voltage (Control)	V _{IND}	VSS - 0.5 to VDD1+0.5	V
Operating Temperature	T _{opr}	- 40 to + 105	°C
Storage Temperature	T _{stg}	- 40 to + 150	°C

Note: Please refer to the test circuit about Supply Voltage (VDD).

■ RECOMMENDED OPERATIONAL CONDITION

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage 1	VDD1	1.8	-	5.5	V
Supply Voltage 2	VDD2	1.8	-	VDD1	V

■ ELECTRICAL CHARACTERISTICS 1

(Ta = 25°C, VSS = 0V, Please refer to the test circuit, VDD=VDD1=VDD2=1.8V and R1 = 0Ω, unless otherwise noted)

[DC CHARACTERISTICS]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Consumption in modulation and demodulation	I _{DD1}	VDD=1.8V, No Signal	-	1.9	2.2	mA
Current Consumption in power down	I _{DD2}	VDD=1.8V, No Signal	-	0.01	10	uA
Current Consumption in only modulation	I _{DD3}	VDD=1.8V, No Signal	-	1.1	1.2	mA
Current Consumption in only demodulation	I _{DD4}	VDD=1.8V, No Signal	-	1.7	1.9	mA
Logical High Input Voltage	V _{IH}	VDD=1.8V, No Signal *NOTE2	0.75 x VDD	-	VDD	V
Logical Low Input Voltage	V _{IL}	VDD=1.8V, No Signal *NOTE2	VSS	-	0.25 x VDD	V
Hysteresis Width of Digital	V _{HS}	VDD=1.8V, No Signal *NOTE3	-	0.5	-	V
Logical Low Output Voltage	V _{OL}	VDD=1.8V, No Signal, I _o =-1.6mA *NOTE4	VSS	-	0.4	V

Logical High Output Voltage	V_{OH}	VDD=1.8V, No Signal, $I_o=+0.4mA$ *NOTE4	VDD - 0.4	-	VDD	V
Digital Input Leakage Current	I_I	VDD=1.8V, Other Input Pins are connected to VSS or VDD *NOTE2	-200	-	200	nA
Analog Input Leakage Current	I_{IA}	VDD=1.8V, No Signal, AIN Pin is connected to VSS or VDD	-100	-	100	nA
AGS Bias Voltage	V_{B1}	VDD=1.8V, No Signal *NOTE3	-	$0.39 \times VDD$	-	V
MX Bias Voltage	V_{B2}	VDD=1.8V, No Signal *NOTE3	-	0.9	-	V
AGS Offset Voltage	V_{OS1}	VDD=1.8V, No Signal, Criterion Voltage is $0.39 \times VDD$	-50	-	+50	mV
MX Offset Voltage	V_{OS2}	VDD=1.8V, No Signal, Criterion Voltage is 0.9 V	-150	-	+150	mV

*NOTE2: The measurement terminals are BR, FSE, PDTX, PDRX, TD, FRS, FRK, and PLLS.

*NOTE3: Please refer to the typical characteristics.

*NOTE4: The measurement terminals are TRD, RTM, and RDT

I_o shows input current of each pins, and negative value means output current.

[AC CHARACTERISTICS]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Open Loop Gain	G_O	VDD=1.8V, No load	60	-	-	dB
Frequency Bandwidth of Input Buffer Amplifier	f_T	VDD=1.8V, No load	0.8	1.0	-	MHz
Modulated Output at MX Pin	V_{OM}	VDD=1.8V, Load 30k Ω //50pF	-7	-6	-5	dBV
Demodulation Bit Error Rate 1	E_{BR1}	VDD=1.8V, PLLS=VSS, BR=VDD S/N=8dB, S= -2 to -32dBV N = Gaussian Noise (5 kHz), *NOTE3	-	1×10^{-3}	-	-
Demodulation Bit Error Rate 2	E_{BR2}	VDD=1.8V, PLLS=VSS, BR=VDD S/N=10dB, S= -2 to -32dBV N = Gaussian Noise (5 kHz), *NOTE3	-	5×10^{-5}	-	-
Demodulation Bit Error Rate 3	E_{BR3}	VDD=1.8V, PLLS=VSS, BR=VDD S/N=6dB, S= -20dBV N = Gaussian Noise (5 kHz),	-	-	5×10^{-2}	-
PLL Pull-in Bit 1	N_{LH}	VDD=1.8V, PLLS=VSS, Less than 22.5deg phase shift	-	-	12	bit
PLL Pull-in Bit 2	N_{LL}	VDD=1.8V, PLLS=VDD, Less than 22.5deg phase shift	-	-	50	bit
Decoding Reference Frequency Tolerance	D_F	VDD=1.8V, PLLS=VDD or VSS *NOTE3	-	2.4	-	%
Modulation Distortion	MXd	VDD=1.8V, BR=VDD, TD=VDD, Load=30k Ω // 50pF	-	1.5	3	%
Crystal Oscillator Frequency	F_{CK}	VDD=1.8V, No Signal	14.7440	14.7456	14.7472	MHz

*NOTE3: Please refer to the typical characteristics.

[TIMING CHARACTERISTICS]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit Hold Time	t_{DA}	VDD=1.8V, BR=VDD *NOTE3	-	400	-	us
Data Set Up Time	t_{DS}	VDD=1.8V, BR=VDD *NOTE3	-	416.7	-	ns
Data Hold Time	t_{DH}	VDD=1.8V, BR=VDD *NOTE3	-	416.7	-	ns
Demodulation Output Delay Time	t_{OM}	VDD=1.8V, BR=VDD	-	-	300	us
Frame Reset Time	t_{FR}	VDD=1.8V, BR=VDD	1	-	-	us
Power Up Time	t_{PU}	VDD=1.8V, BR=VDD	0.04	-	2.00	ms
Transmit Cycle Time	t_{TC}	VDD=1.8V, BR=VDD	833	-	834	us
Demodulation Delay Time	t_{RD}	VDD=1.8V, BR=VDD	-	-	2	ms
Receive Clock Cycle	t_{CY}	VDD=1.8V, BR=VDD	755	-	912	us
Receive Clock High Level Width	t_{TH}	VDD=1.8V, BR=VDD	416	-	417	us
Receive Clock Low Level Width	t_{TL}	VDD=1.8V, BR=VDD	338	-	496	us
Data Output Delay Time	t_{DD}	VDD=1.8V, BR=VDD	-	-	50	ns
Power Down Delay Time	t_{PD}	VDD=1.8V, BR=VDD	-	-	200	ns

*NOTE3: Please refer to the typical characteristics.

■ ELECTRICAL CHARACTERISTICS 2

(Ta = -40 or +105°C, VSS = 0V, Please refer to the test circuit, VDD=1.8V and R1=0Ω unless otherwise noted)

[DC CHARACTERISTICS]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Consumption in modulation and demodulation	I _{DD1}	VDD=1.8V, No Signal	-	-	2.2	mA
Current Consumption in power down	I _{DD2}	VDD=1.8V, No Signal	-	-	10	uA
Current Consumption in only modulation	I _{DD3}	VDD=1.8V, No Signal	-	-	1.2	mA
Current Consumption in only demodulation	I _{DD4}	VDD=1.8V, No Signal	-	-	1.9	mA
Logical High Input Voltage	V _{IH}	VDD=1.8V, No Signal *NOTE2	0.75 x VDD	-	VDD	V
Logical Low Input Voltage	V _{IL}	VDD=1.8V, No Signal *NOTE2	VSS	-	0.25 x VDD	V
Logical Low Output Voltage	V _{OL}	VDD=1.8V, No Signal, I _o =-1.6mA *NOTE4	VSS	-	0.4	V
Logical High Output Voltage	V _{OH}	VDD=1.8V, No Signal, I _o =+0.4mA *NOTE4	VDD - 0.4	-	VDD	V
Digital Input Leakage Current	I _I	VDD=1.8V, Other Input Pins are connected to VSS or VDD *NOTE2	-200	-	200	nA
Analog Input Leakage Current	I _{IA}	VDD=1.8V, No Signal, AIN Pin is connected to VSS or VDD	-100	-	100	nA
AGS Pin Offset Voltage	V _{OS1}	VDD=1.8V, No Signal, Reference Voltage= 0.39 x VDD	-50	-	+50	mV
MX Pin Offset Voltage	V _{OS2}	VDD=1.8V, No Signal Reference Voltage=0.9V	-150	-	+150	mV

*NOTE2: The measurement terminals are BR, FSE, PDTX, PDRX, TD, FRS, FRK, and PLLS.

*NOTE4: The measurement terminals are TRD, RTM, and RDT

I_o shows input current of each pins, and negative value means output current.

[AC CHARACTERISTICS]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Open Loop Gain	G_O	VDD=1.8V, No load	60	-	-	dB
Frequency Bandwidth of Signal Amplifier	f_T	VDD=1.8V, No load	0.8	-	-	MHz
Modulated Output at MX Pin	V_{OM}	VDD=1.8V, Load 30k Ω //50pF	-7	-	-5	dBV
Demodulation Bit Error Rate 3	E_{BR3}	VDD=1.8V, PLLS=VSS, BR=VDD S/N=6dB, S= -20dBV N = Gaussian Noise (5 kHz),	-	-	5×10^{-2}	-
PLL Pull-in Bit 1	N_{LH}	VDD=1.8V, PLLS=VSS, Less than 22.5deg phase shift	-	-	12	bit
PLL Pull-in Bit 2	N_{LL}	VDD=1.8V, PLLS=VDD, Less than 22.5deg phase shift	-	-	50	bit
Modulation Distortion	MXd	VDD=1.8V, BR=VDD, TD=VDD, LOAD=30k Ω // 50pF	-	-	3	%
Crystal Oscillator Frequency	F_{CK}	VDD=1.8V, No Signal	14.7440	-	14.7472	MHz

[TIMING CHARACTERISTICS]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulation Output Delay Time	t_{OM}	VDD=1.8V, BR=VDD	-	-	300	us
Frame Reset Time	t_{FR}	VDD=1.8V, BR=VDD	1	-	-	us
Power Up Time	t_{PU}	VDD=1.8V, BR=VDD	0.04	-	2.00	ms
Transmit Cycle Time	t_{TC}	VDD=1.8V, BR=VDD	833	-	834	us
Demodulation Delay Time	t_{RD}	VDD=1.8V, BR=VDD	-	-	2	ms
Receive Clock Cycle	t_{CY}	VDD=1.8V, BR=VDD	755	-	912	us
Receive Clock High Level Width	t_{TH}	VDD=1.8V, BR=VDD	416	-	417	us
Receive Clock Low Level Width	t_{TL}	VDD=1.8V, BR=VDD	338	-	496	us
Data Output Delay Time	t_{DD}	VDD=1.8V, BR=VDD	-	-	50	ns
Power Down Delay Time	t_{PD}	VDD=1.8V, BR=VDD	-	-	200	ns

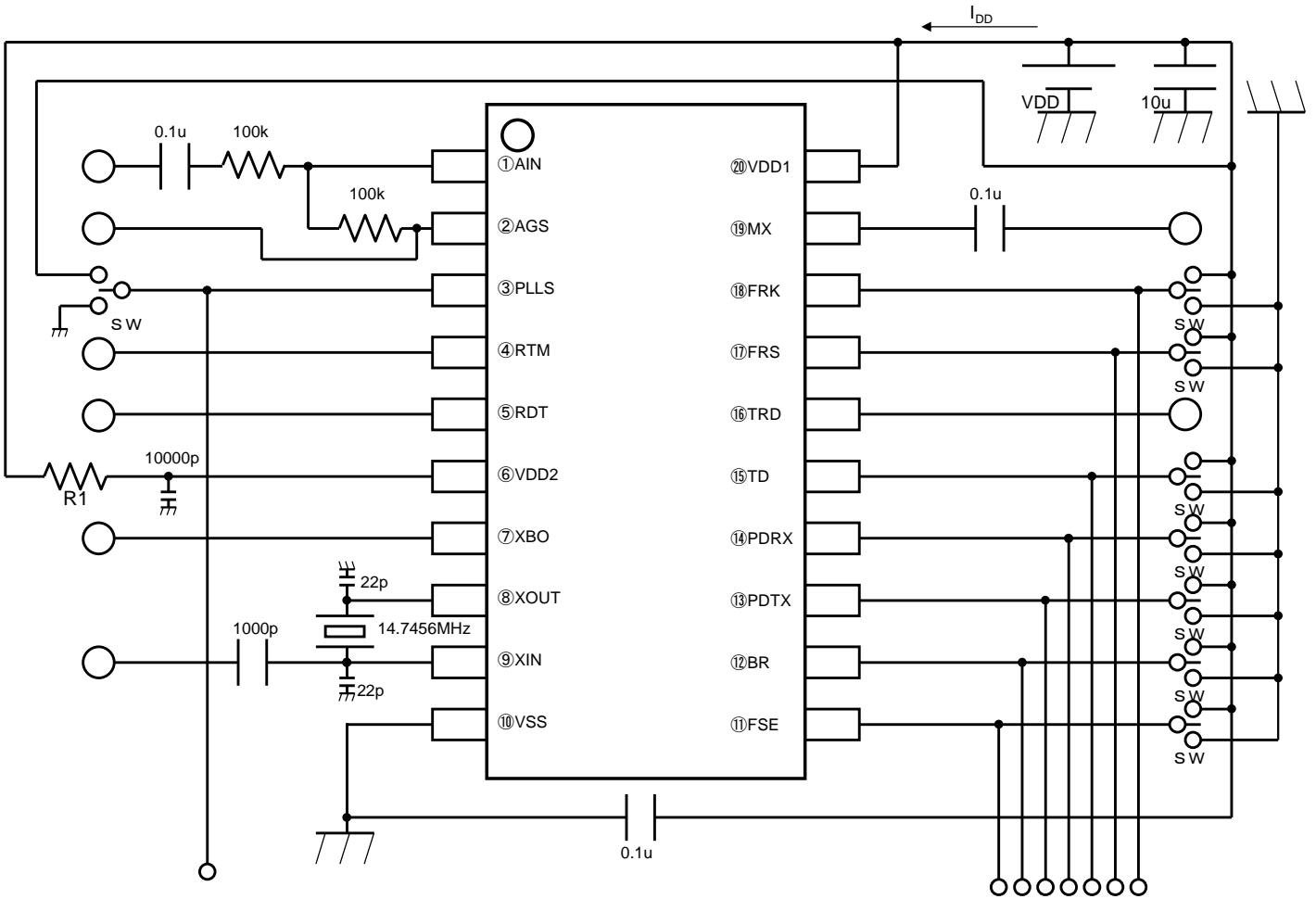
■ Terminal conditions when measuring

PARAMETER	SYMBOL	Terminal conditions: Pin Name (Pin No.)								Note
		PLLS (3)	FSE (11)	BR (12)	PDTX (13)	PDRX (14)	TD (15)	FRS (17)	FRK (18)	
Current Consumption in modulation and demodulation	I _{DD1}	Lo	Lo	Hi	Hi	Hi	Lo	Hi	Hi	
Current Consumption in power down	I _{DD2}	Lo	Lo	Hi	Lo	Lo	Lo	Hi	Hi	
Current Consumption in only modulation	I _{DD3}	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Hi	
Current Consumption in only demodulation	I _{DD4}	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Hi	
PLLS Pin Logical High/Low Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Hi/Lo	Lo	Hi	Lo	Hi	*1)	Hi	Hi	*1) TD Pin input signal PLLS=Lo : (1,0,1,···12bit)+(frame pattern 1) + (1,0,1,···16bit) PLLS=Hi : (1,0,1,···50bit)+(frame pattern 1) + (1,0,1,···60bit)
FSE Pin Logical High/Low Input Voltage Digital Input Leakage Current Crystal Oscillator Frequency	V _{IH} , V _{IL} I _I F _{CK}	Lo	Hi/Lo	Hi	Hi	Hi	Lo	Hi	Hi	
BR Pin Logical High Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Lo	Lo	Hi	Hi	Hi	Lo	Hi	Hi	
PDTX Pin Logical High/Low Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Lo	Lo	Hi	Hi/Lo	Lo	Lo	Hi	Hi	
PDRX Pin Logical High/Low Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Lo	Lo	Hi	Hi	Hi/Lo	Lo	Hi	Hi	
TD Pin Logical High/Low Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Lo	Lo	Hi	Hi	Lo	Hi/Lo	Hi	Hi	
FRS Pin Logical High/Low Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Lo	Lo	Hi	Hi	Hi	*2)	Hi/Lo	Hi	*2) TD Pin input signal FRS=Lo : (1,0,1,···12bit)+(frame pattern 2) + (1 continuation) FRS=Hi : (1,0,1,···12bit)+(frame pattern 1) + (1 continuation)
FRK Logical High/Low Input Voltage Digital Input Leakage Current	V _{IH} , V _{IL} I _I	Lo	Lo	Hi	Hi	Hi	Hi	Hi	Hi/Lo	
Hysteresis Width of Digital	V _{HS}	-	-	-	-	-	-	-	-	V _{HS} = V _{OH} - V _{OL}
RTM Pin Logical High/Low Output Voltage	V _{OL} , V _{OH}	Lo	Lo	Hi	Lo	Hi	Hi	Hi	Lo	
RDT Pin Logical High/Low Output Voltage	V _{OL} , V _{OH}	Lo	Lo	Hi	Lo	Hi	Hi/Lo	Hi	Lo	
TRD Pin Logical High/Low Output Voltage	V _{OL} , V _{OH}	Lo	Lo	Hi	Hi	Lo	Hi	Hi	Lo	
Analog Input Leakage Current	I _{IA}	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Hi	
AGS Pin Bias Voltage Offset Voltage	V _{B1} V _{OS1}	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Hi	
MX Pin Bias Voltage Offset Voltage	V _{B2} V _{OS2}	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Hi	
Open Loop Gain	G _O	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Hi	
Frequency Bandwidth of Input Buffer Amplifier	F _T	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Hi	
MX Pin Modulated Output	V _{OM}	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Hi	
Demodulation Bit Error Rate 1	E _{BR1}	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Lo	
PLL Pull-in Bit 1	N _{LH}	Lo	Lo	Hi	Lo	Hi	*1)	Hi	Hi	*1) TD Pin input signal
PLL Pull-in Bit 2	N _{LL}	Hi	Lo	Hi	Lo	Hi	*1)	Hi	Hi	PLLS=Lo : (1,0,1,···12bit)+(frame pattern 1) + (1,0,1,···16bit) PLLS=Hi : (1,0,1,···50bit)+(frame pattern 1) + (1,0,1,···60bit)
Decoding Reference Frequency Tolerance	D _F	Lo	Lo	Hi	Lo	Hi	*1)	Hi	Hi	
Modulation Distortion	MXd	Lo	Lo	Hi	Hi	Lo	Hi	Hi	Hi	
Transmit Hold Time	t _{DA}									
Data Set Up Time	t _{DS}									
Data Hold Time	t _{DH}									
Demodulation Output Delay Time	t _{OM}	Hi	Lo	Hi	*3)	Lo	*3)	Hi	Hi	*3) Refer to the MSK modulation timing chart.
Frame Reset Time	t _{FR}									
Power Up Time	t _{PU}									
Transmit Cycle Time	t _{TC}									
Demodulation Delay Time	t _{RD}									
Receive Clock Cycle	t _{CY}									
Receive Clock High/Low Level Width	t _{TH} , t _{TL}	Lo	Lo	Hi	Hi	*4)	Lo	Lo	Lo	*4) Refer to the MSK demodulation timing chart.
Data Output Delay Time	t _{DD}									
Power Down Delay Time	t _{PD}									
Frame Reset Time	t _{FR}									
Demodulation Bit Error Rate 3	E _{BR3}	Lo	Lo	Hi	Lo	Hi	Lo	Hi	Lo	

*NOTE5: The conditions of Hi ("1") level and Lo ("0") level
 $0.75 \times V_{DD} \leq \text{Hi ("1")} \leq V_{DD}$
 $V_{SS} \leq \text{Lo ("0")} \leq 0.25 \times V_{DD}$

*NOTE6: frame pattern 1 = 1,1,0,0,0,1,0,0,1,1,0,1,0,1,1,0 (C4D6H)
 frame pattern 2 = 1,0,0,1,0,0,1,1,0,0,1,1,0,1,1,0 (9336H)

■ TEST CIRCUIT



*NOTE7: R1

R1 must be set to the value in range of the maximum excitation electric power of the crystal oscillator to be used. The test circuit is set as follows:

- Crystal Oscillator: NX4025DA (U-816-78, NIHON DEMPA KOGYO CO.,LTD.)
- R1 : VDD = 1.8V condition, R1 = 0Ω
VDD = 5.5V condition, R1 = 3kΩ

It checks with a crystal maker about the specification of a crystal oscillator.

■ TERMINAL FUNCTION

($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = V_{DD1} = V_{DD2} = 1.8\text{V}$, $R_1 = 0\Omega$)

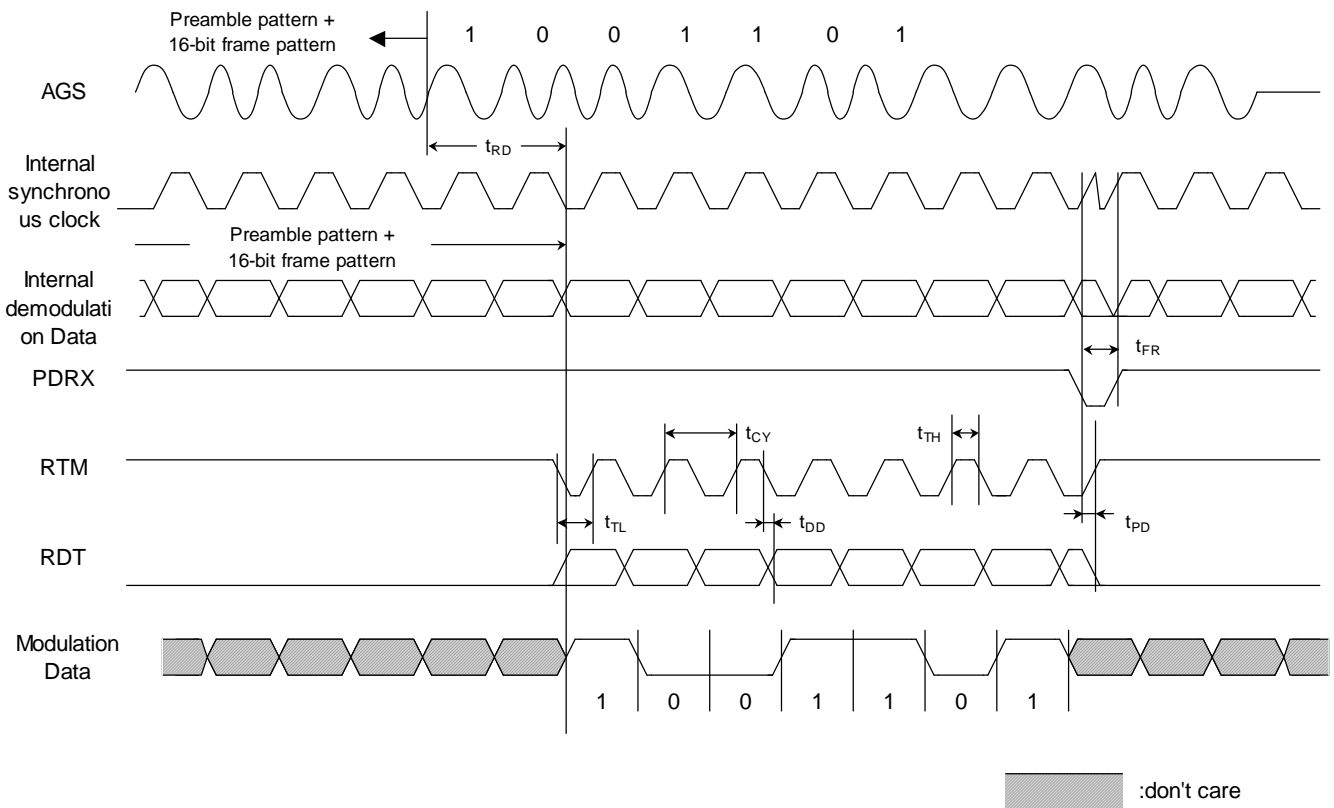
Pin	SYMBOL	Internal equivalent circuit	Terminal voltage	Remarks
1	AIN		-	<p>It is an input terminal of the input buffer amplifier. The gain of this amplifier is fixed by an external feedback resistor connected between this pin and Pin 2 for optimizing of BER (Bit Error Rate). Refer to the [demodulation bit error rate] of example of the characteristic for optimal level.</p>
2	AGS		$0.4 \times V_{DD1}$	<p>It is an output terminal of the input buffer amplifier. The gain of this amplifier is fixed by an external feedback resistor connected between this pin and Pin 1 for optimizing of BER (Bit Error Rate). Refer to the [demodulation bit error rate] of example of the characteristic for optimal level.</p>
3	PLLS		-	<p>It is a PLL control input terminal. It is a terminal which controls, the pull-in characteristic of PLL. The maximum phase correction angle High : Low-speed phase correction (3.75°) Low : High-speed phase correction (30°)</p>
4	RTM		V_{SS} to 0.4, V_{DD} to $V_{DD}-0.4$	<p>It is a MSK demodulation synchronous clock output terminal. The clock in sync with the digital data to which it restored outputs. Phase correction is applied to the clock generated by internal PLL, and a clock signal is reproduced.</p>
5	RDT			<p>It is a MSK demodulation data output terminal. The digital data to which it restored is outputted to a received signal. Data is outputted synchronizing with falling of Pin 4 signal.</p>

Pin	SYMBOL	Internal equivalent circuit	Terminal voltage	Remarks
6	VDD2		-	<p>It is an oscillator circuit power supply terminal. Please set VDD2 to one or less ($VDD2 \leq VDD1$) VDD. Please adjust VDD2 and do not exceed the maximum excitation electric power of the crystal oscillator to be used.</p>
7	XBO		VSS to VDD1	<p>It is an oscillator circuit buffer output terminal. The square wave of the frequency selected by Pin 11 is outputted. It can be used as a clock of an external device.</p>
8 9	XOUT XIN		VSS to VDD2	<p>Pin 8 is an oscillator circuit output terminal. Pin 9 is an oscillator circuit input terminal. A crystal oscillator is connected (Recommended). 14.7456 MHz should be used for the frequency of a crystal oscillator. When using an external clock signal instead of a crystal oscillator, please use a No. 9 pin as an input terminal, and the No. 8 pin should make it opening.</p>
10	VSS		-	It is a ground terminal.
11	FSE		-	It is a buffer output frequency change terminal. Pin 7 output frequency is chosen. High : Oscillating frequency Low : 1/4 of oscillating frequency
12	BR			It is a transmission speed control terminal. It always sets to High.
13	PDTX			It is a modulation block power down control terminal. High : Modulation circuit unit operational mode Low : Modulation circuit unit non-operational mode
14	PDRX			It is a demodulation block power down control terminal. High : Demodulating circuit operational mode Low : Demodulating circuit non-operational mode
15	TD			It is MSK modulation data input terminal. The modulation data are red with synchronized clocks signal of Pin 16.

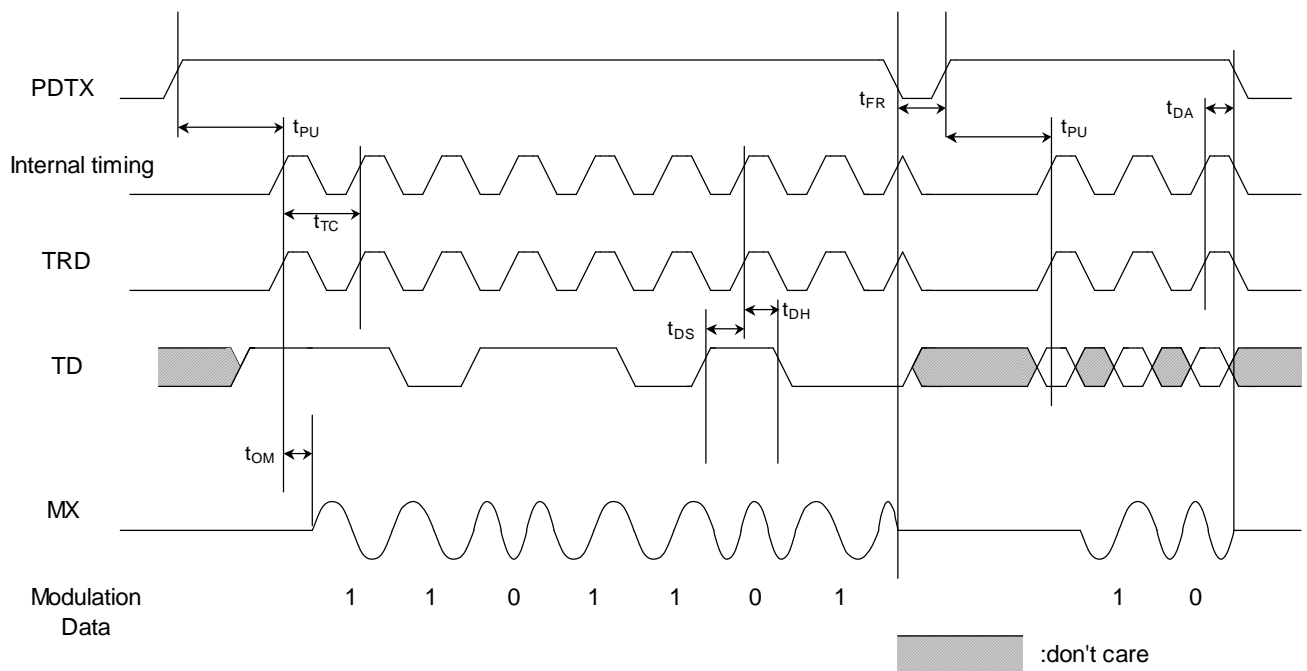
Pin	SYMBOL	Internal equivalent circuit	Terminal voltage	Remarks
16	TRD		VSS to 0.4, VDD to VDD-0.4	It is MSK modulation read data timing output terminal. A clock signal is outputted. The data of a No. 15 pin is red at rising edge of the clock signal.
17	FRS		-	It is a frame pattern selection input terminal. High : C4D6H Low : 9336H
18	FRK			It is a frame detection function selection terminal. High : a frame detection function -- enable Low : Frame detection function – disenable
19	MX		0.9V	It is a MSK modulating signal output terminal. The digital data taken in from the Pin 15 is changed into an analog signal, and is outputted (High: 1200Hz, Low: 1800 Hz). Output level - It is 6dBV. In order to remove the harmonics ingredient of a false sine wave generating circuit, it outputs through a secondary Bata Worth low pass filter.
20	VDD1		-	It is a power supply terminal. VDD2 is used for the main oscillating circuit unit, and VDD1 is used for the output stage and the other circuits of an oscillating circuit level shifter.

■ TIMING CHART

MSK demodulation timing chart



MSK modulation timing chart



■ TERMINAL OPERATION TIMING

PDTX: Transmitting (Modulating) block power down

Since PDTX serves as reset of an internal circuit, please set a PDTX terminal (Pin 13) to Low once for the prevention from malfunction at the time of power supply starting.

Since the MSK modulating signal currently outputted from MX terminal (Pin 19) stops if PDTX is changed to a logical low from a logical high, depending on the timing of PDTX, the last of a MSK modulating signal may be missing.

PDRX: Receiving (Demodulating) block power down

Since PDRX serves as reset of a frame detection circuit, when the state of the time of power supply starting, a FRK terminal (Pin 18), and a FRS terminal (Pin 17) is changed, please set a PDRX terminal (Pin 14) to Low once.

FRK: Selection of a frame detection function

At the time of the setting change of FRK, as shown in the following tables, it operates.

FRK (Selection of a frame detection function) OPERATION

FRK	At the time of frame detection completion	At the time of frame detection un-completing
Low(invalid) ->High (effective)	Stopping, RTW and RDT are output starts after frame detection.	
High (effective) -> Low(invalid)	RTW and RDT output continuously.	RTW and RDT start outputting.

FRS: Frame pattern selection

It operates as follows at the time of the setting change of FRS.

FRS (Frame pattern selection) OPERATION

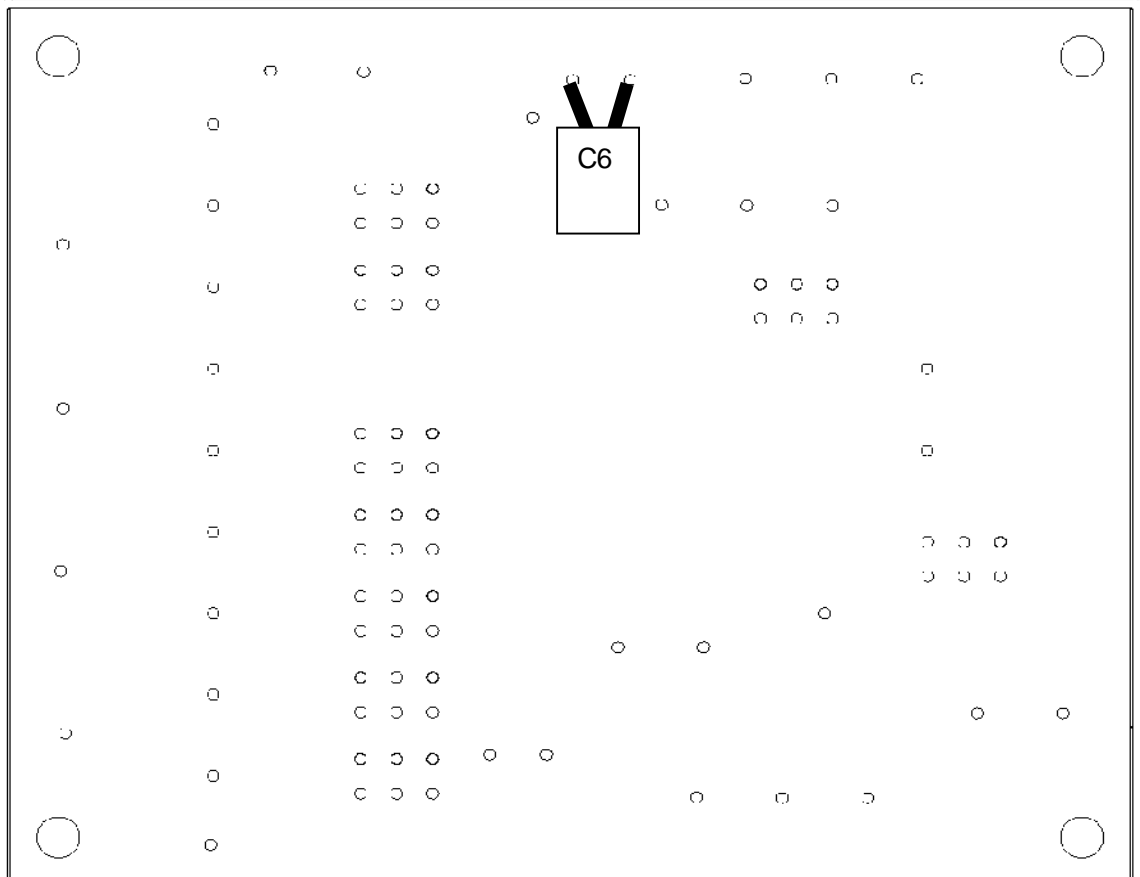
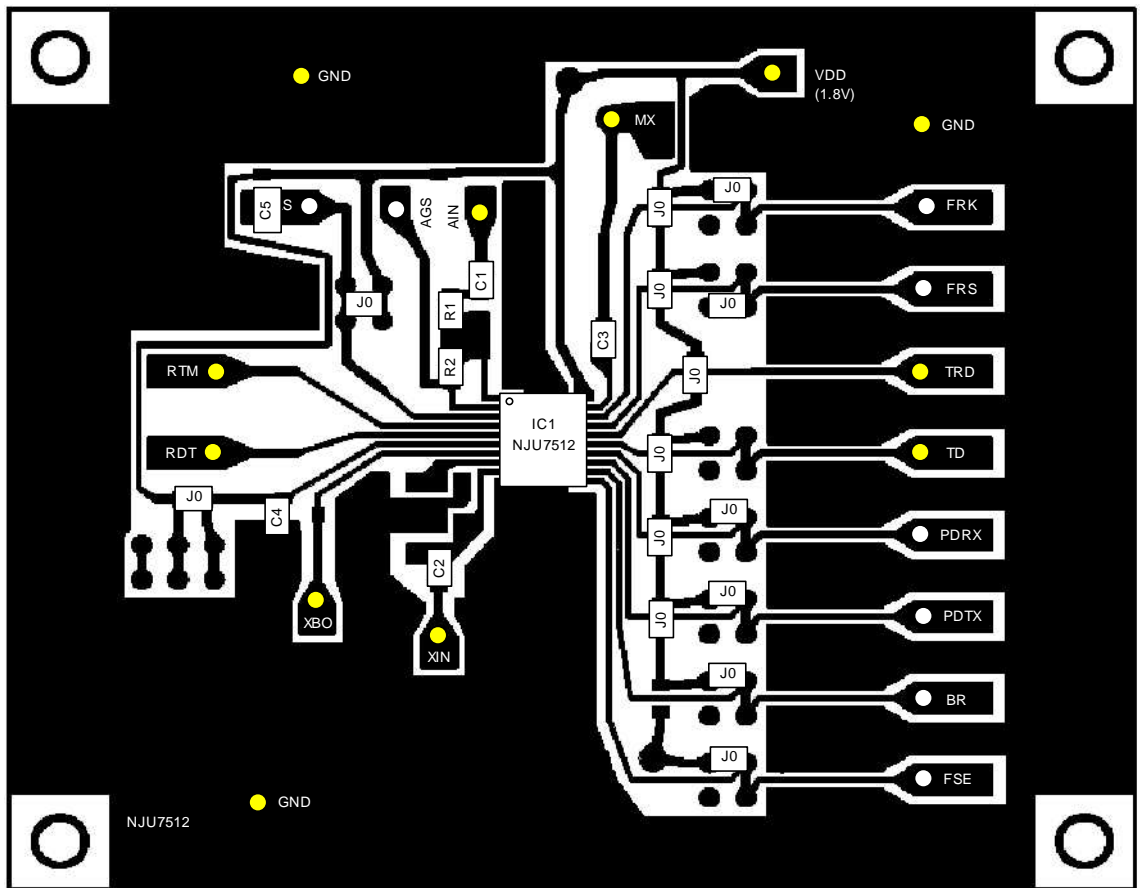
FRS	At the time of frame detection completion	At the time of frame detection un-completing
Low -> High, High -> Low	*NOTE15 RTW and RDT output continuously.	After detection of the frame data, RTW and RDT start outputting.

*NOTE8:

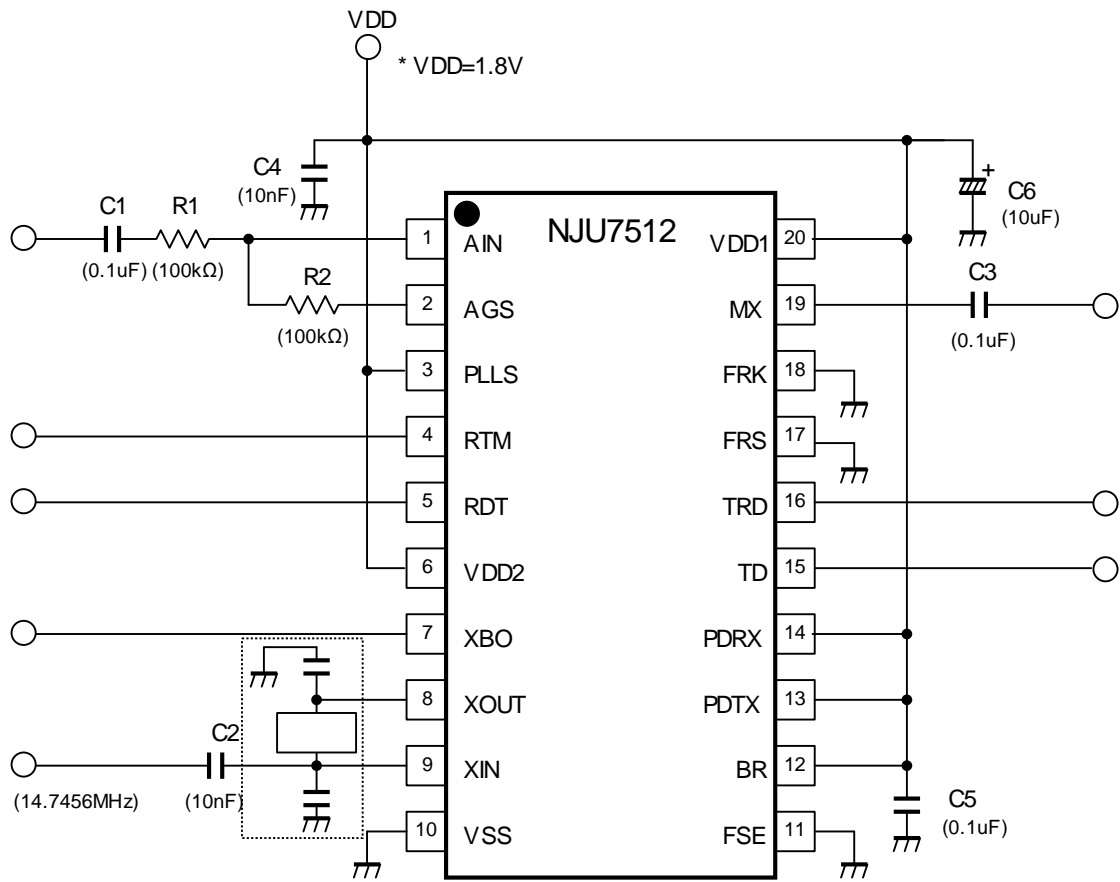
If a PDRX terminal (No. 14 pin) is set to Low once, RTM and RDT come to a halt. After frame pattern detection, RTM and RDT start outputting.

■ EVALUATION BOARD

● PCB Layout



● Circuit Diagram



*NOTE9: J0 on the evaluation board are chip jumpers (chip 0Ω register).

*NOTE10: An oscillator module (crystal and capacitor) isn't assembled on the shipped evaluation board from factory.

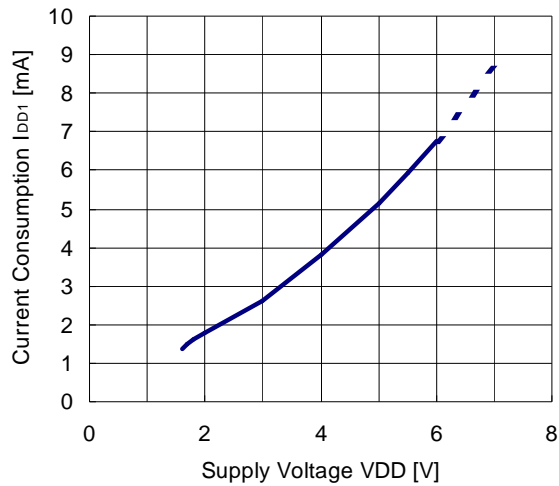
■ TYPICAL CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$, Please refer to the test circuit, $V_{DD} = V_{DD1} = V_{DD2} = 1.8\text{V}$ and $R_1 = 0\Omega$, unless otherwise noted)

[DC CHARACTERISTICS]

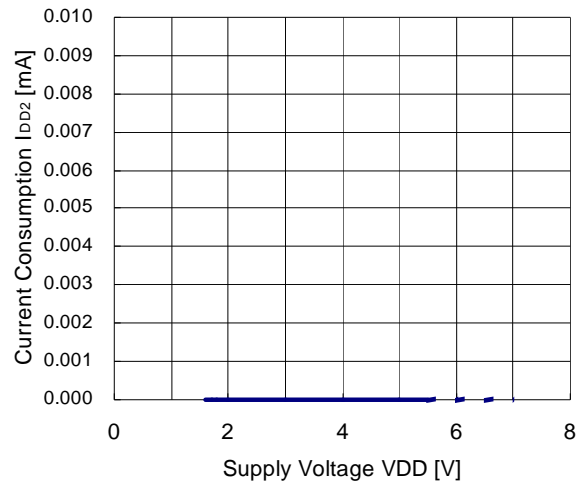
Current Consumption in mod. and demod.

($V_{DD1} - V_{DD2} : 0\Omega$, PLLS/FSE/FRS/FRK : VDD, BR/TD : VSS)



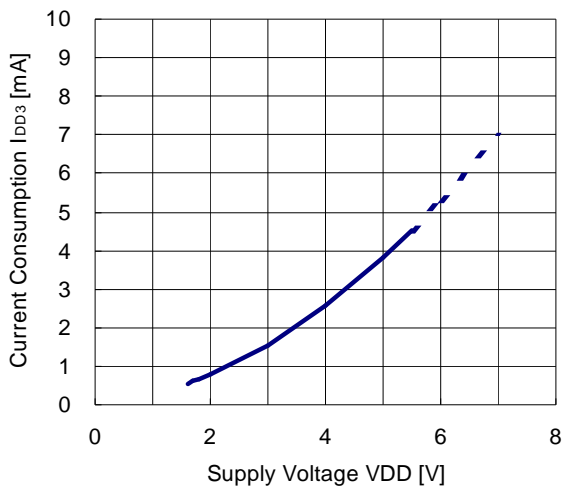
Current Consumption in power down

($V_{DD1} - V_{DD2} : 0\Omega$, PLLS/FSE/FRS/FRK : VDD, BR/TD : VSS)



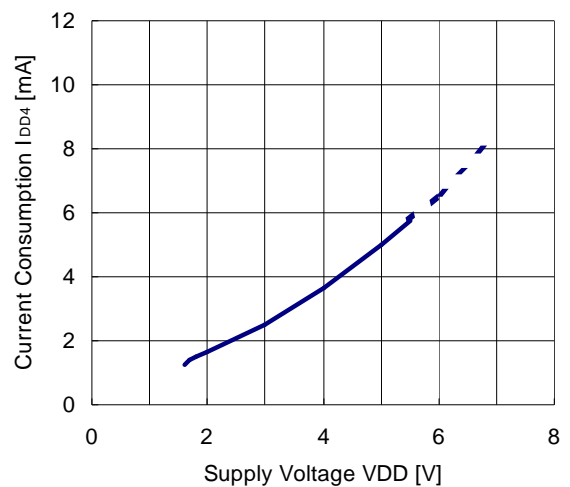
Current Consumption in only mod.

($V_{DD1} - V_{DD2} : 0\Omega$, PLLS/FSE/FRS/FRK : VDD, BR/TD : VSS)



Current Consumption in only demod.

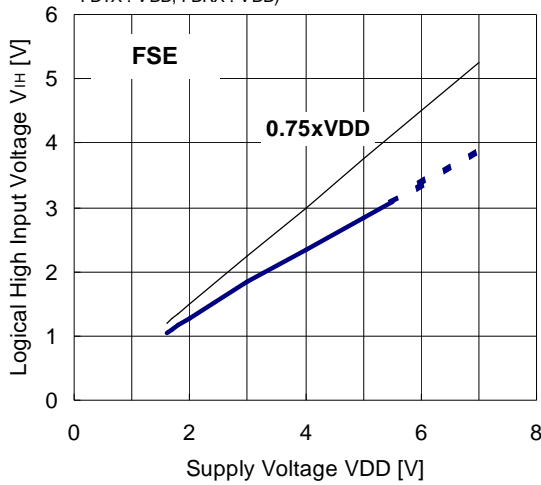
($V_{DD1} - V_{DD2} : 0\Omega$, PLLS/FSE/FRS/FRK : VDD, BR/TD : VSS)



[DC CHARACTERISTICS]

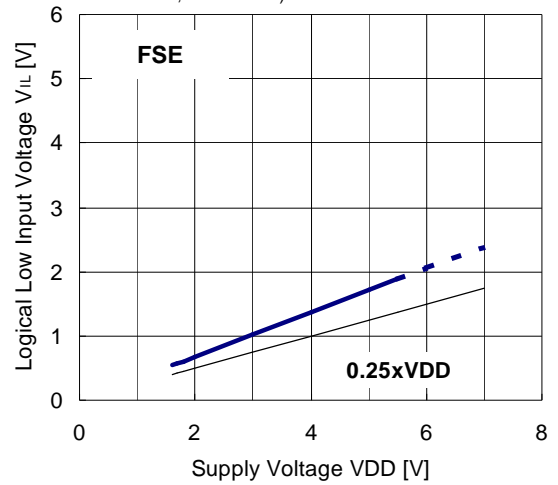
Logical High Input Voltage

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VDD, PDRX : VDD)



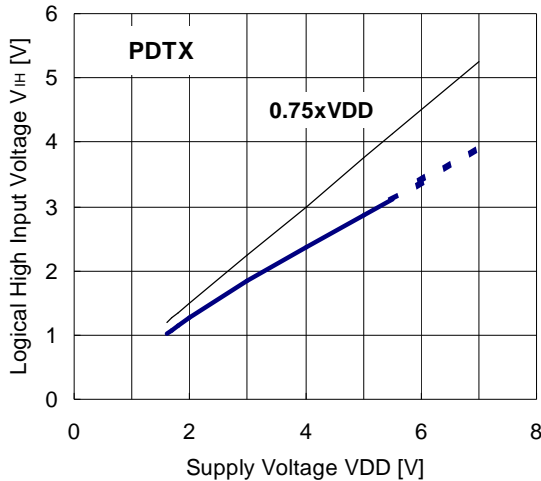
Logical Low Input Voltage

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VDD, PDRX : VDD)



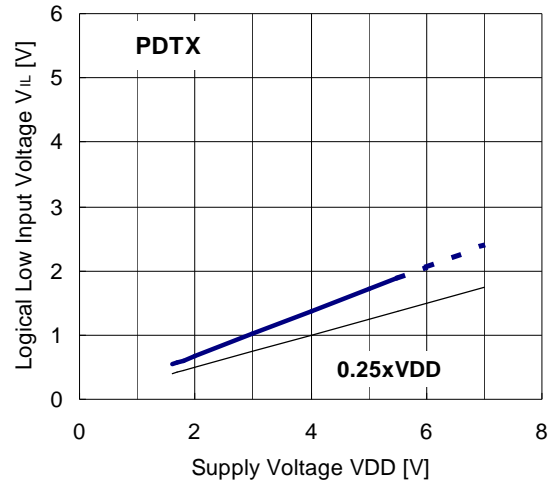
Logical High Input Voltage versus

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDRX : VSS)



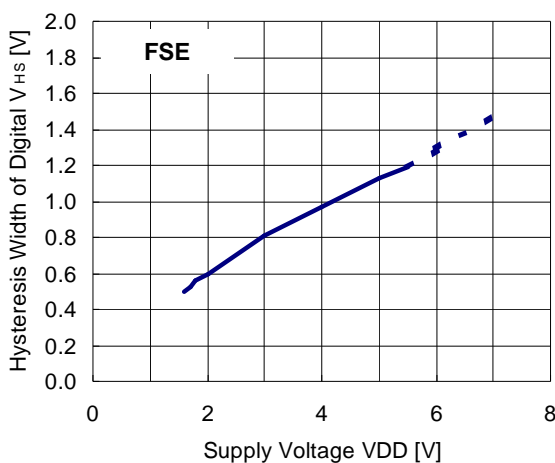
Logical Low Input Voltage

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDRX : VSS)



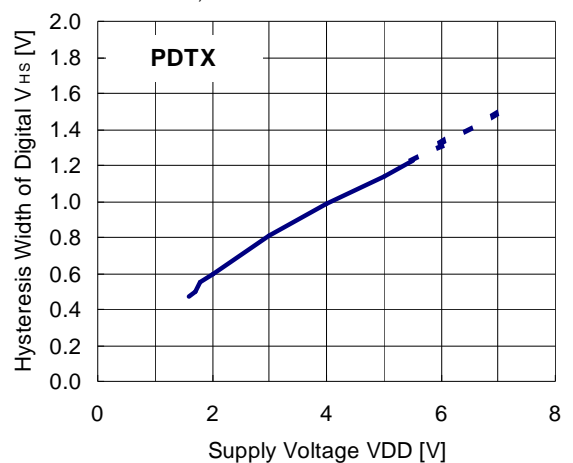
Hysteresis Width of Digital

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VDD, PDRX : VDD)



Hysteresis Width of Digital

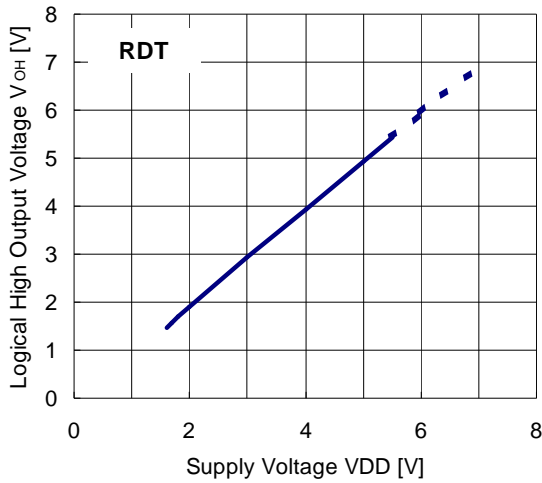
(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDRX : VSS)



[DC CHARACTERISTICS]

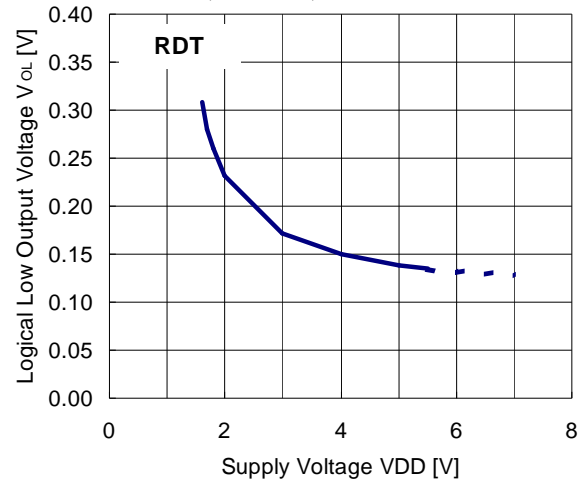
Logical High Output Voltage

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VDD, PDRX : VSS, I_o = 0.4mA



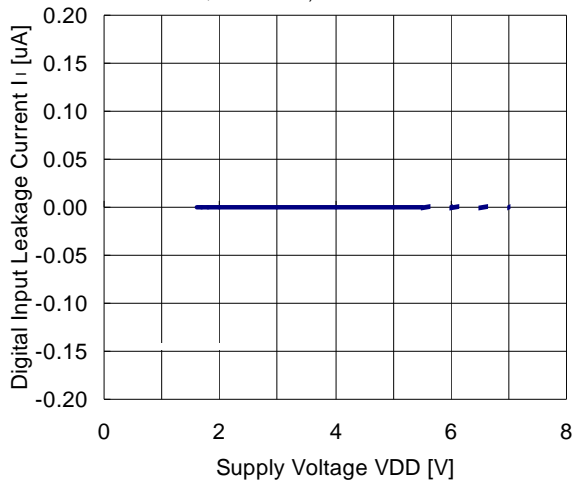
Logical Low Output Voltage

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VDD, PDRX : VSS, I_o = -1.6mA



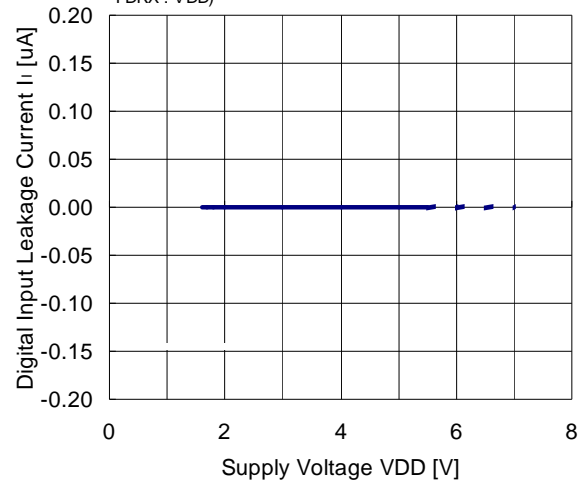
Digital Input Leakage Current

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VDD, PDRX : VSS)



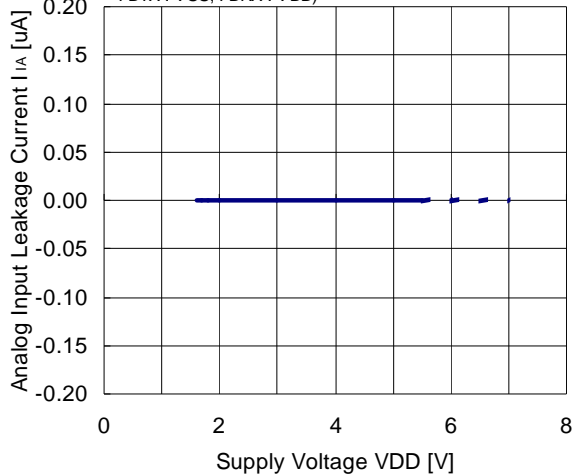
Digital Input Leakage Current

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDRX : VDD)



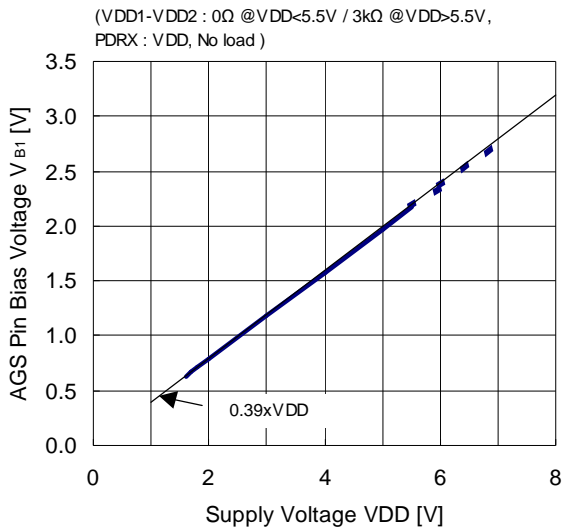
Analog Input Leakage Current

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD>5.5V,
PDTX : VSS, PDRX : VDD)

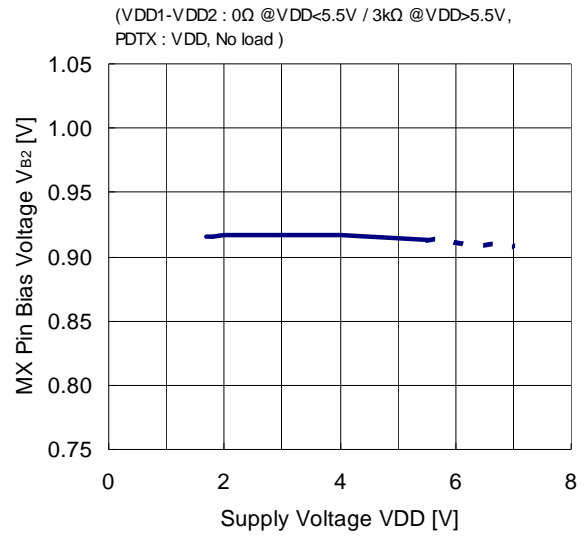


[DC CHARACTERISTICS]

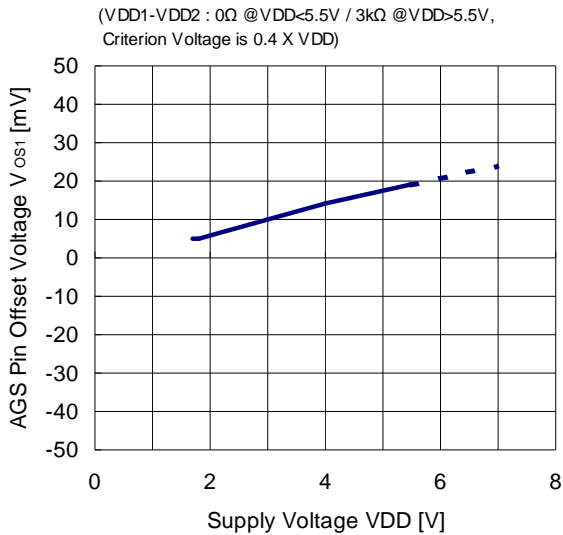
AGS Pin Bias Voltage



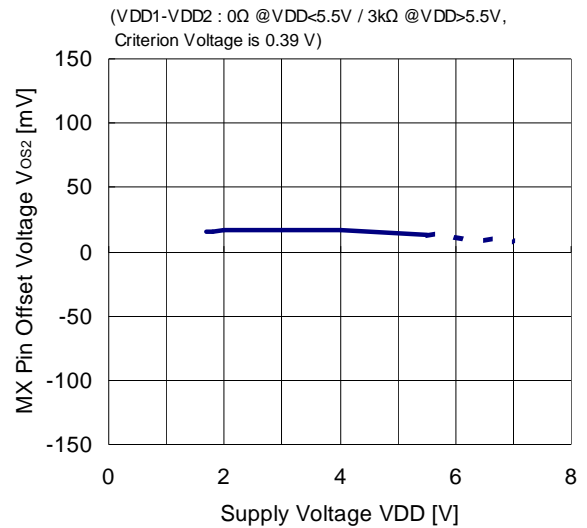
MX Pin Bias Voltage



AGS Pin Offset Voltage

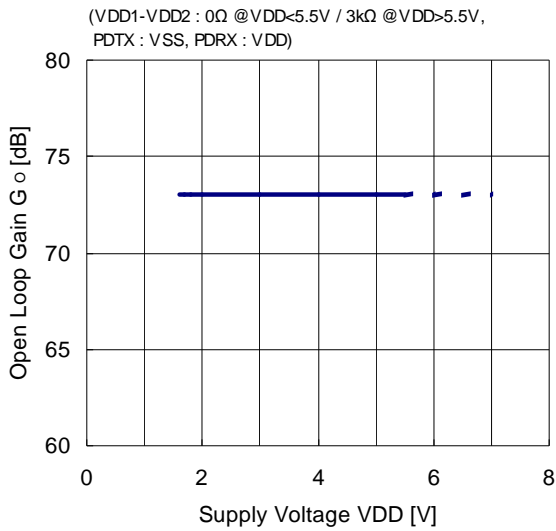


MX Pin Offset Voltage

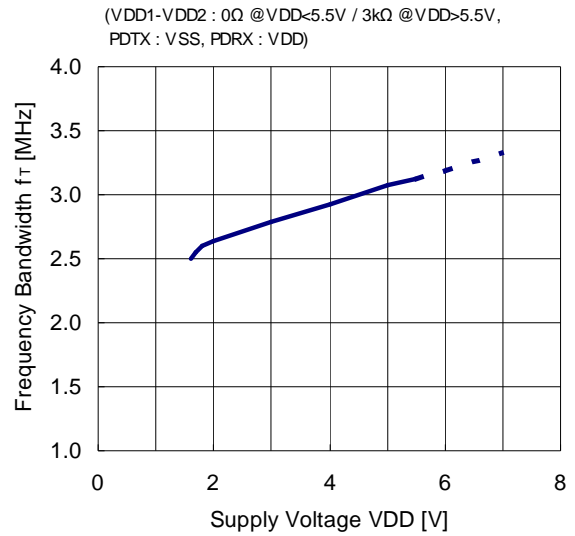


[AC CHARACTERISTICS] *For demodulation bit error rate, and described elsewhere.

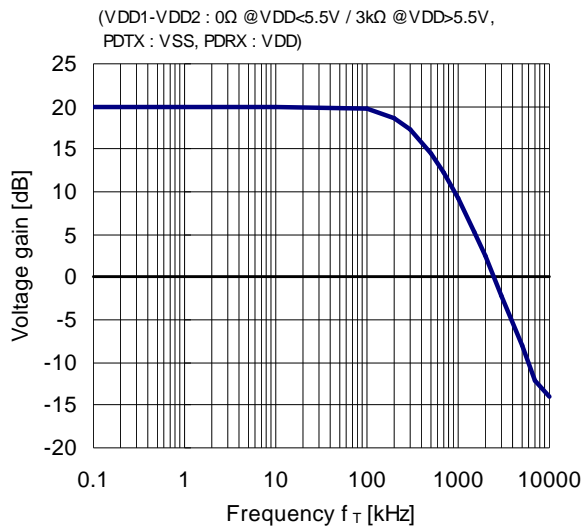
Open Loop Gain



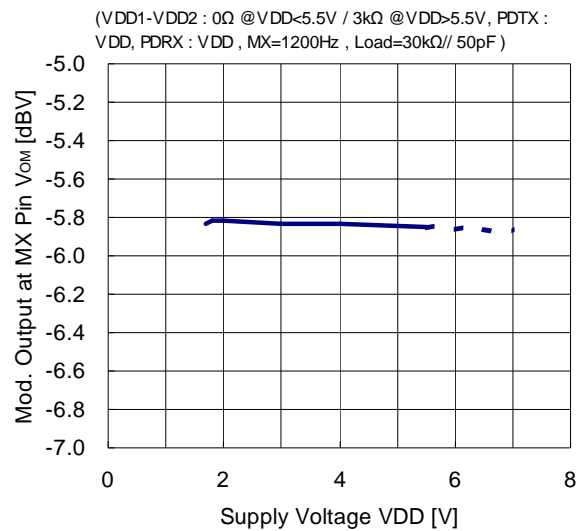
Frequency Bandwidth of Input Buffer Amplifier



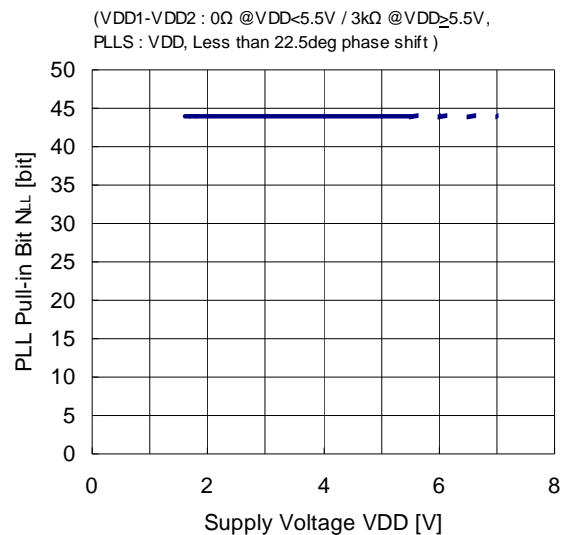
Frequency Bandwidth of Input Buffer Amplifier



Mod. Output at MX Pin

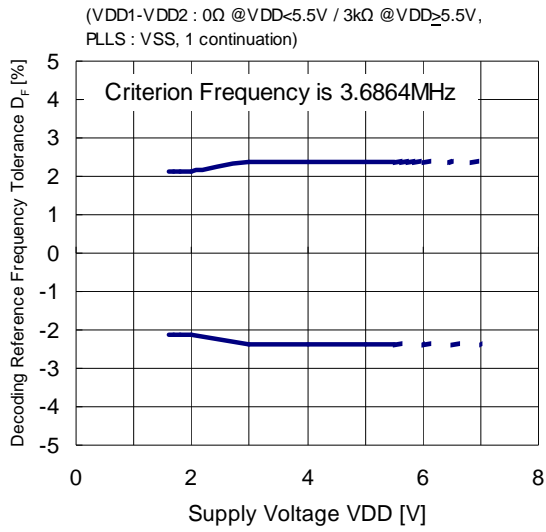


PLL Pull-in Bit 2

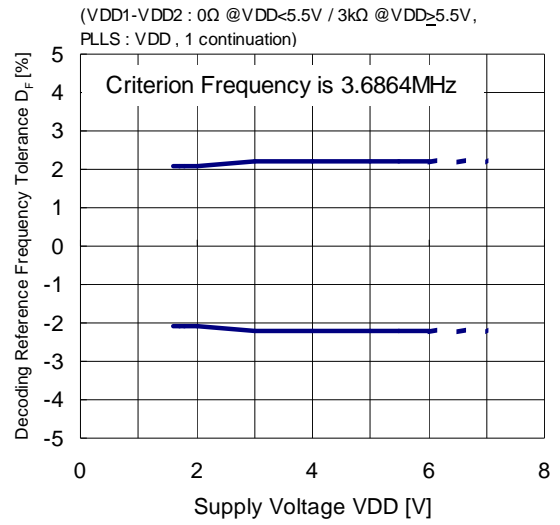


[AC CHARACTERISTICS] *For demodulation bit error rate, and described elsewhere.

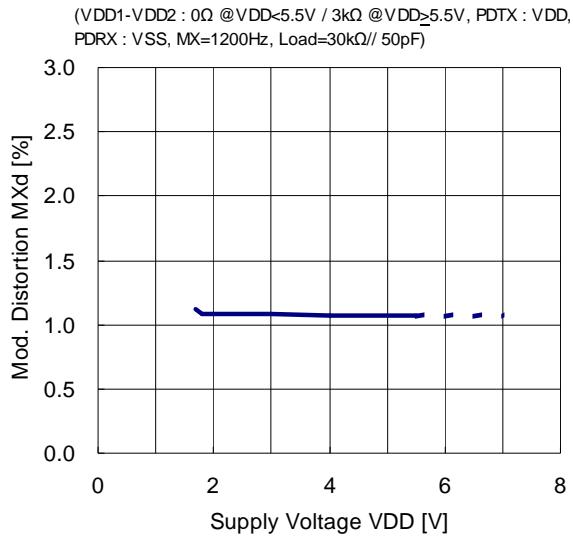
Decoding Reference Frequency Tolerance



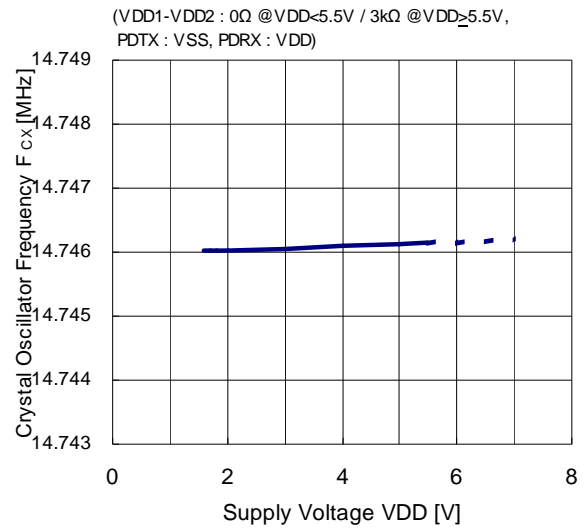
Decoding Reference Frequency Tolerance



Mod. Distortion

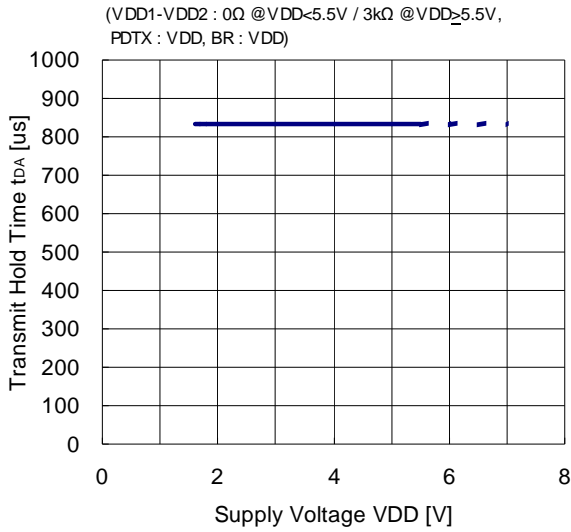


Crystal Oscillator Frequency

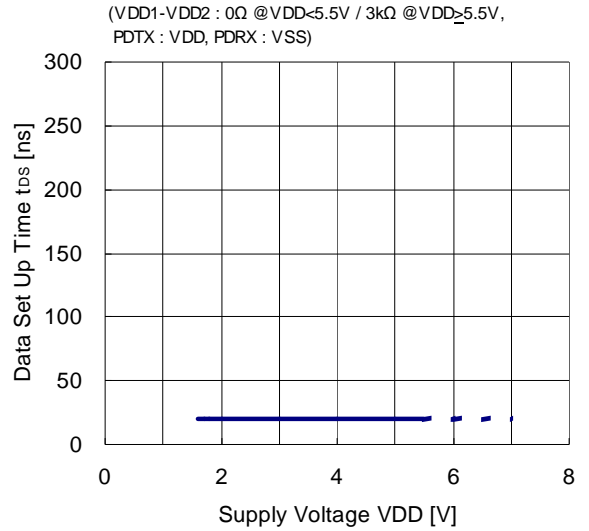


[TIMING CHARACTERISTICS]

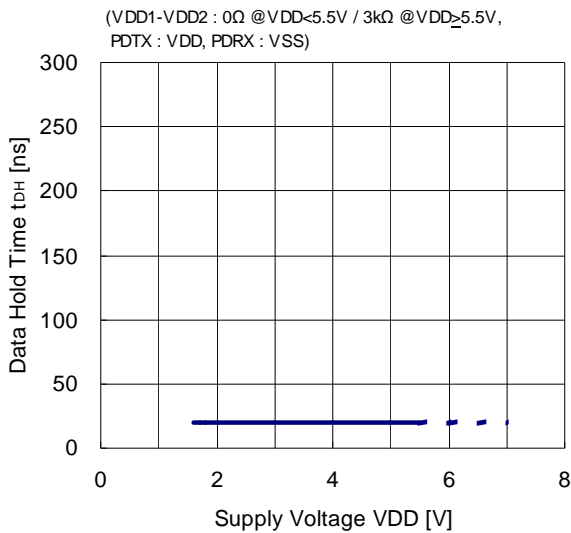
Transmit Hold Time



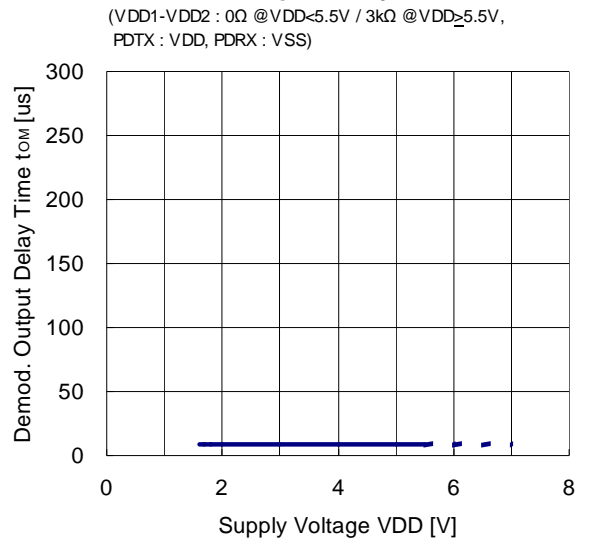
Data Set Up Time



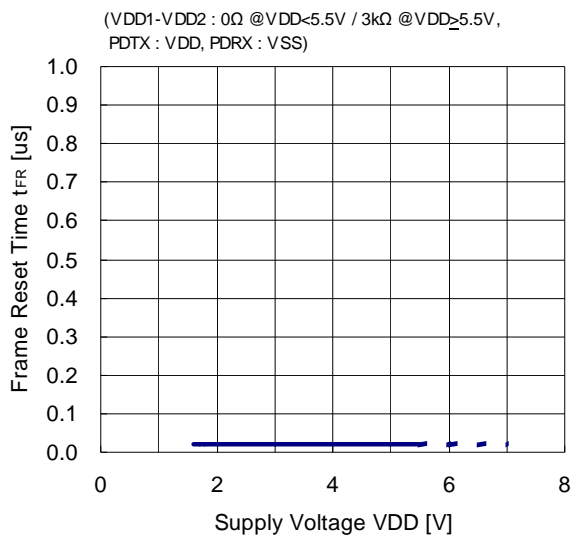
Data Hold Time



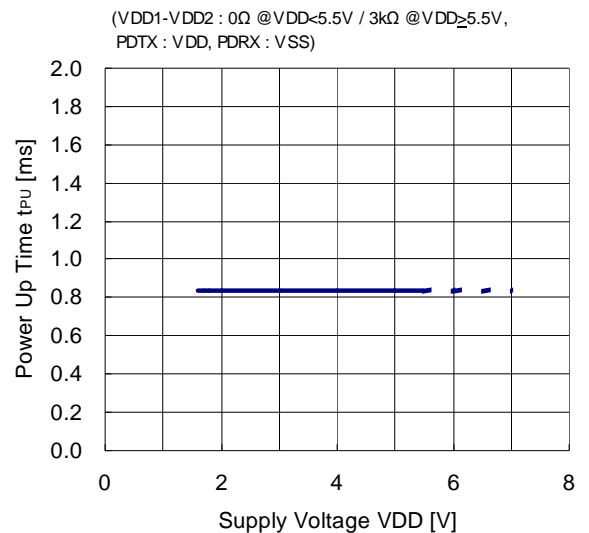
Demod. Output Delay Time



Frame Reset Time



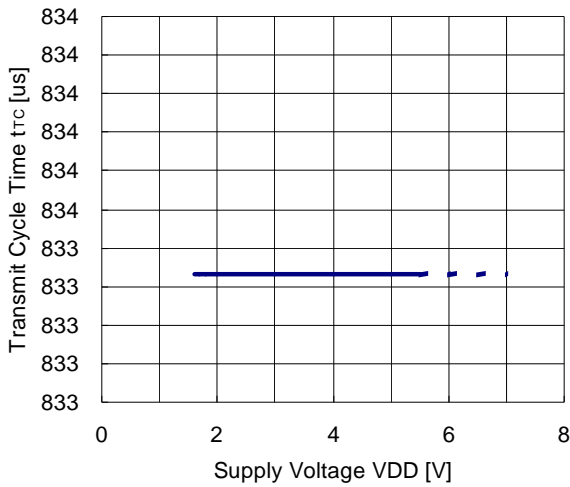
Power Up Time



[TIMING CHARACTERISTICS]

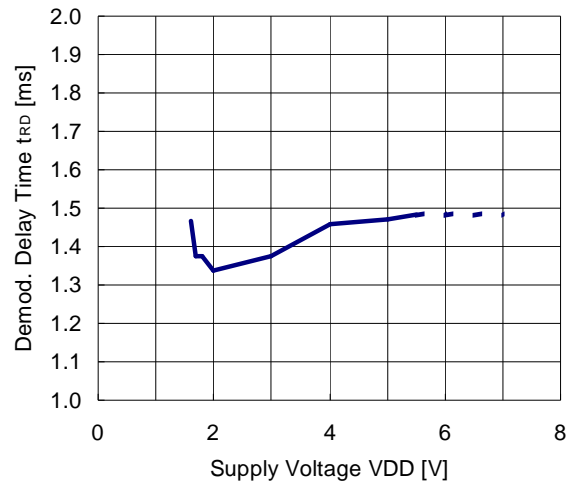
Transmit Cycle Time

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDTX : VDD, BR : VDD)



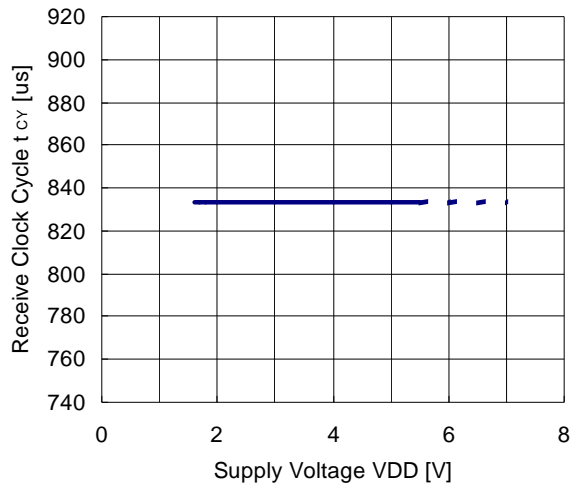
Demod. Delay Time

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDTX : VSS, PDRX : VDD)



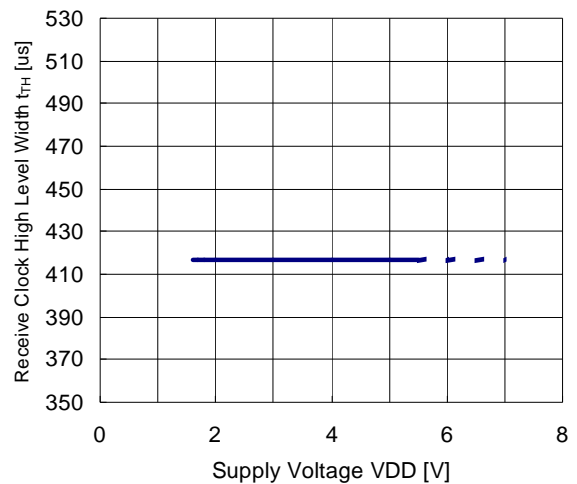
Receive Clock Cycle

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDTX : VDD, BR : VDD)



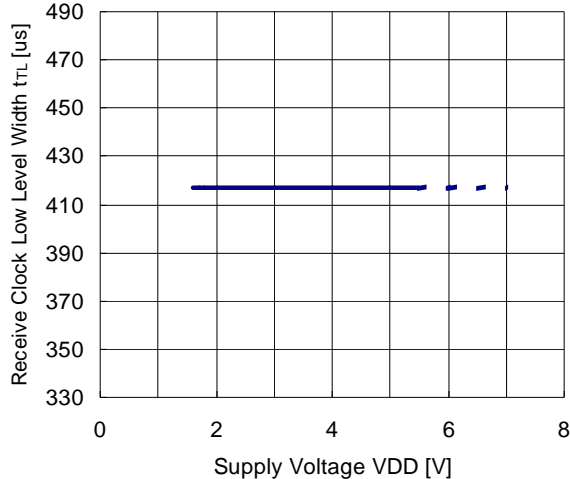
Receive Clock High Level Width

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDRX : VDD, BR : VDD)



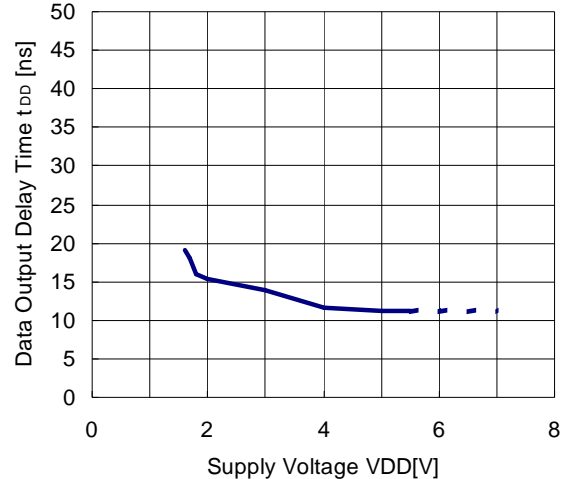
Receive Clock Low Level Width

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDRX : VDD, BR : VDD)



Data Output Delay Time

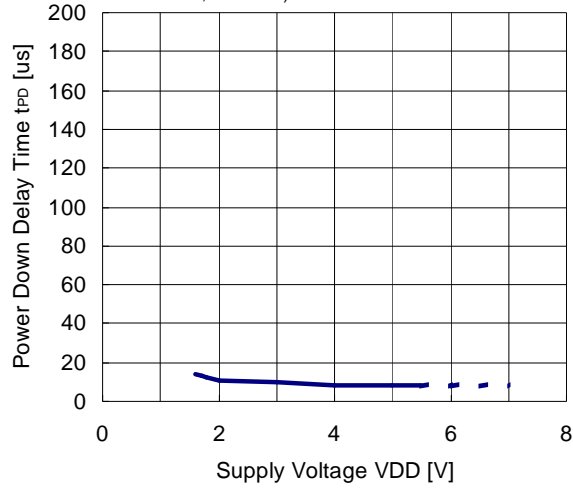
(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDRX : VDD, BR : VDD)



[TIMING CHARACTERISTICS]

Power Down Delay Time

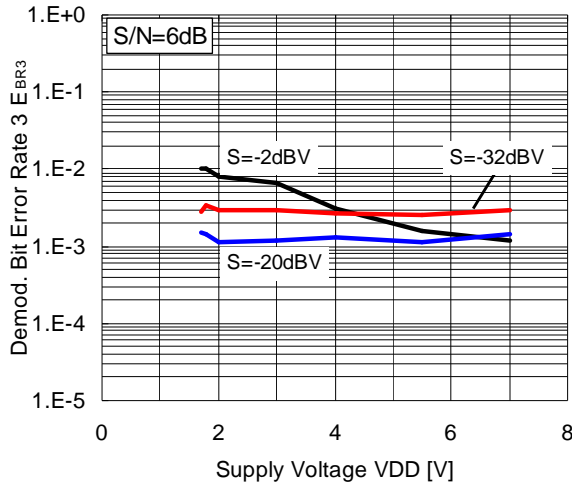
(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V,
PDRX : VDD, BR : VDD)



[Demodulation Bit Error Rate]

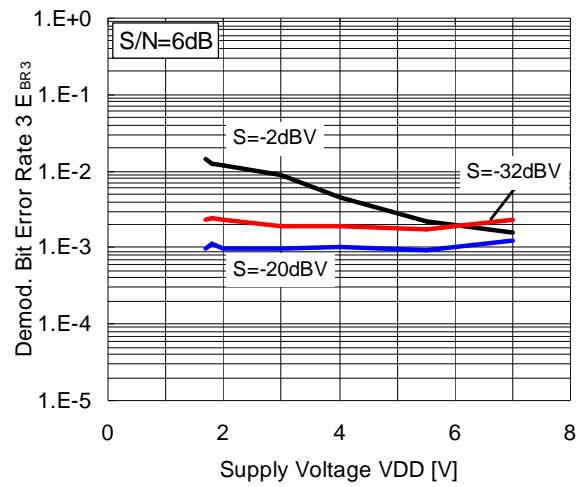
Demod. BER 3 versus Supply Voltage
PDRX:VDD, BR:VDD, PLLS:VDD

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V)



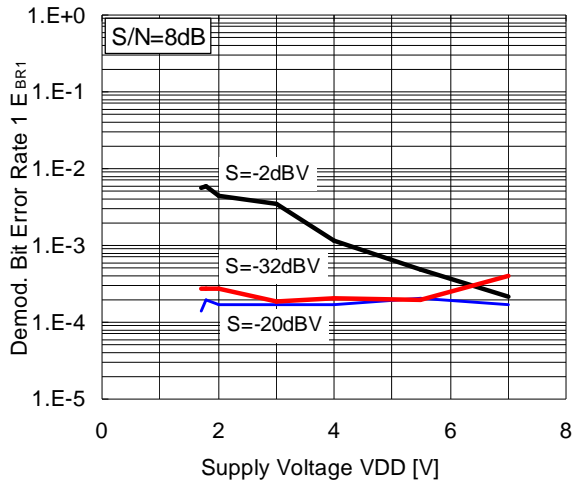
Demod. BER 3 versus Supply Voltage
PDRX:VDD, BR:VDD, PLLS:VSS

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V)



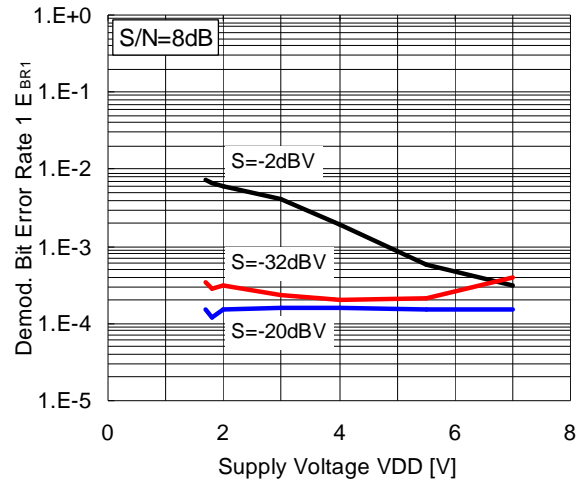
Demod. BER 1 versus Supply Voltage
PDRX:VDD, BR:VDD, PLLS:VDD

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V)



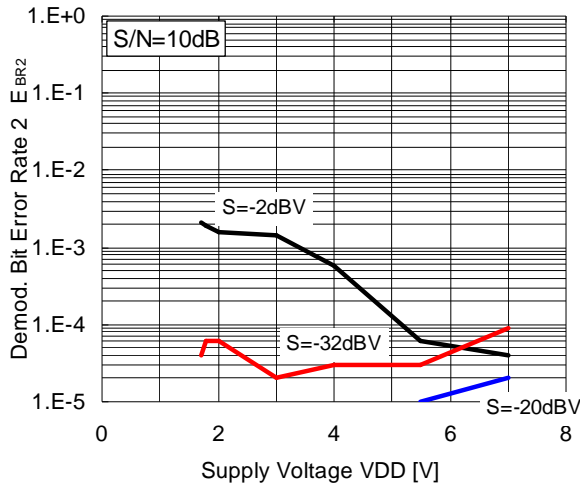
Demod. BER 1 versus Supply Voltage
PDRX:VDD, BR:VDD, PLLS:VSS

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V)



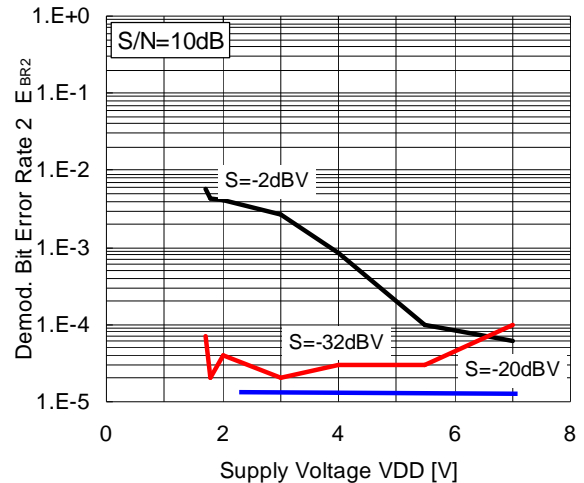
Demod. BER 2 versus Supply Voltage
PDRX:VDD, BR:VDD, PLLS:VDD

(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V)



Demod. BER 2 versus Supply Voltage
PDRX:VDD, BR:VDD, PLLS:VSS

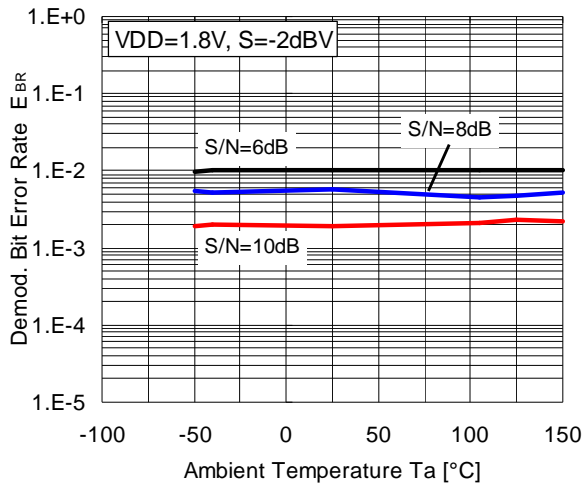
(VDD1-VDD2 : 0Ω @VDD<5.5V / 3kΩ @VDD≥5.5V)



[Demodulation Bit Error Rate]

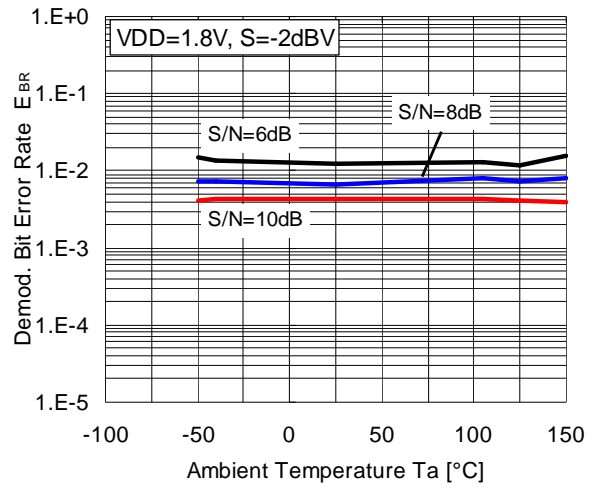
Demod. BER versus Temperature
PDRX:VDD, BR:VDD, PLLS:VDD

(VDD1-VDD2 : 0Ω @VDD<5.5V)



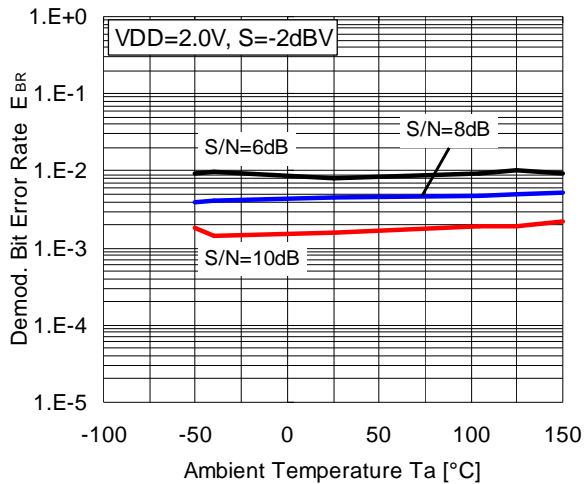
Demod. BER versus Temperature
PDRX:VDD, BR:VDD, PLLS:VSS

(VDD1-VDD2 : 0Ω @VDD<5.5V)



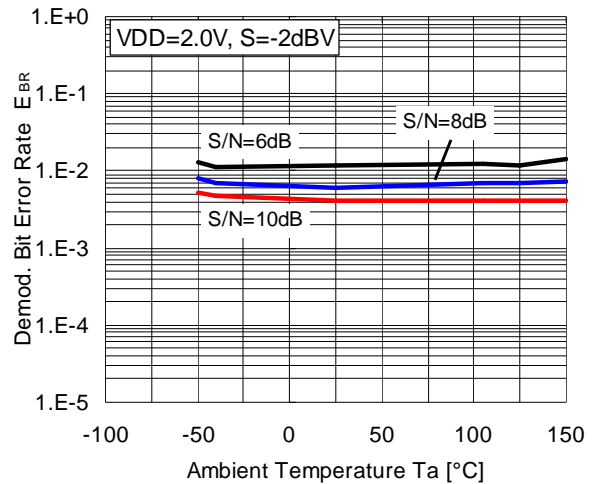
Demod. BER versus Temperature
PDRX:VDD, BR:VDD, PLLS:VDD

(VDD1-VDD2 : 0Ω @VDD<5.5V)



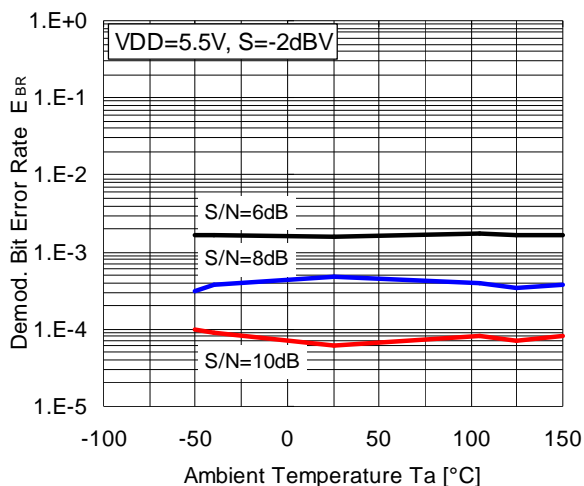
Demod. BER versus Temperature
PDRX:VDD, BR:VDD, PLLS:VSS

(VDD1-VDD2 : 0Ω @VDD<5.5V)



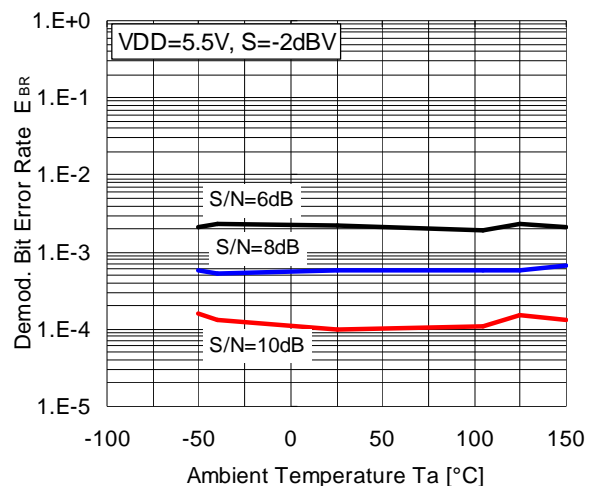
Demod. BER versus Temperature
PDRX:VDD, BR:VDD, PLLS:VDD

(VDD1-VDD2 : 3kΩ @VDD≥5.5V)



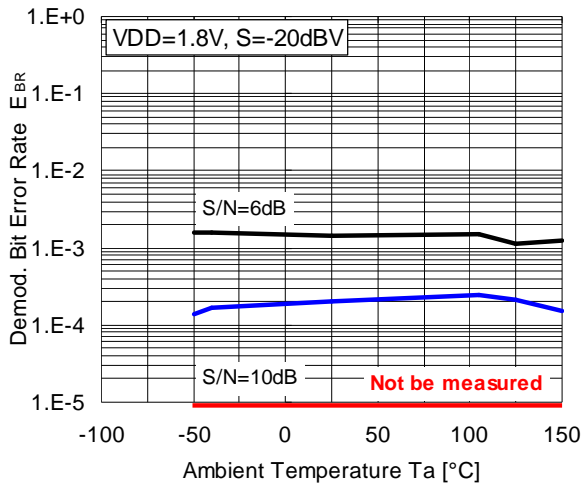
Demod. BER versus Temperature
PDRX:VDD, BR:VDD, PLLS:VSS

(VDD1-VDD2 : 3kΩ @VDD≥5.5V)

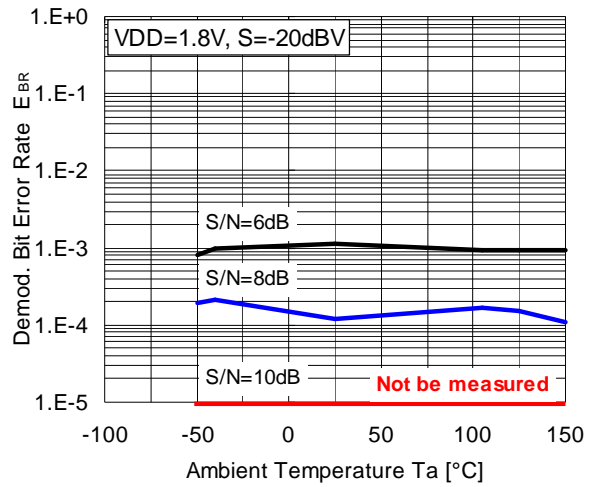


[Demodulation Bit Error Rate]

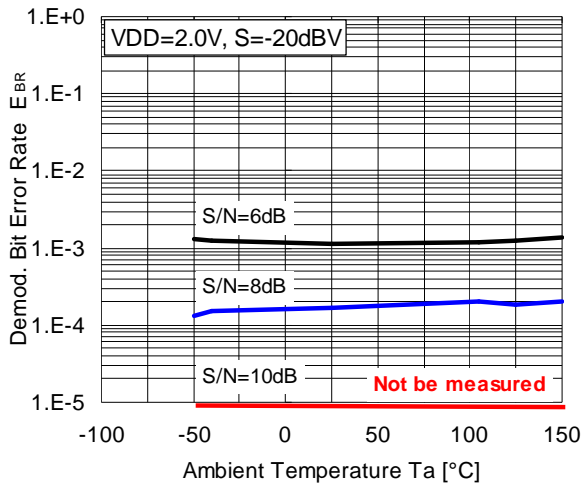
Demod. BER versus Temperature
 PDRX:VDD, BR:VDD, PLLS:VDD
 (VDD1-VDD2 : 0Ω @VDD<5.5V)



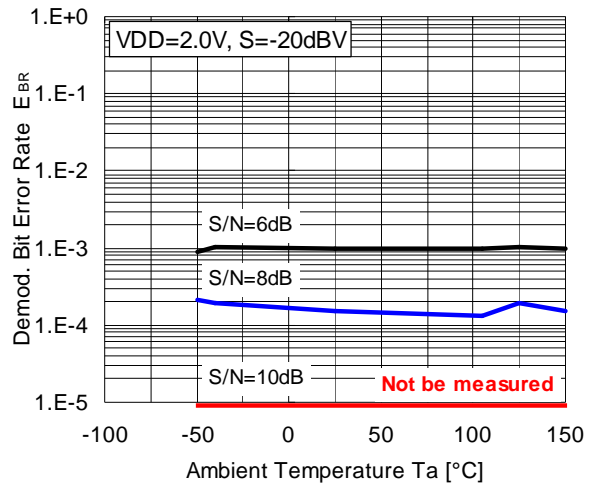
Demod. BER versus Temperature
 PDRX:VDD, BR:VDD, PLLS:VSS
 (VDD1-VDD2 : 0Ω @VDD<5.5V)



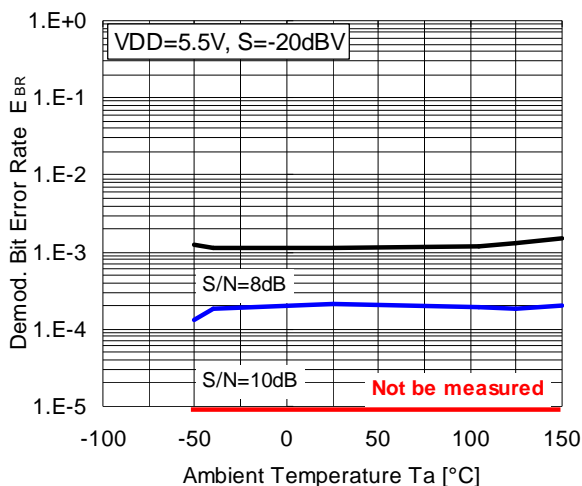
Demod. BER versus Temperature
 PDRX:VDD, BR:VDD, PLLS:VDD
 (VDD1-VDD2 : 0Ω @VDD<5.5V)



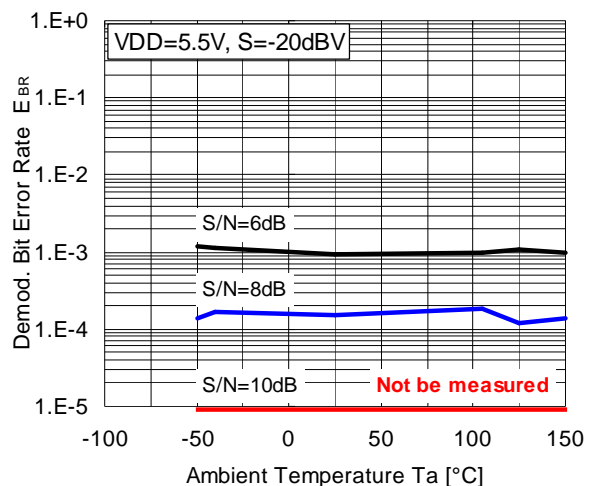
Demod. BER versus Temperature
 PDRX:VDD, BR:VDD, PLLS:VSS
 (VDD1-VDD2 : 0Ω @VDD<5.5V)



Demod. BER versus Temperature
 PDRX:VDD, BR:VDD, PLLS:VDD
 (VDD1-VDD2 : 3kΩ @VDD≥5.5V)



Demod. BER versus Temperature
 PDRX:VDD, BR:VDD, PLLS:VSS
 (VDD1-VDD2 : 3kΩ @VDD≥5.5V)

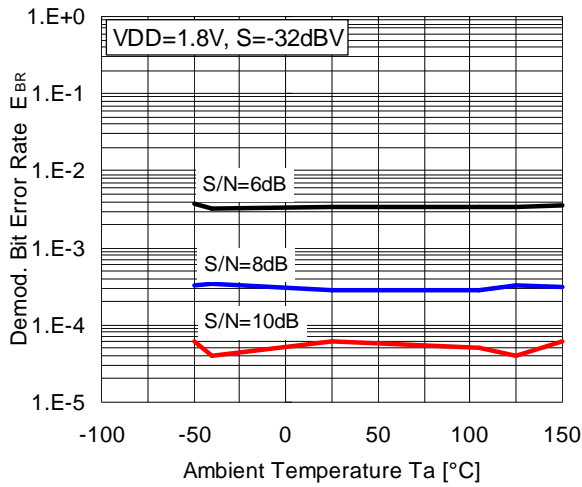


[Demodulation Bit Error Rate]

Demod. BER versus Temperature

PDRX:VDD, BR:VDD, PLLS:VDD

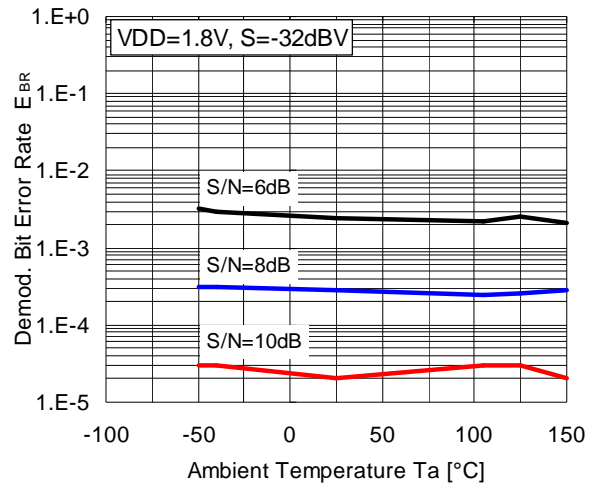
(VDD1-VDD2 : 0Ω @VDD<5.5V)



Demod. BER versus Temperature

PDRX:VDD, BR:VDD, PLLS:VSS

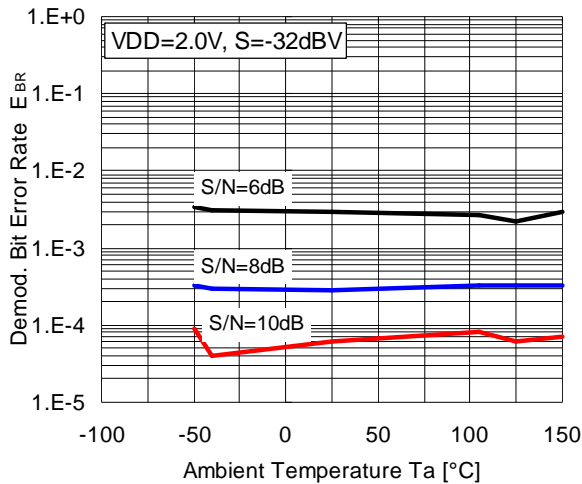
(VDD1-VDD2 : 0Ω @VDD<5.5V)



Demod. BER versus Temperature

PDRX:VDD, BR:VDD, PLLS:VDD

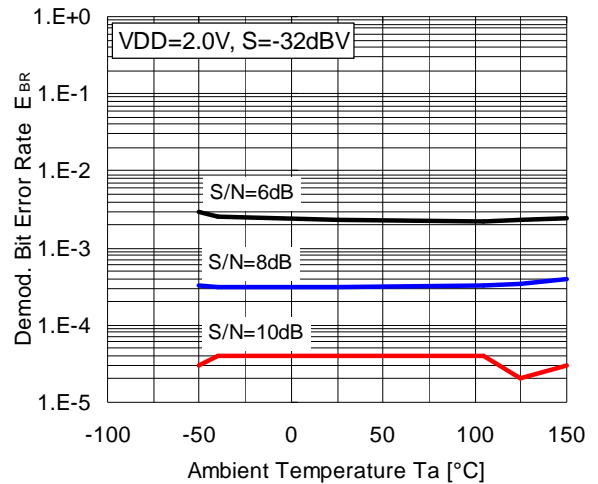
(VDD1-VDD2 : 0Ω @VDD<5.5V)



Demod. BER versus Temperature

PDRX:VDD, BR:VDD, PLLS:VSS

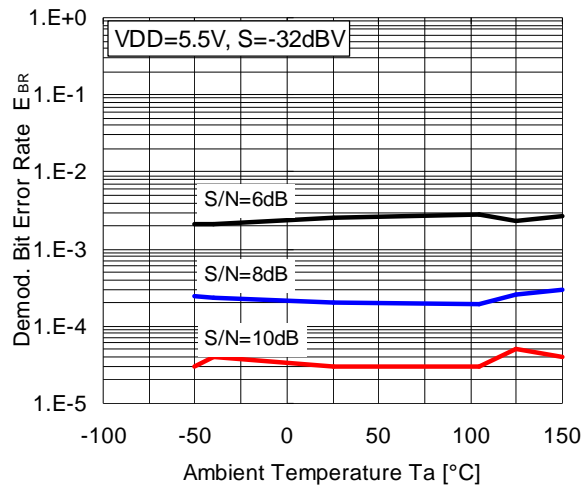
(VDD1-VDD2 : 0Ω @VDD<5.5V)



Demod. BER versus Temperature

PDRX:VDD, BR:VDD, PLLS:VDD

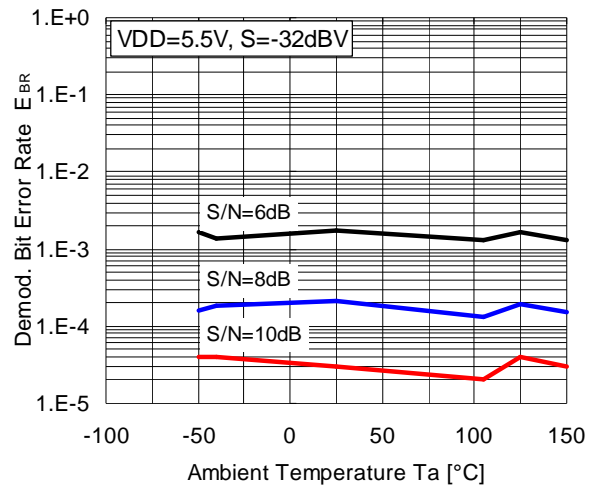
(VDD1-VDD2 : 3kΩ @VDD≥5.5V)



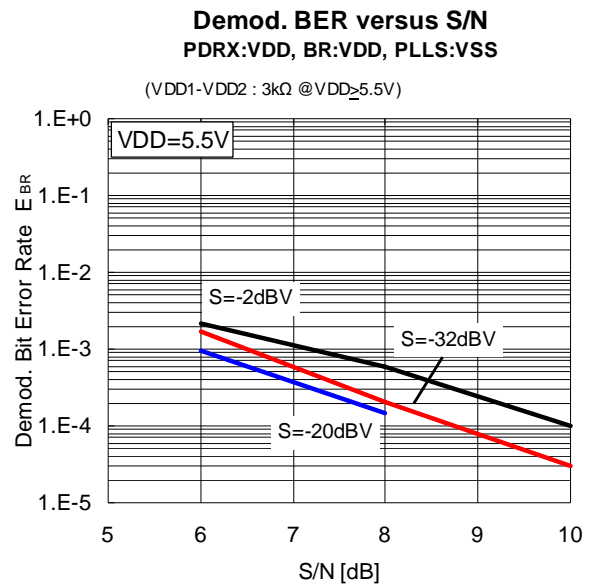
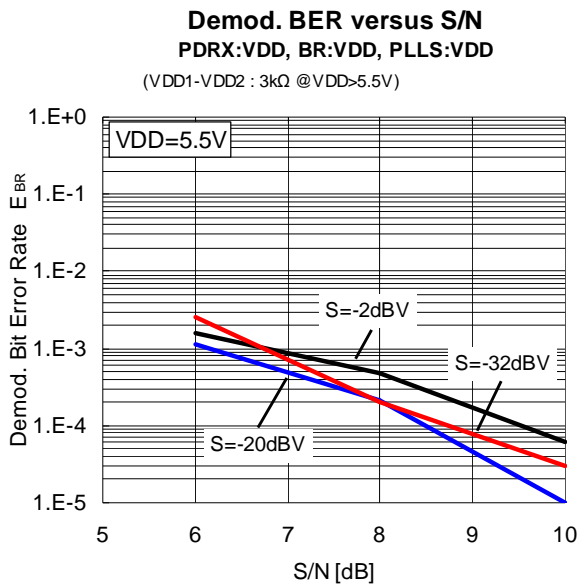
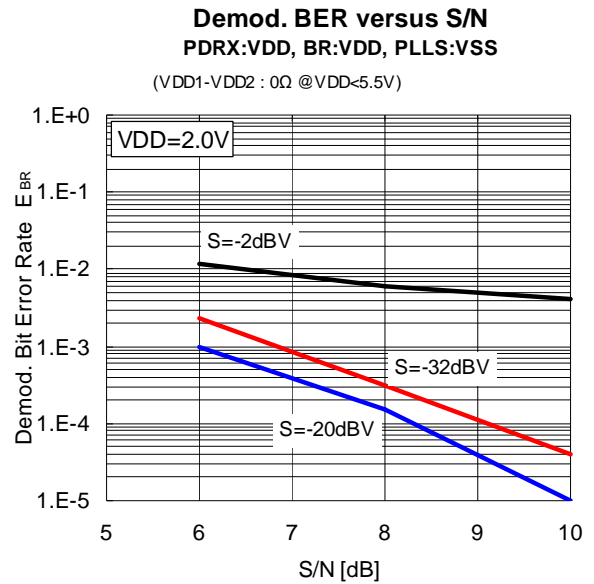
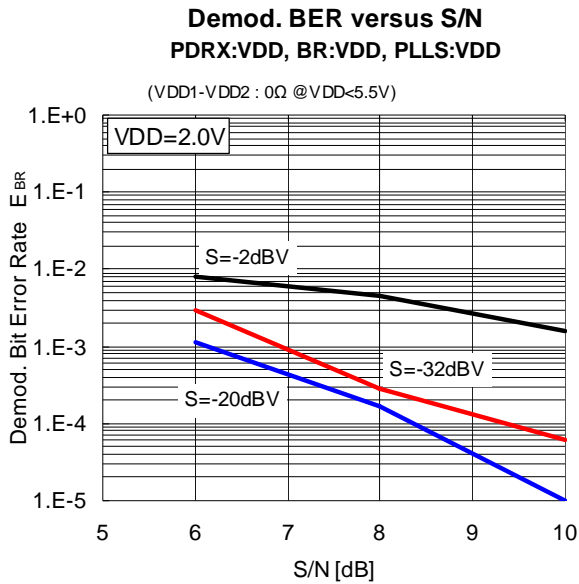
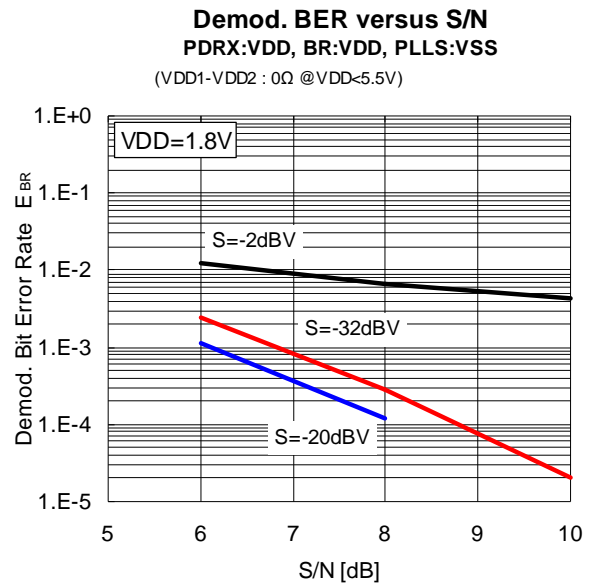
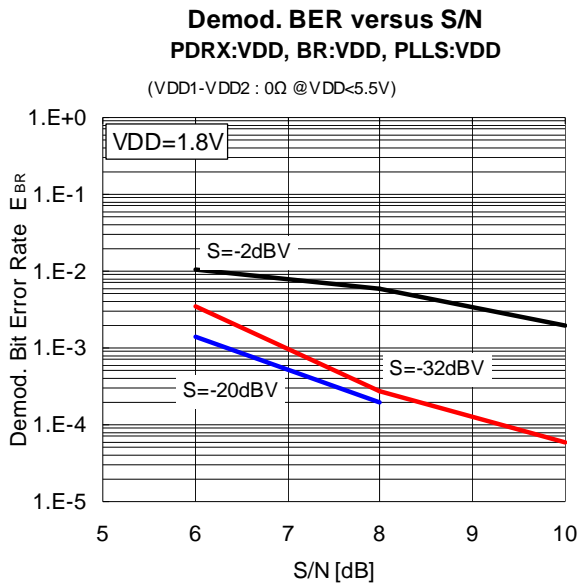
Demod. BER versus Temperature

PDRX:VDD, BR:VDD, PLLS:VSS

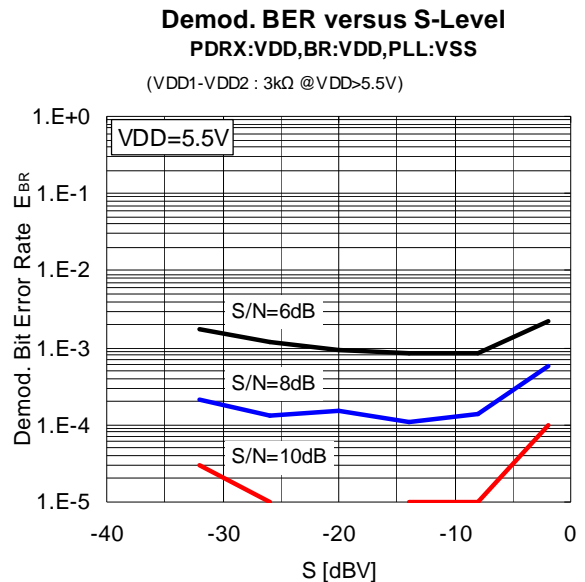
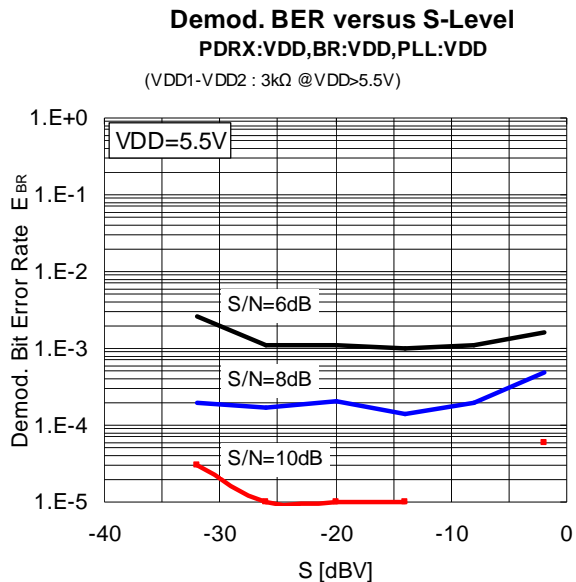
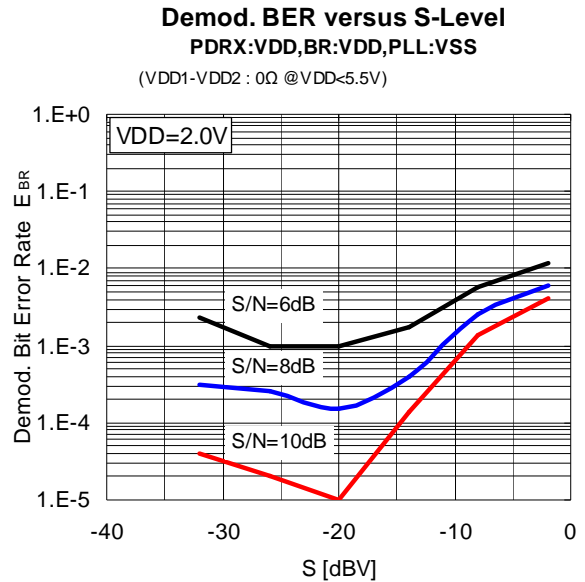
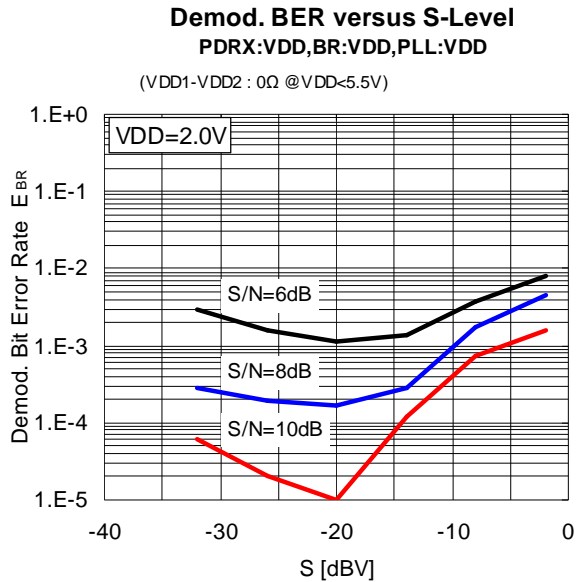
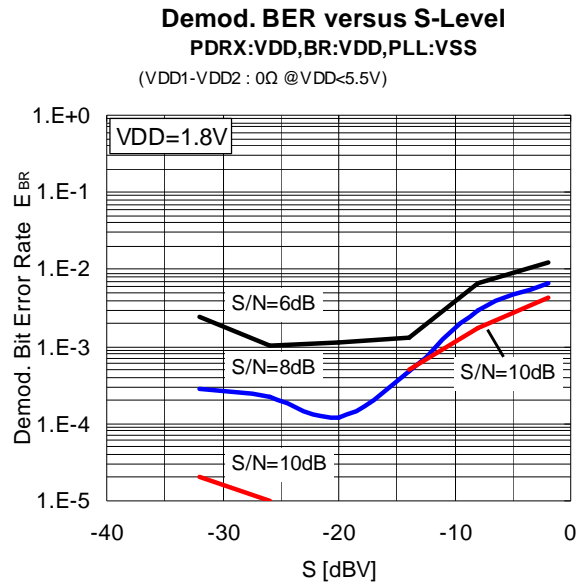
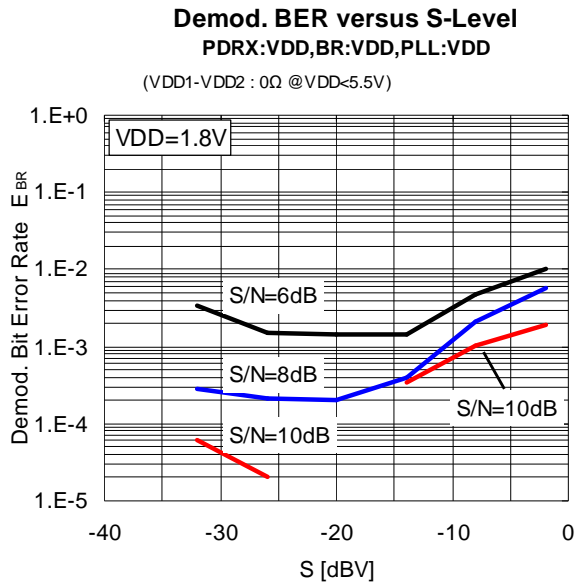
(VDD1-VDD2 : 3kΩ @VDD≥5.5V)



[Demodulation Bit Error Rate]



[Demodulation Bit Error Rate]



[CAUTION]

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