

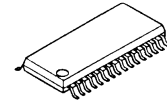
## 7-INPUT / 3-OUTPUT DUAL ANALOG SWITCH

### ■ GENERAL DESCRIPTION

The **NJU72750A** is a 7-input / 3-output dual analog switch. Functions are controlled via two-wired serial bus. A-channel switches and B-channel switches are controlled independently.

The **NJU72750A** is well-suited for multi-channel audio systems such as AV amplifiers, DVD receivers and others.

### ■ PACKAGE OUTLINE



**NJU72750AV**

### ■ FEATURES

ℓ Operating Voltage

ℓ 2-wired Serial BUS Control

ℓ Selectable 2-Chip Address

ℓ ON Resistance

ℓ Low Distortion

ℓ CMOS Technology

ℓ Package Outline

Dual power supply:  $\pm 4.5$  to  $\pm 7.5$ V

Single power supply: +9.0 to +15.0V

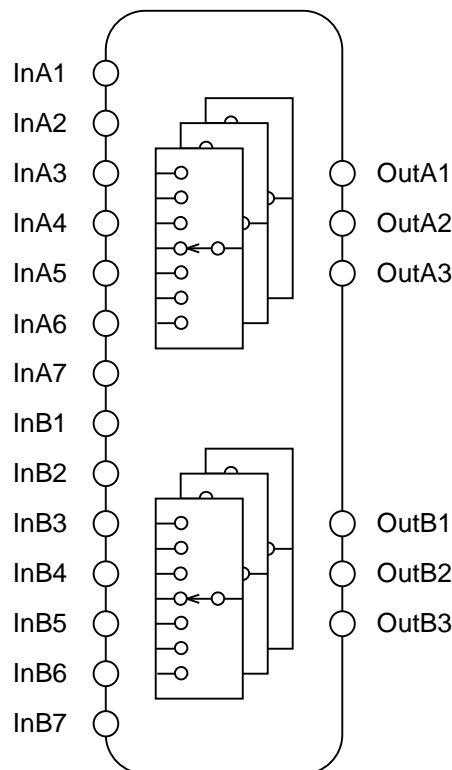
Available for using four chips on same serial bus line

15 $\Omega$  typ.

0.0004% typ. ( $V_{IN}=1V_{rms}$ )

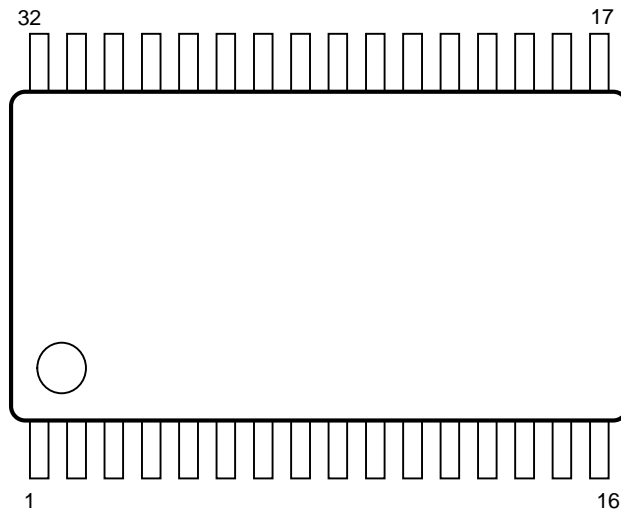
SSOP32

### ■ BLOCK DIAGRAM



# NJU72750A

## ■ PIN CONFIGURATION



| No. | Symbol | Function                                 |    | Symbol | Function                           |
|-----|--------|--|----|--------|------------------------------------|
| 1   | V+     | Power supply (+)                         | 17 | DATA   | Control data signal Input terminal |
| 2   | InA1   | Ach Input terminal 1                     | 18 | CLOCK  | Clock signal Input terminal        |
| 3   | InB1   | Bch Input terminal 1                     | 19 | NC     | No connect                         |
| 4   | InA2   | Ach Input terminal 2                     | 20 | NC     | No connect                         |
| 5   | InB2   | Bch Input terminal 2                     | 21 | OutB3  | Bch Output terminal 3              |
| 6   | InA3   | Ach Input terminal 3                     | 22 | OutA3  | Ach Output terminal 3              |
| 7   | InB3   | Bch Input terminal 3                     | 23 | REF_B  | Bch Reference Voltage terminal     |
| 8   | InA4   | Ach Input terminal 4                     | 24 | OutB2  | Bch Output terminal 2              |
| 9   | InB4   | Bch Input terminal 4                     | 25 | OutA2  | Ach Output terminal 2              |
| 10  | InA5   | Ach Input terminal 5                     | 26 | REF_A  | Ach Reference Voltage terminal     |
| 11  | InB5   | Bch Input terminal 5                     | 27 | OutB1  | Bch Output terminal 1              |
| 12  | InA6   | Ach Input terminal 6                     | 28 | OutA1  | Ach Output terminal 1              |
| 13  | InB6   | Bch Input terminal 6                     | 29 | NC     | No connect                         |
| 14  | InA7   | Ach Input terminal 7                     | 30 | ADR0   | Chip address setting terminal 0    |
| 15  | InB7   | Bch Input terminal 7                     | 31 | ADR1   | Chip address setting terminal 1    |
| 16  | REF    | Digital block reference voltage terminal | 32 | V-     | Power supply (-)                   |

## ■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

| PARAMETER                   | SYMBOL                         | RATING   | UNIT |
|-----------------------------|--------------------------------|--|------|
| Supply Voltage              | V <sup>+</sup> /V <sup>-</sup> | ±8   | V    |
| Maximum Input Voltage       | V <sub>IM</sub>                | V <sup>+</sup> /V <sup>-</sup>   | V    |
| Power Dissipation           | P <sub>D</sub>                 | 950<br>NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting | mW   |
| Operating Temperature Range | T <sub>opr</sub>               | -40 to +85   | °C   |
| Storage Temperature Range   | T <sub>stg</sub>               | -40 to +125  | °C   |
| Load Resistance             | R <sub>L</sub>                 | >1   | kΩ   |

## ■ RECOMMENDED OPERATING VOLTAGE RANGE (Ta=25°C unless otherwise specified)

| PARAMETER               | SYMBOL                         | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------------|--------------------------------|----------------|------|------|------|------|
| Operating Voltage Range | V <sup>+</sup> /V <sup>-</sup> |                | ±4.5 | ±7.0 | ±7.5 | V    |

## ■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V<sup>+</sup>/V<sup>-</sup>=±7, R<sub>L</sub>=20kΩ unless otherwise specified)

### ◆DC CHARACTERISTICS

| PARAMETER             | SYMBOL           | TEST CONDITION  | MIN. | TYP. | MAX. | UNIT |
|-----------------------|------------------|---|------|------|------|------|
| Supply Current1       | I <sub>DD</sub>  | No Signal (V <sup>+</sup> ), No Load                  | -    | 0.4  | 1    | mA   |
| Supply Current2       | I <sub>SS</sub>  | No Signal (V <sup>-</sup> ), No Load                  | -    | 0.4  | 1    | mA   |
| Switch ON Resistance1 | R <sub>ON1</sub> | Switch A11 to A73, B11 to B73,<br>I <sub>O</sub> =3mA | -    | 15   | 40   | Ω    |
| Switch ON Resistance2 | R <sub>ON2</sub> | L-Imp A1 to A3, B1 to B3,<br>I <sub>O</sub> =300μA    | -    | 0.4  | 1    | kΩ   |

### ◆AC CHARACTERISTICS

| PARAMETER                 | SYMBOL | TEST CONDITION  | MIN. | TYP.   | MAX. | UNIT |
|---------------------------|--------|---|------|--------|------|------|
| Total Harmonic Distortion | T.H.D. | f=1kHz, V <sub>IN</sub> =1Vrms,<br>BW=400Hz to 30kHz            | -    | 0.0004 | -    | %    |
| Cross Talk                | CT     | R <sub>g</sub> =0Ω, f=1kHz, V <sub>IN</sub> =2Vrms,<br>Bandpass | -    | -110   | -    | dB   |
| Channel Separation        | CS     | R <sub>g</sub> =0Ω, f=1kHz, V <sub>IN</sub> =2Vrms,<br>Bandpass | -    | -110   | -    | dB   |

## ■ LOGIC CONTROL CHARACTERISTICS (Ta=25°C unless otherwise specified)

### ◆LOGIC CONTROL TERMINAL CHARACTERISTICS

| PARAMETER                  | SYMBOL           | TEST CONDITION       | MIN. | TYP. | MAX.           | UNIT |
|----------------------------|------------------|----------------------|------|------|----------------|------|
| High Level Input Voltage 1 | V <sub>IH1</sub> | ADR0, ADR1 terminal  | 2.5  | -    | V <sup>+</sup> | V    |
| Low Level Input Voltage 1  | V <sub>IL1</sub> | ADR0, ADR1 terminal  | 0    | -    | 0.8            | V    |
| High Level Input Voltage 2 | V <sub>IH2</sub> | DATA, CLOCK terminal | 2.5  | -    | 5.5            | V    |
| Low Level Input Voltage 2  | V <sub>IL2</sub> | DATA, CLOCK terminal | 0    | -    | 0.8            | V    |

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## ■ TERMINAL DESCRIPTION

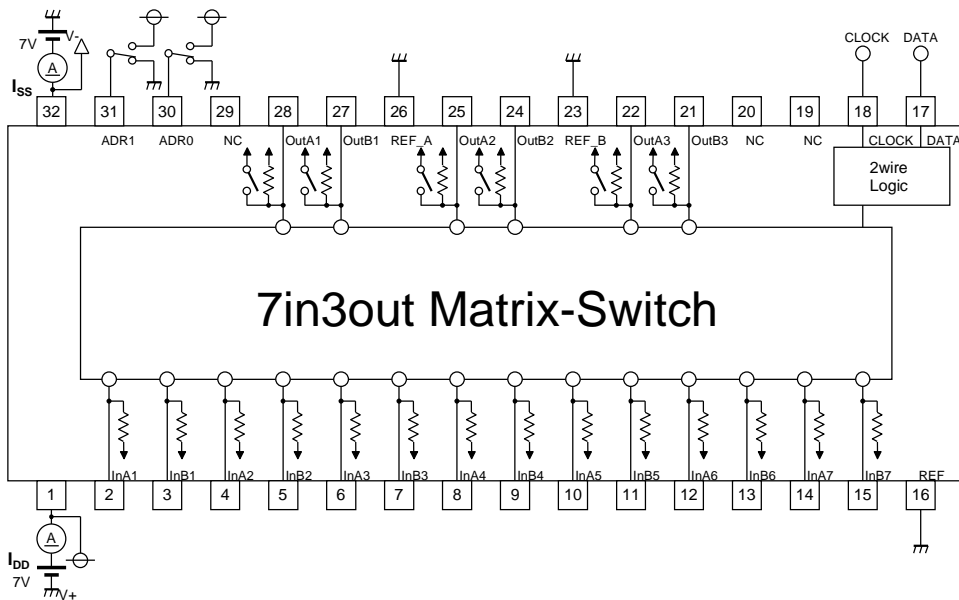
| Terminal   | SYMBOL   | FUNCTION   | EQUIVALENT CIRCUIT | VOLTAGE |
|--|--|--|--------------------|---------|
| 2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10<br>11<br>12<br>13<br>14<br>15<br>23<br>26 | InA1<br>InB1<br>InA2<br>InB2<br>InA3<br>InB3<br>InA4<br>InB4<br>InA5<br>InB5<br>InA6<br>InB6<br>InA7<br>InB7<br>REF_B<br>REF_A | Ach Input 1<br>Bch Input 1<br>Ach Input 2<br>Bch Input 2<br>Ach Input 3<br>Bch Input 3<br>Ach Input 4<br>Bch Input 4<br>Ach Input 5<br>Bch Input 5<br>Ach Input 6<br>Bch Input 6<br>Ach Input 7<br>Bch Input 7<br>Bch Reference<br>Ach Reference |                    | -       |
| 16   | REF  | Digital Reference  |                    | -       |
| 17<br>18   | DATA<br>CLOCK  | Control data Input<br>Clock signal Input   |                    | -       |
| 21<br>22<br>24<br>25<br>27<br>28   | OutB3<br>OutA3<br>OutB2<br>OutA2<br>OutB1<br>OutA1   | Bch Output 3<br>Ach Output 3<br>Bch Output 2<br>Ach Output 2<br>Bch Output 1<br>Ach Output 1   |                    | -       |

| Terminal         | SYMBOL               | FUNCTION                                 | EQUIVALENT CIRCUIT | VOLTAGE  |
|------------------|----------------------|--|--------------------|----------|
| <p>30<br/>31</p> | <p>ADR0<br/>ADR1</p> | <p>Chip address 0<br/>Chip address 1</p> |                    | <p>-</p> |

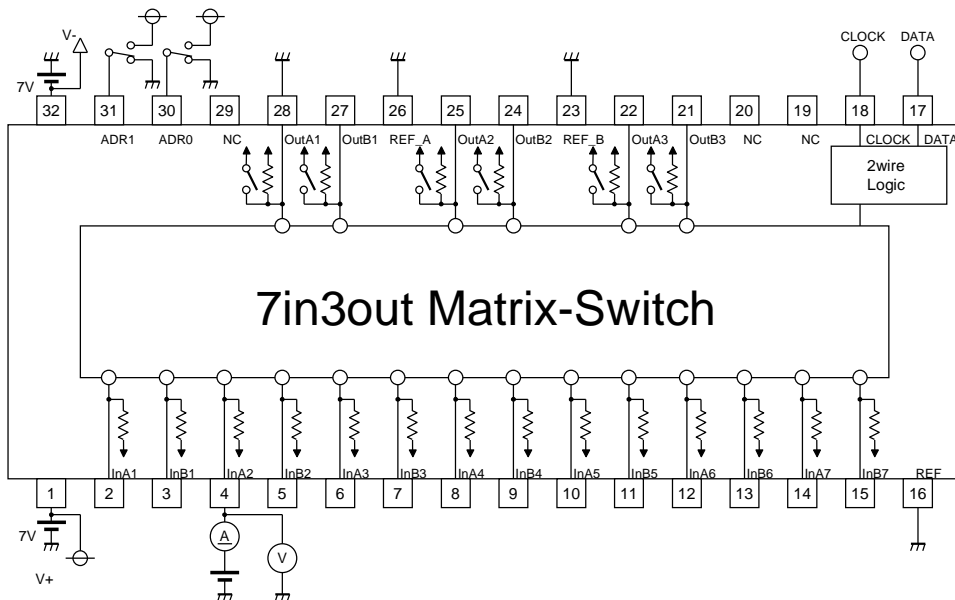
# NJU72750A

## ■ TEST CIRCUIT

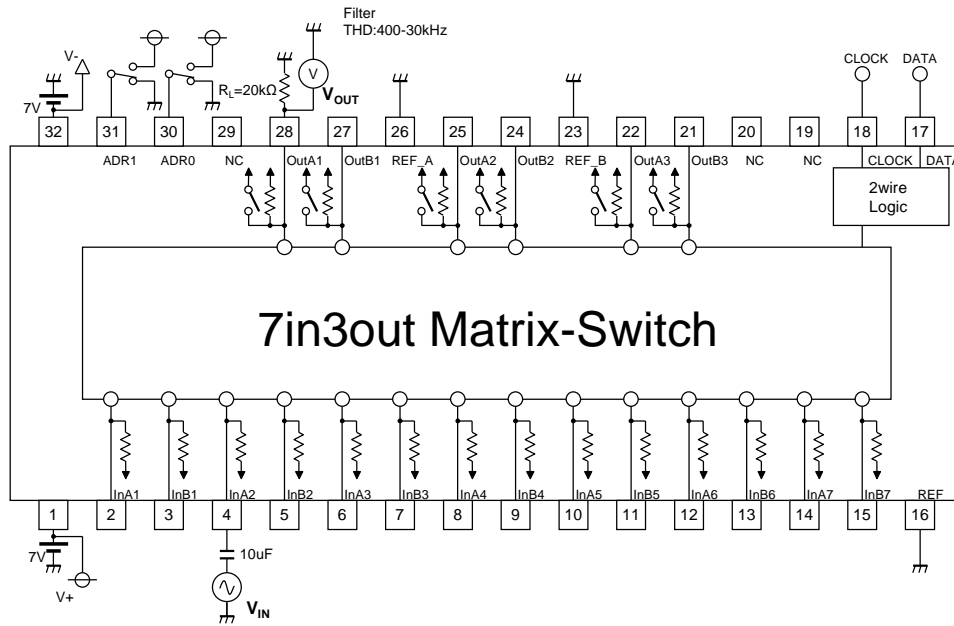
◆  $I_{DD}/I_{SS}$



◆  $R_{ON}$



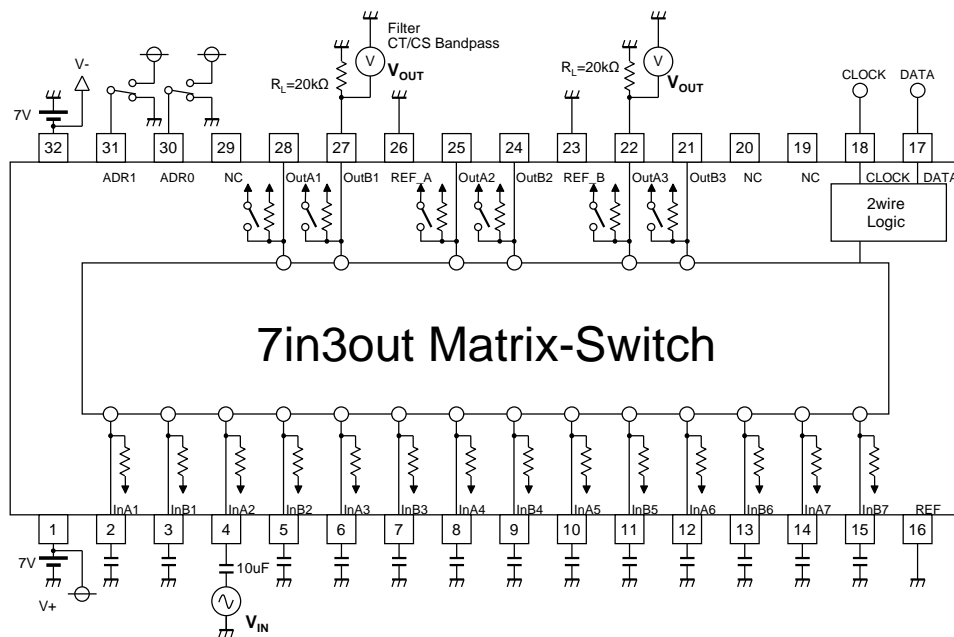
## ◆THD



## ◆CT/CS

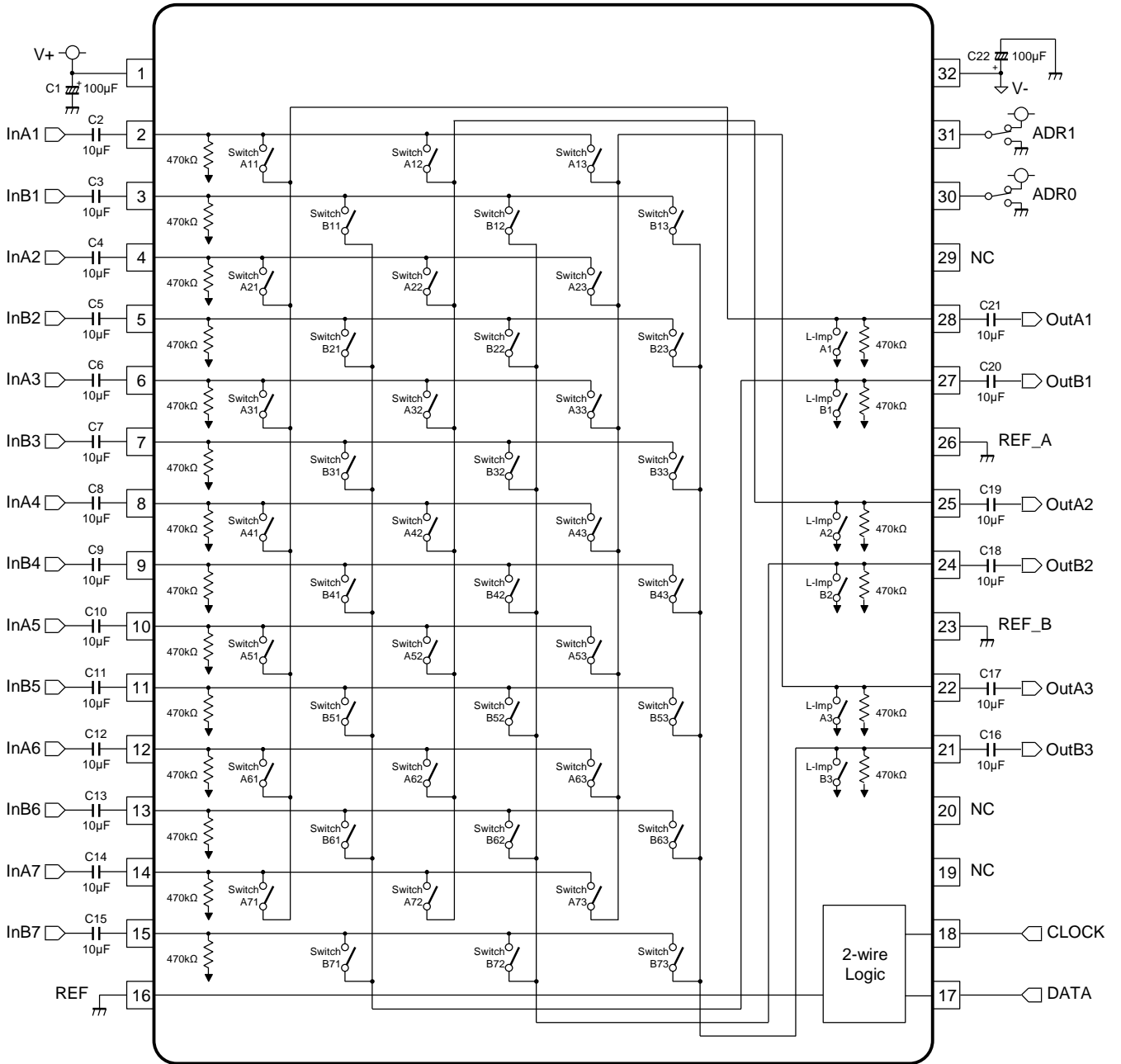
**CT** Ex) A11=ON, A21=OFF, Input=InA2 -> Measure=OutA1  
 B12=ON, B22=OFF, Input=InB2 -> Measure=OutB2

**CS** Ex) A11=ON, B11=ON, Input=InB1 -> Measure=OutA1  
 B11=ON, A31=ON, Input=InA3 -> Measure=OutB1



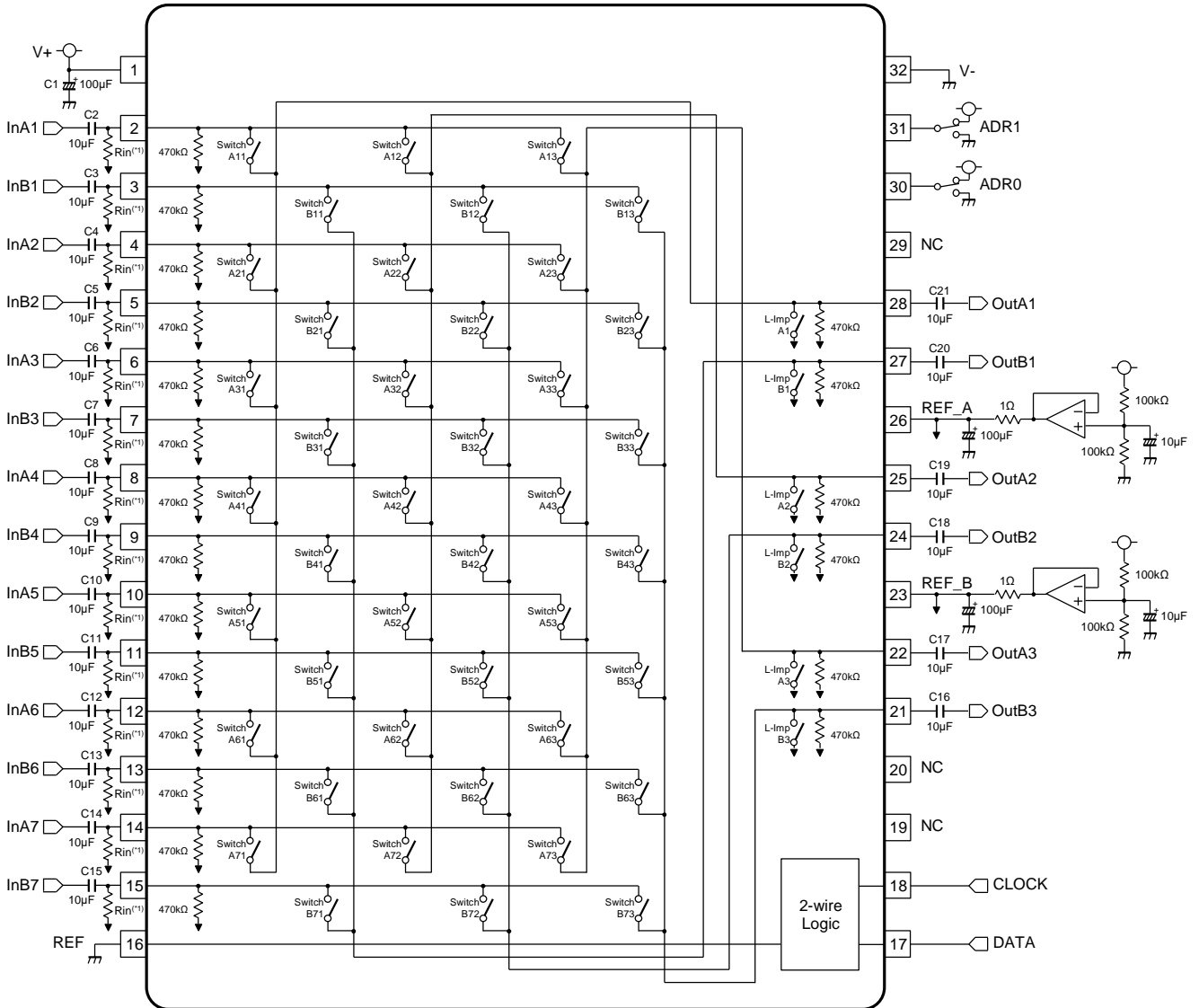
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## ■ APPLICATION CIRCUIT 1 (Dual power supply operation)





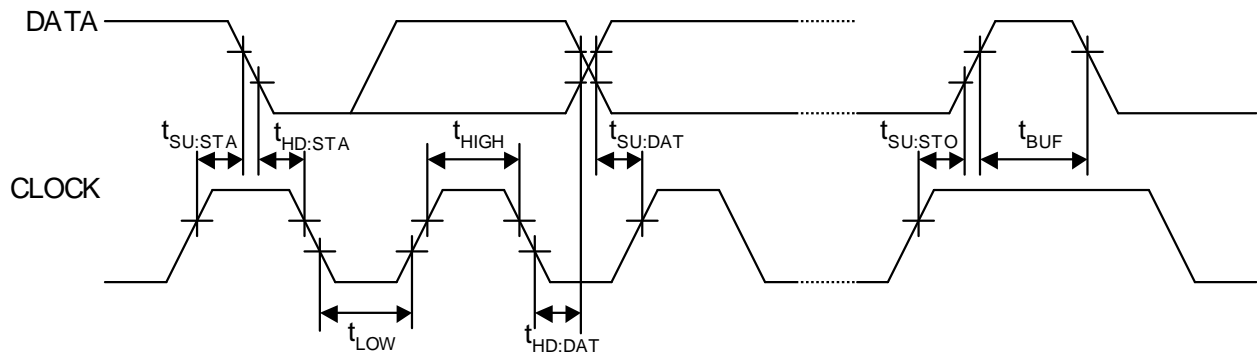
## APPLICATION CIRCUIT 2 (Single power supply operation)



(\*) When power supply is turned on, please add external resistors "Rin" in the case that wish to shorten the time to stabilize reference voltage.

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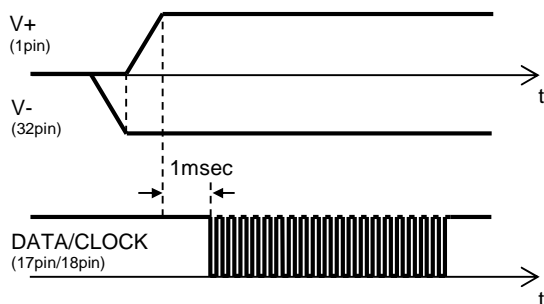
## ■TIMING ON 2-wire BUS (DATA, CLOCK)



## ■CHARACTERISTICS OF I/O STAGES FOR 2-wire BUS (DATA, CLOCK)

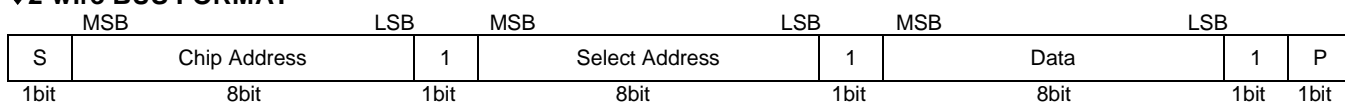
| PARAMETER     | SYMBOL   | MIN. | TYP. | MAX. | UNIT          |
|---------------|--|------|------|------|---------------|
| $t_{HD\_STA}$ | Hold time (repeated) START condition.            | 4    | -    | -    | $\mu\text{s}$ |
| $t_{LOW}$     | Low period of the CLOCK clock                    | 2    | -    | -    | $\mu\text{s}$ |
| $t_{HIGH}$    | High period of the CLOCK clock                   | 2    | -    | -    | $\mu\text{s}$ |
| $t_{SU\_STA}$ | Set-up time for a repeated START condition       | 2    | -    | -    | $\mu\text{s}$ |
| $t_{HD\_DAT}$ | Data hold time                                   | 1    | -    | -    | $\mu\text{s}$ |
| $t_{SU\_DAT}$ | Data set-up time                                 | 1    | -    | -    | $\mu\text{s}$ |
| $t_{SU\_STO}$ | Set-up time for STOP condition                   | 2    | -    | -    | $\mu\text{s}$ |
| $t_{BUF}$     | Bus free time between a STOP and START condition | 4    | -    | -    | $\mu\text{s}$ |

## ■RECOMMENDED POWER-UP SEQUENCE



## ■ DEFINITION OF 2-wire REGISTER

### ◆ 2-wire BUS FORMAT



S: Starting Term

P: Ending Term

### ◆ Chip Address

| MSB |   |   |   |   | LSB  |      |   |                                |
|-----|---|---|---|---|------|------|---|--------------------------------|
| 1   | 0 | 0 | 1 | 1 | ADR1 | ADR0 | 0 |                                |
| 1   | 0 | 0 | 1 | 1 | 0    | 0    | 0 | 98H (ADR1 = Low, ADR0 = Low)   |
| 1   | 0 | 0 | 1 | 1 | 0    | 1    | 0 | 9AH (ADR1 = Low, ADR0 = High)  |
| 1   | 0 | 0 | 1 | 1 | 1    | 0    | 0 | 9CH (ADR1 = High, ADR0 = Low)  |
| 1   | 0 | 0 | 1 | 1 | 1    | 1    | 0 | 9EH (ADR1 = High, ADR0 = High) |

### ◆ Select Address

The select address sets each function.

The auto increment function cycles the select address as follows.

00H→01H→02H→03H→04H→05H→00H

| Select Address | MSB |     |     |     |     |     |     | LSB      |
|----------------|-----|-----|-----|-----|-----|-----|-----|----------|
|                | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0       |
| 00H            | A71 | A61 | A51 | A41 | A31 | A21 | A11 | L-Imp A1 |
| 01H            | B71 | B61 | B51 | B41 | B31 | B21 | B11 | L-Imp B1 |
| 02H            | A72 | A62 | A52 | A42 | A32 | A22 | A12 | L-Imp A2 |
| 03H            | B72 | B62 | B52 | B42 | B32 | B22 | B12 | L-Imp B2 |
| 04H            | A73 | A63 | A53 | A43 | A33 | A23 | A13 | L-Imp A3 |
| 05H            | B73 | B63 | B53 | B43 | B33 | B23 | B13 | L-Imp B3 |

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## ■ INITIAL CONDITION

| Select Address | Data |    |    |    |    |    |    |    |
|----------------|------|----|----|----|----|----|----|----|
|                | D7   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00H            | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 01H            | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 02H            | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 03H            | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 04H            | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 05H            | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

Note.) This product starts up by MUTE setting in power "ON". Use it after removing MUTE of each setting.

If any audio signal is inputted in input signal terminal before power "ON", it may cause initial condition abnormality.

In conditions of use such as the above, it prevents that abnormality by setting MUTE before power "OFF"

## ■ DEFINITION OF RESISTOR

**Switch(A11 to A73, B11 to B73):** Select "Switch ON" or "Switch OFF". Each switch is controlled independently.

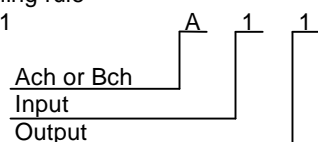
**L-Imp(A1 to A3, B1 to B3):** Select "Switch ON" or "Switch OFF". Each switch is controlled independently.

It is the switch lowers the impedance of the output terminal.

| Select Address | MSB  |     |     |     | LSB |     |     |          |
|----------------|------|-----|-----|-----|-----|-----|-----|----------|
|                | Data |     |     |     |     |     |     |          |
|                | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0       |
| 00H            | A71  | A61 | A51 | A41 | A31 | A21 | A11 | L-Imp A1 |
| 01H            | B71  | B61 | B51 | B41 | B31 | B21 | B11 | L-Imp B1 |
| 02H            | A72  | A62 | A52 | A42 | A32 | A22 | A12 | L-Imp A2 |
| 03H            | B72  | B62 | B52 | B42 | B32 | B22 | B12 | L-Imp B2 |
| 04H            | A73  | A63 | A53 | A43 | A33 | A23 | A13 | L-Imp A3 |
| 05H            | B73  | B63 | B53 | B43 | B33 | B23 | B13 | L-Imp B3 |

Data naming rule

Ex.) A11



< Switch Setting >

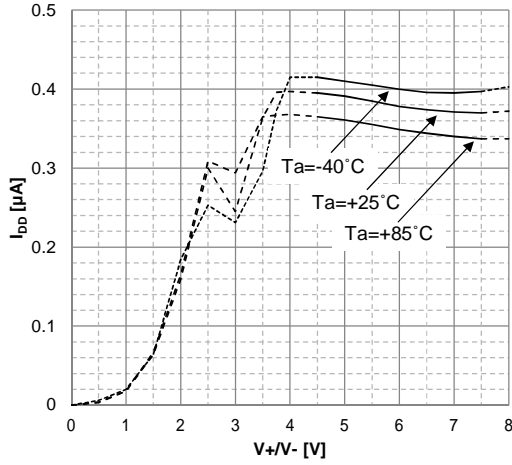
| Data    | Setting            |
|---------|--------------------|
| D7 ~ D0 |                    |
| 0       | OFF <sup>(c)</sup> |
| 1       | ON                 |

<sup>(c)</sup>Initial Setting

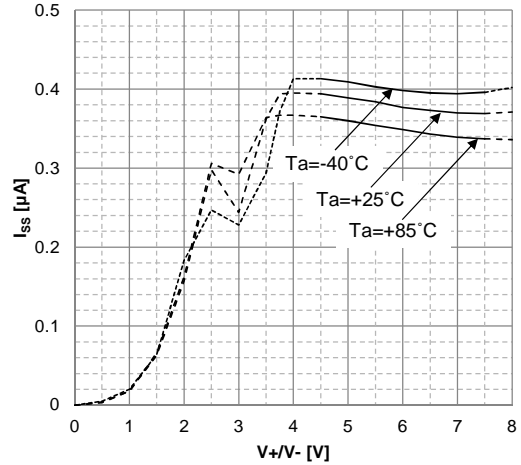
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## ■ TYPICAL CHARACTERISTICS

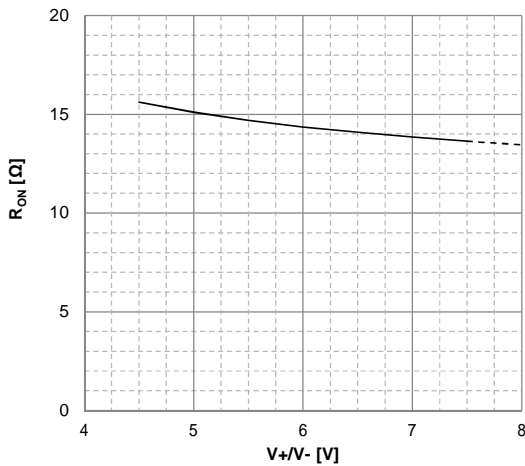
**Supply Current 1 vs Supply Voltage**  
No signal



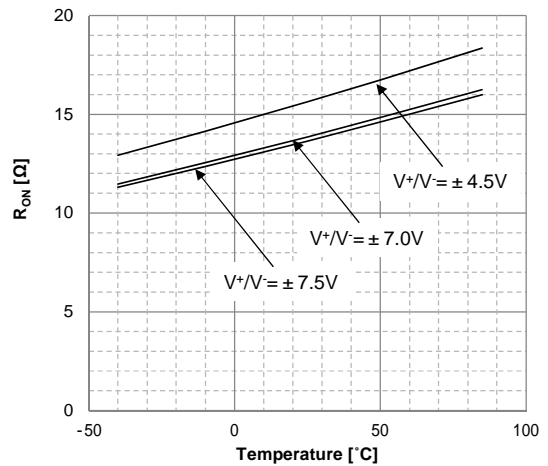
**Supply Current 2 vs Supply Voltage**  
No signal



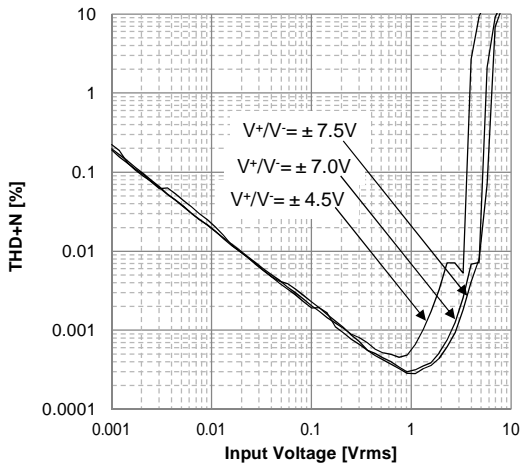
**Switch ON Resistance vs Supply Voltage**  
 $I_O=3mA$



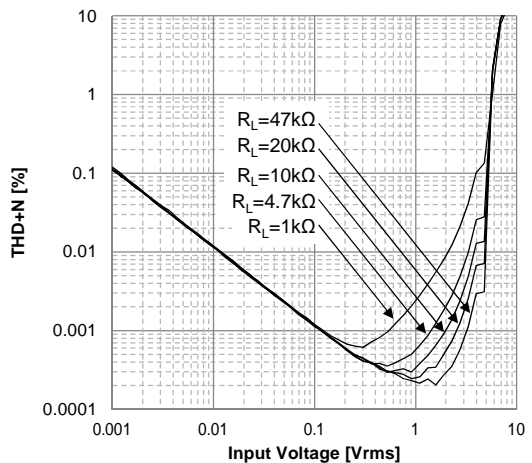
**Switch ON Resistance vs Temperature**  
 $I_O=3mA$



**THD+N vs Input Voltage**  
 $f=1kHz, R_L=20k\Omega, BW: 400-30kHz$



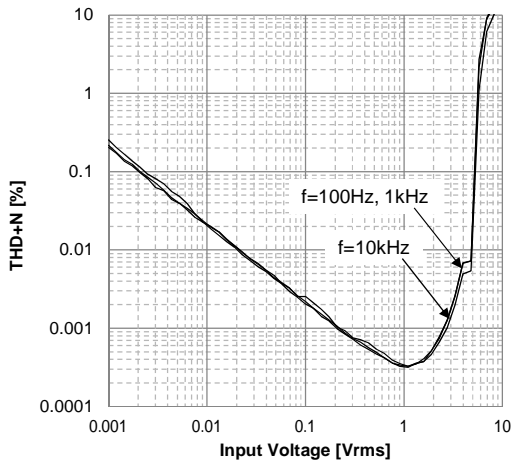
**THD+N vs Input Voltage**  
 $V+/V- = \pm 7V, f=1kHz, BW: 400-30kHz,$



## TYPICAL CHARACTERISTICS

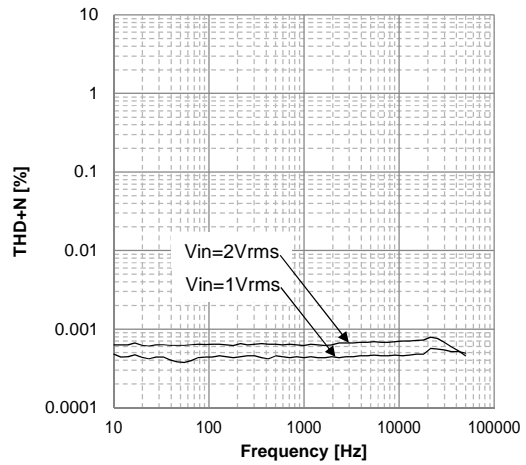
### THD+N vs Input Voltage

$V^+/V^- = \pm 7V$ ,  $R_L = 20k\Omega$ , BW: 10-30kHz



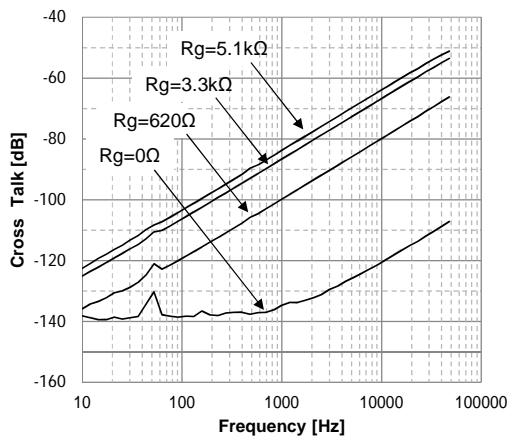
### THD+N vs Frequency

$V^+/V^- = \pm 7V$ ,  $R_L = 20k\Omega$ , BW: 10-80kHz



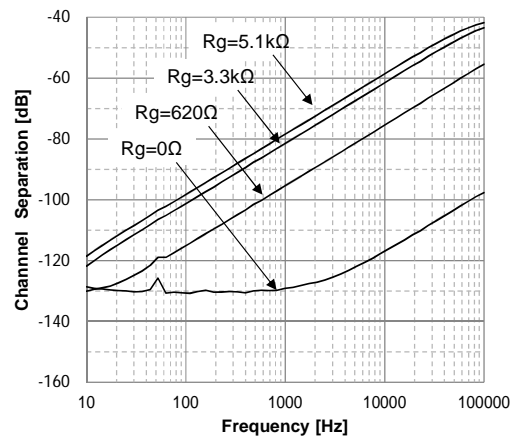
### Cross Talk vs Frequency

$V^+/V^- = \pm 7V$ ,  $V_{in} = 2V_{rms}$ ,  $R_L = 20k\Omega$ ,  
BW: Bandpass, I/O: InA2,3,4,5,6,7-OutA1,  
Rg: InA1, Select Channel=InA11



### Channel Separation vs Frequency

$V^+/V^- = \pm 7V$ ,  $V_{in} = 2V_{rms}$ ,  $R_L = 20k\Omega$ ,  
BW: Bandpass, I/O: InB1,2,3,4,5,6,7-OutA1,  
Rg: InA1, Select Channel=InA11, InB11-73



**[CAUTION]**  
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