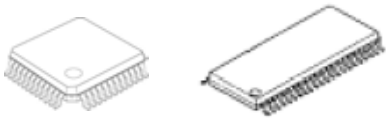
Preliminary

1/3, 1/4 Duty LCD Driver

■ GENERAL DESCRIPTION

NJU6532 is a 1/3 or 1/4 duty segment type LCD driver.
It incorporates 4 common driver circuits and 32 segment driver circuits. **NJU6532** can drive maximum 96(84)* segments in 1/3 duty ratio and maximum 128(112)* segments in 1/4 duty ratio.
Be addition, the **NJU6532**'s useful functions and small package meet a wide range of applications.

■ PACKAGE OUTLINE

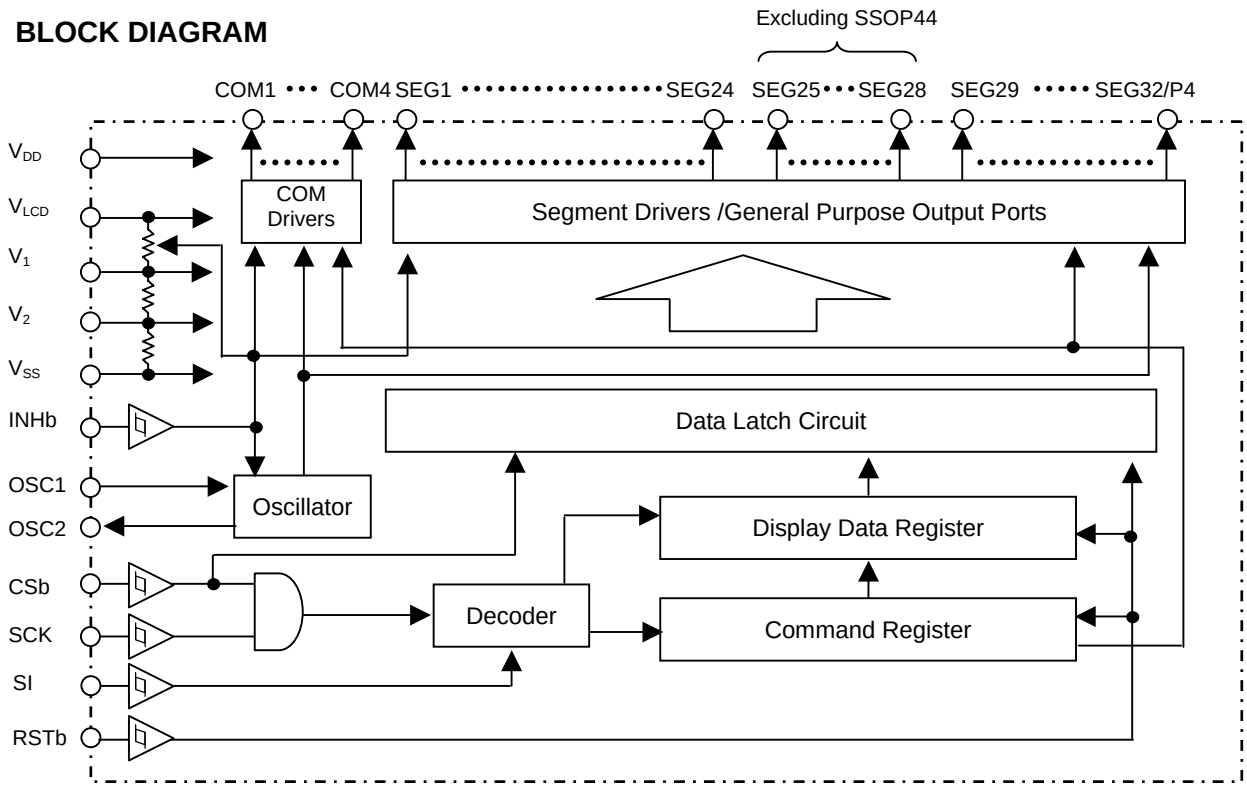


NJU6532FR3 **NJU6532V**

■ FEATURES

- LCD driving circuit :Max. 32outputs (SSOP44: Max. 28outputs) (4 outputs as for general purpose ports)
- Programmable Duty Ratio
  1/3 duty ratio :Driving max. 96 segments (SSOP44:Driving max. 84 segments)
  1/4 duty ratio :Driving max. 128 segments (SSOP44:Driving max. 112 segments)
- Programmable Bias Ratio :1/2, 1/3 bias ratio
- Serial Data Transfer :Shift clock max. 2MHz
- Built-in Oscillator :CR oscillation with external resistor, or external oscillation signal input
- Display OFF :INHb terminal
- Operating Voltage :2.7 to 5.5V
- LCD Driving Voltage :Vdd to 8.0V
- C-MOS Technology :P-Sub
- Package Outline :SSOP44, LQFP48-R3

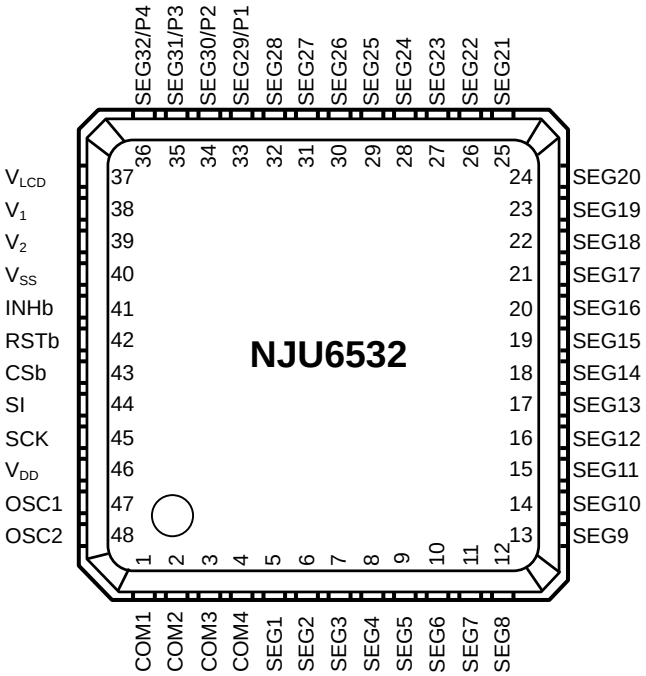
■ BLOCK DIAGRAM



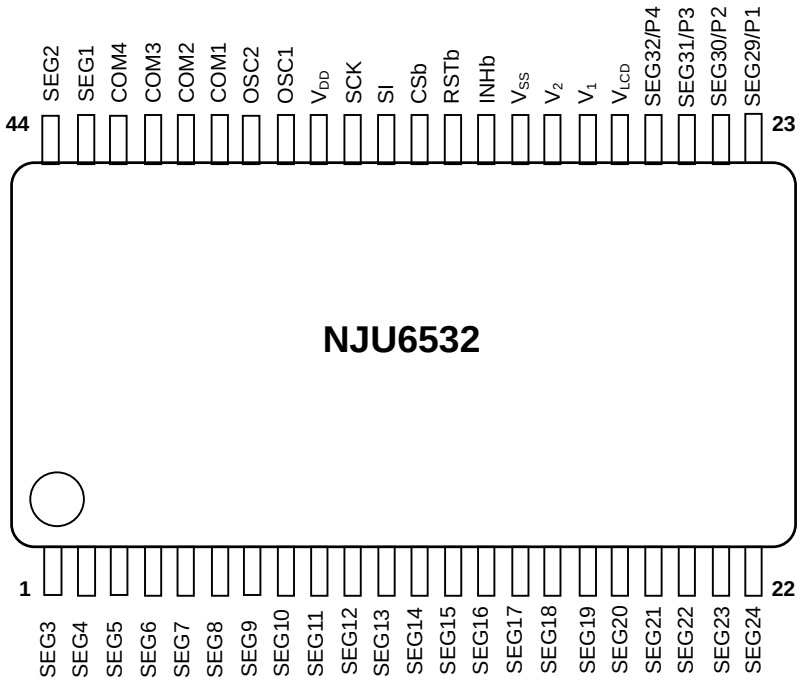
Preliminary

■ PIN CONFIGURATION

- LQFP48-R3



- SSOP44



■ TERMINAL DISCRIPTION

No.		Terminal	Function
LQFP48-R3	SSOP44		
46	36	V_{DD}	Power supply: 3V /5V
37	27	V_{LCD}	LCD driving voltage $V_{LCD} \geq V_1 \geq V_2 \geq V_{SS}$, $V_{LCD} \geq V_{DD}$
38, 39	28, 29	V_1, V_2	Bias At 1/3 bias ratio, keep V_1- V_2 open. At 1/2 bias ratio, short V_1- V_2.
40	30	V_{SS}	GND V_{SS} =0V
41	31	INHb	Display OFF * When INHb is "H", display is ON, and when INHb is "L", display is off. When SEG29(P1)~SEG32 (P4) are selected as general purpose output ports, even if input "0" to INHb terminal, SEG29~32 will still be recognized as general purpose output ports.
42	32	RSTb	Reset When RSTb is "L", command register and latch circuit is reset.
43	33	CSb	Chip select When CSb is "L", data can be read in.
44	34	SI	Serial data input (8 bit=1word)
45	35	SCK	Serial clock
47, 48	37, 38	OSC1, OSC2	External resistor connection terminal for CR oscillation, or external clock input terminal When external clock is used, input the signal to OSC1 and keep OSC2 open.
1~4	39~42	COM1 ~ COM4	Common driver outputs
5~28	43~44 1~22	SEG1 ~ SEG24	Segment driver outputs
29~32	-	SEG25 ~ SEG28	Segment driver outputs (Excluding SSOP44)
33~36	23~26	SEG29/P1 ~ SEG32/P4	Segment driver outputs/general purpose output ports These 4 terminals can be used as segment outputs or general purpose output ports by setting Command Register. When selected as general purpose ports, data can be outputted via these ports during COM1 timing. According to transferred data, "H"=V_{DD} or "L"=V_{SS} will be outputted.

*: For details about INHb, please refer to "**7 FUNCTION DESCRIPTION** (5) Display OFF function (INHb terminal)".

■ FUNCTION DESCRIPTION

(1) Block Function

(1-1) Oscillator

The oscillator includes a built-in capacitor and an external resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC1 and keep OSC2 open.

(1-2) Decoder

Input serial data is decoded and sent to the appropriate block.

(1-3) Command Register

Command data is written to this 8 bits command register to control **NJU6532** operation.

(1-4) Display Data Register

Data is written to this 8 bits register as display data.

(1-5) Latch Circuit

Data stored in display data register is assigned to the corresponding SEG/port.

(1-6) Segment Driver/General Purpose Ports

Basing on display data, segment drivers output LCD SEG driving signal.
And, SEG29/P1 ~ SEG32/P4 terminals can be selected as segment driver output or general-purpose ports by instruction.

(1-7) Common Driver

Common drivers output LCD COM driving signal.

(1-8) Reset Circuit

When RSTb="L", **NJU6532** is initialized.

(2) Serial data Transfer

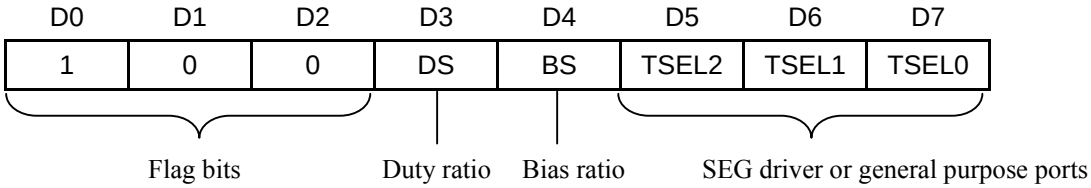
The transfer of data is conducted by synchronizing clock via interface with CPU. During CSb="L", serial data is obtainable and will be write in at the rising edge of SCK signal. The data is latched at falling edge of the CSb signal condition.
After CSb becoming low, address or command data is distinguished by the first 8bit data.
In the case of address data, the 2nd data can be transferred continually and interrupted as display data even if CSb maintained low.

(3) Command Register

Command Register is used to set the duty ratio, the bias ratio, and the SEG driver/general purpose ports. When the D0 to D2 bits of the 1st word are (1,0,0), the D3 ~ D7 bits are recognized as command data.
The contents of Command Register will be initialized as following when applying input signal to Reset terminal.

The Default Value of Command Register

- Duty ratio : 1/4
- Bias ratio : 1/3
- SEG driver/General purpose ports : SEG drivers(SEG32, SEG31, SEG30, SEG29)



- Duty Ratio

DS	Duty ratio
0	1/4
1	1/3

*) Do not change the duty ratio during display ON.

- Bias ratio

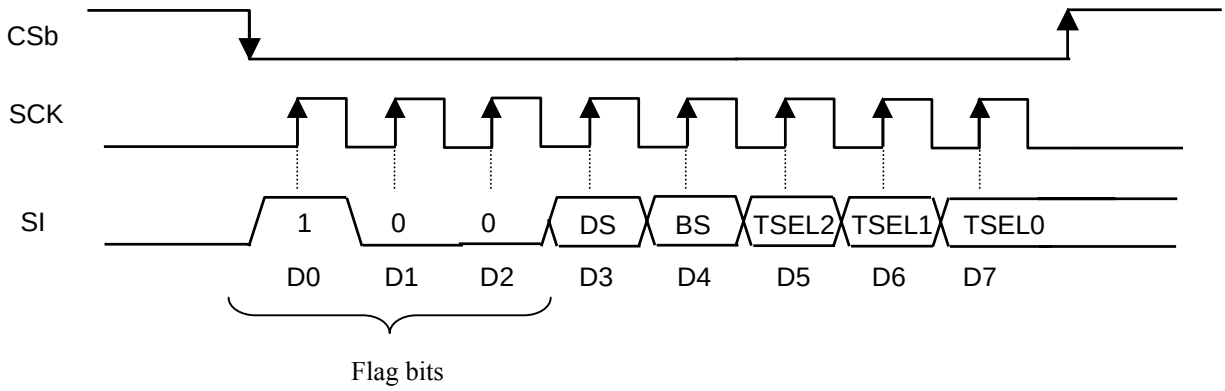
BS	Bias ratio
0	1/3
1	1/2

- SEG driver or general purpose ports

TSEL2	TSEL1	TSEL0	SEG29/P1	SEG30/P2	SEG31/P3	SEG32/P4
0	0	0	SEG29	SEG30	SEG31	SEG32
0	0	1	SEG29	SEG30	SEG31	P4
0	1	0	SEG29	SEG30	P3	P4
0	1	1	SEG29	P2	P3	P4
1	0	0	P1	P2	P3	P4

**) If TSEL2 ~ TSEL0 is set to (1, 0, 1), (1, 1, 0), (1, 1, 1) all outputs are used as segment drivers.

Timing of Serial Data Transfer



(4) Shift Register Select

Output Address Counter will specify the addresses of the SEG and COM drivers for the display data.
When the 8bits (D0 to D3, D6, D7) of the 1st data is "011100", the 8bits (D4, D5) specify the address of COM drivers, and after the 2nd data is display data which will be sent to the 1st –data –specified drivers.

- Address Data

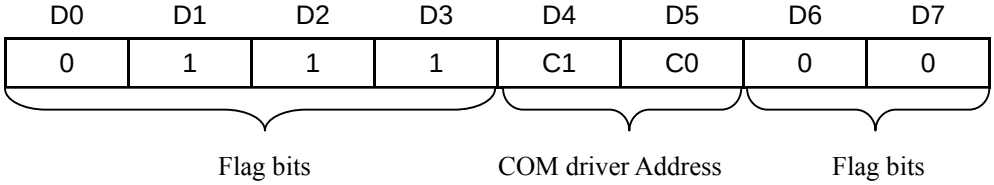


Table 1. The Relationship Between Output Address and SEG/COM Drivers

C1	C0	COM Driver	SEG Driver							
0	0	COM1	D8	D9	D10	D11	D12	D13	D14	D15
			SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
			D16	D17	D18	D19	D20	D21	D22	D23
			SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
			D24	D25	D26	D27	D28	D29	D30	D31
			SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
			D32	D33	D34	D35	D36	D37	D38	D39
			SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
0	1	COM2	D8	D9	D10	D11	D12	D13	D14	D15
			SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
			D16	D17	D18	D19	D20	D21	D22	D23
			SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
			D24	D25	D26	D27	D28	D29	D30	D31
			SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
			D32	D33	D34	D35	D36	D37	D38	D39
			SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
1	0	COM3	D8	D9	D10	D11	D12	D13	D14	D15
			SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
			D16	D17	D18	D19	D20	D21	D22	D23
			SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
			D24	D25	D26	D27	D28	D29	D30	D31
			SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
			D32	D33	D34	D35	D36	D37	D38	D39
			SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
1	1	COM4	D8	D9	D10	D11	D12	D13	D14	D15
			SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
			D16	D17	D18	D19	D20	D21	D22	D23
			SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
			D24	D25	D26	D27	D28	D29	D30	D31
			SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
			D32	D33	D34	D35	D36	D37	D38	D39
			SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32

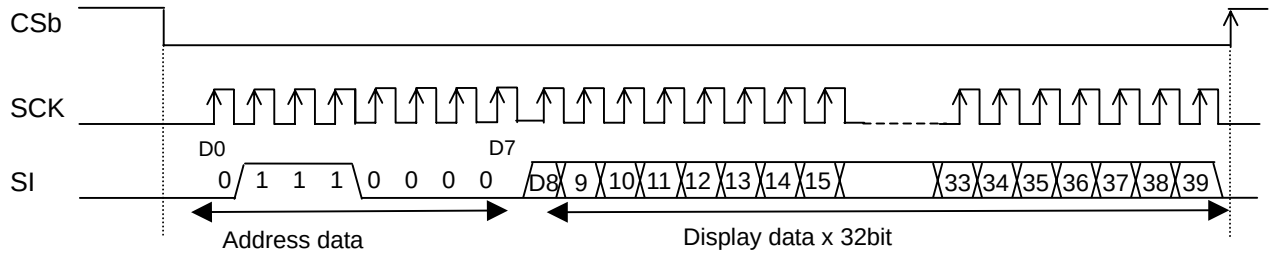
Increment Direction

- ✧ If general purpose ports are selected by Command Register, under (C1, C0)=(0, 0), D36 to D39 are the addresses of (P1, P2, P3, P4) ports which corresponds to (SEG29, SEG30, SEG31, SEG32).
- ✧ When SEG29~SEG32 are set as general purpose output ports, data for SEG29~SEG32 during COM2~COM4 scanning will be ignored.
- ✧ When duty ratio is 1/3, do not set address (C1, C0)=(1,1).
  Set to adress (C1, C0)=(1,1), It is not reflected in the display.

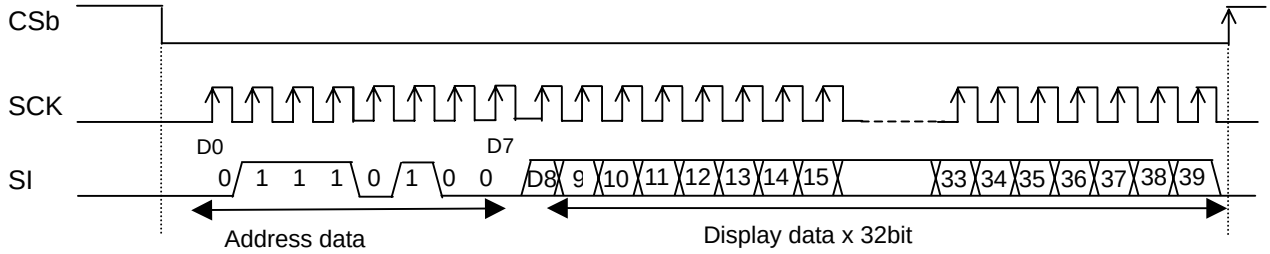
Input Data Format and Timing

Data format is shown below.
The data input is LSB first like as the order of D0, D1, D2, D3, D4, D5, D6, D7. The display data written in after choosing a shift register. (The data input is necessary though from D32 to D35 are not displayed in SSOP44.)

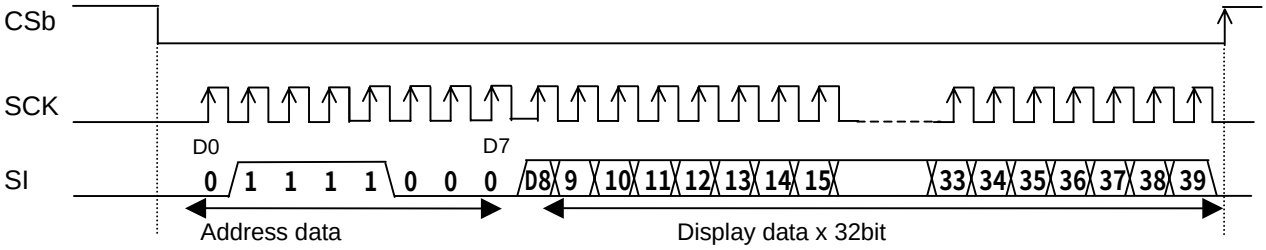
COM1 Display data



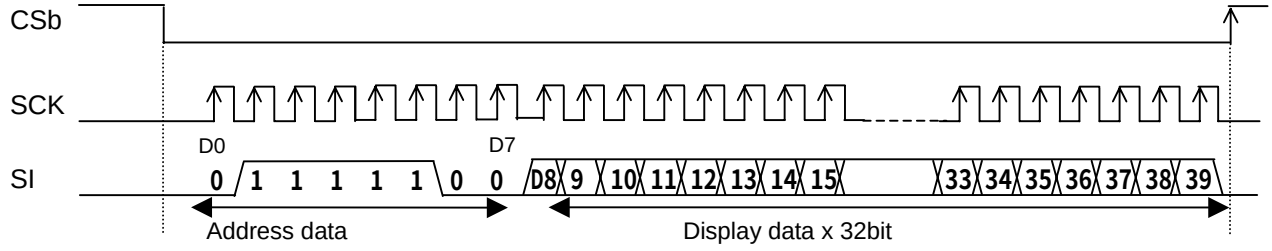
COM2 Display data



COM3 Display data



COM4 Display data



(5) Display OFF Function (INHb)
When INHb="L"

- All segment and common terminal output V_{SS}
  (When general purpose output ports are selected, even INHb="L", these ports can output data)
- Suspending Oscillation (but, if RSTb="L", oscillator works)
- V_1 and V_2 beome “H” (no current pass through the bleeder resistors)

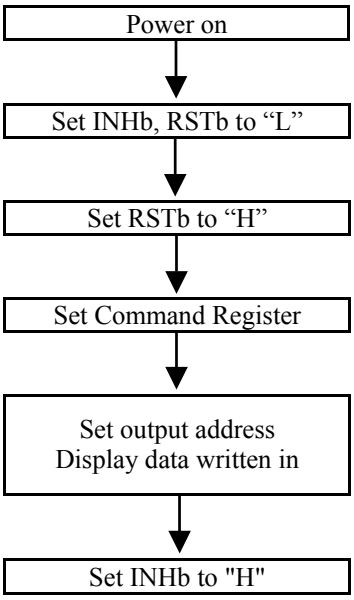
Even during INHb=”L”, interface can be accessed, and data can be written into the command register, address counter and data register.

(6) Initialization
Initialize Status.

- Display Data Register — all "0"
- Duty ratio — 1/4duty
- Bias ratio — 1/3 bias
- Segment/General purpose port: — Segment output(SEG32, SEG31, SEG30, SEG29)

(7) Sequence of Initialization

(7-1) 1/3duty, SEG32 used as general purpose port, data written in from COM2.



Pixels off, Hardware Reset executed.

When the “L” level input over 1.5ms to the RSTb terminal, reset Sequence is executed.

Release to Reset.

	D0	D1	D2	D3	D4	D5	D6	D7
	1	0	0	1	0	0	0	1

Duty ratio=1/3, SEG32 as general purpose port

	D0	D1	D2	D3	D4	D5	D6	D7
	0	1	1	1	0	1	0	0

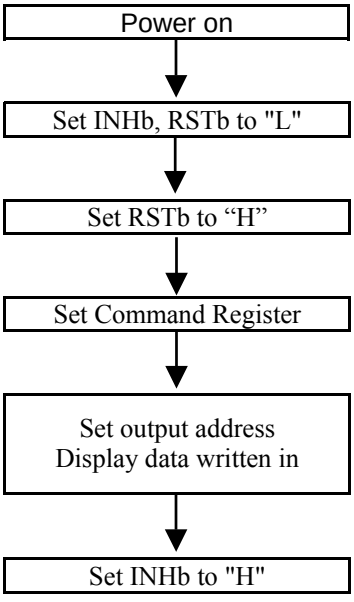
COM driver address=01

Display data writing from D8 to D39.

After the address is set, the display data should be written in the state of CS="L".
The address setting is reset by CS="H".

Pixels on

(7-2) 1/4duty, SEG29 ~ 32 used as SEG drivers, data written in for COM1.



Pixels off, Hardware Reset executed.

When the “L” level input over 1.5ms to the RSTb terminal, reset Sequence is executed.

Release to Reset.

	D0	D1	D2	D3	D4	D5	D6	D7
	1	0	0	0	0	0	0	0

Duty ratio =1/4

	D0	D1	D2	D3	D4	D5	D6	D7
	0	1	1	1	0	0	0	0

COM driver address =00

Display data writing from D8 to D39.

After the address is set, the display data should be written in the state of CS="L".
The address setting is reset by CS="H".

Pixels on

■ ABSOLUTE MAXIMAM RATINGS

(V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply Voltage 1	V_{DD}	-0.3 ~ +6.0	V	
Supply Voltage 2	V_{LCD}	-0.3 ~ +13.5	V	
Supply Voltage 3	V_1, V_2	-0.3 ~ V_{LCD}+0.3	V	
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V	INHb, CSb, SCK, SI, RSTb, OSC1 applicable.
Operating Temp.	Topr	-40 ~ +105	°C	
Storage Temp.	Tstg	-55 ~ +125	°C	
Dissipation Power	P_D	1000(LQFP48-R3) 800(SSOP44)	mW	The power dissipation is value mounted on a glass epoxy board in size: 76.2mm x114.3mm x1.6mm (LQFP48-R3, SSOP44).

Note-1) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used within the range specified in the DC electrical characteristics, or the electrical stress may cause mulfunctions and impact on the reliability.

Note-2) All voltages are relative to V_{SS} = 0V reference.

Note-3) The following relationship shall be maintained.
$V_{LCD} \geq V_1 \geq V_2 \geq V_{SS}$, $V_{LCD} \geq V_{DD}$, and V_{LCD} shall be input after V_{DD}.

Note-4) To stabilize the LSI operation, place decoupling capacitors between V_{DD}-V_{SS} and between V_{LCD}-V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• DC characteristics 1

(V_{DD}=2.7 to 3.6V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply	V_{DD}		2.7		3.6	V	
LCD Driving Voltage	V_{LCD}	$V_{LCD} \geq V_{DD}$	2.7		8.0	V	
LCD Bias Voltage	V_1	Ta=25°C Testing via COM/SEG terminals COM/SEG without load	2/3 V_{LCD}-0.2	2/3 V_{LCD}	2/3 V_{LCD}+0.2	V	
	V_2		1/3 V_{LCD}-0.2	1/3 V_{LCD}	1/3 V_{LCD}+0.2	V	
"H" Level Input Voltage	V_{IH}	INHb, CSb, SCK, SI, RESb, OSC1	0.8 V_{DD}		V_{DD}	V	
"L" Level Input Voltage	V_{IL}	INHb, CSb, SCK, SI, RESb, OSC1	0		0.2 V_{DD}	V	
Hysteresis Voltage	V_H	INHb, CSb, SCK, SI, RESb		0.2V_{DD}		V	
"H" Level Input Current	I_{IH}	V_{IN}= V_{DD} INHb, CSb, SCK, SI, RESb			1.0	μA	
"L" Level Input Current	I_{IL}	V_{IN}= V_{SS} INHb, CSb, SCK, SI, RESb			1.0	μA	
"H" Level Output Voltage	V_{OH}	V_{DD} =3V, V_{LCD}=5.5V, I_O=-5mA, P1 to P4	V_{DD}-0.6			V	
"L" Level Output Voltage	V_{OL}	V_{DD} =3V, V_{LCD}=5.5V, I_O=5mA, P1 to P4			0.6	V	
Driver-on Resistance (COM)	R_{COM}	±Id=1μA, V_{LCD}=3V/5.5V	-	-	10	kΩ	5
Driver-on Resistance (SEG)	R_{SEG}	±Id=1μA, V_{LCD}=3V/5.5V	-	-	10	kΩ	5
Oscillating Frequency	f_{OSC}	V_{DD} =3V, R_{OSC}=1.1MΩ, Ta=25°C	6.3	7.9	9.1	kHz	
External Clock Frequency	f_{CP}	Input into OSC1	5.13	-	46.2	kHz	
External Clock Duty	duty	Input into OSC1	45	50	55	%	
Bleeder Resistor	R_B	V_{LCD}-V_{SS} Ta=25°C	127	150	173	kΩ	
Operating Current	I_{DD1}	V_{DD} =3V, INHb="L", RSTb="H", Ta=25°C		0.1	1.0	μA	
	I_{DD2}	V_{DD} =3V, V_{LCD}=5V, Ta=25°C, Checker flag display, 1/3 bias Using internal oscillator, no output		4.0	10	μA	
	I_{LCD1}	V_{DD}=3V, V_{LCD}=5V, RSTb="H", INHb="L", Ta=25°C		0.1	1.0	μA	
	I_{LCD2}	V_{DD} =3V, V_{LCD}=5V, Ta=25°C, Checker flag display, 1/3 bias Using internal oscillator, no output		34	60	μA	

Note-5) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_{LCD}, V_{SS}, V_1 or V_2 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.

Note-6) ["H" Level Input Voltage], ["L" Level Input Voltage], [Hysteresis Voltage], ["H" Level Input Current], ["L" Level Input Current], [External Clock Frequency] and [External Clock Duty] are as the same as if V_{DD}=4.5 to 5.5V.

- DC characteristics 2

(V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYM BOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply	V_{DD}		4.5		5.5	V	
LCD Driving Voltage	V_{LCD}	$V_{LCD} \geq V_{DD}$	4.5		8.0	V	
LCD Bias Voltage	V_1	Ta=25°C Testing via COM/SEG terminals COM/SEG without load	2/3 V_{LCD}-0.2	2/3 V_{LCD}	2/3 V_{LCD}+0.2	V	
	V_2		1/3 V_{LCD}-0.2	1/3 V_{LCD}	2/3 V_{LCD}+0.2	V	
"H" Level Input Voltage	V_{IH}	INHb, CSb, SCK, SI, RESb, OSC1	0.8V_{DD}		V_{DD}	V	
"L" Level Input Voltage	V_{IL}	INHb, CSb, SCK, SI, RESb, OSC1	0		0.2 V_{DD}	V	
Hysteresis Voltage	V_H	INHb, CSb, SCK, SI, RESb		0.2V_{DD}		V	
"H" Level Input Current	I_{IH}	V_{IN}= V_{DD} INHb, CSb, SCK, SI, RESb			1.0	µA	
"L" Level Input Current	I_{IL}	V_{IN}= V_{SS} INHb, CSb, SCK, SI, RESb			1.0	µA	
"H" Level Output Voltage	V_{OH}	V_{DD} =5V, V_{LCD}=5.5V, I_O=-10mA, P1 to P4	V_{DD}-1.0			V	
"L" Level Output Voltage	V_{OL}	V_{DD} =5V, V_{LCD}=5.5V, I_O=10mA, P1 to P4			1.0	V	
Driver-on Resistance (COM)	R_{COM}	±Id=1µA, V_{LCD}=4.5V/5.5V	-	-	10	kΩ	7
Driver-on Resistance (SEG)	R_{SEG}	±Id=1µA, V_{LCD}=4.5V/5.5V	-	-	10	kΩ	7
Oscillating Frequency	f_{OSC}	V_{DD} =5V, R_{OSC}=1.2MΩ, Ta=25°C	6.3	7.9	9.1	kHz	
External Clock Frequency	f_{CP}	Input into OSC1	5.13		46.2	kHz	
External Clock Duty	duty	Input into OSC1	45	50	55	%	
Bleeder Resistor	R_B	V_{LCD}-V_{SS} Ta=25°C	127	150	173	kΩ	
Operating Current	I_{DD1}	V_{DD} =5V, INHb="L", RSTb="H", Ta=25°C		0.1	1.0	µA	
	I_{DD2}	V_{DD} =5V, V_{LCD}=5V, Ta=25°C, Checker flag display, 1/3 bias Using internal oscillator, no output		10	20	µA	
	I_{LCD1}	V_{DD} =5V, V_{LCD}=5V, INHb="L", RSTb="H",Ta=25°C		0.1	1.0	µA	
	I_{LCD2}	V_{DD} =5V, V_{LCD}=5V, Ta=25°C, Checker flag display, 1/3 bias Using internal oscillator, no output		34	60	µA	

Note-7) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_{LCD}, V_{SS}, V_1 or V_2 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.

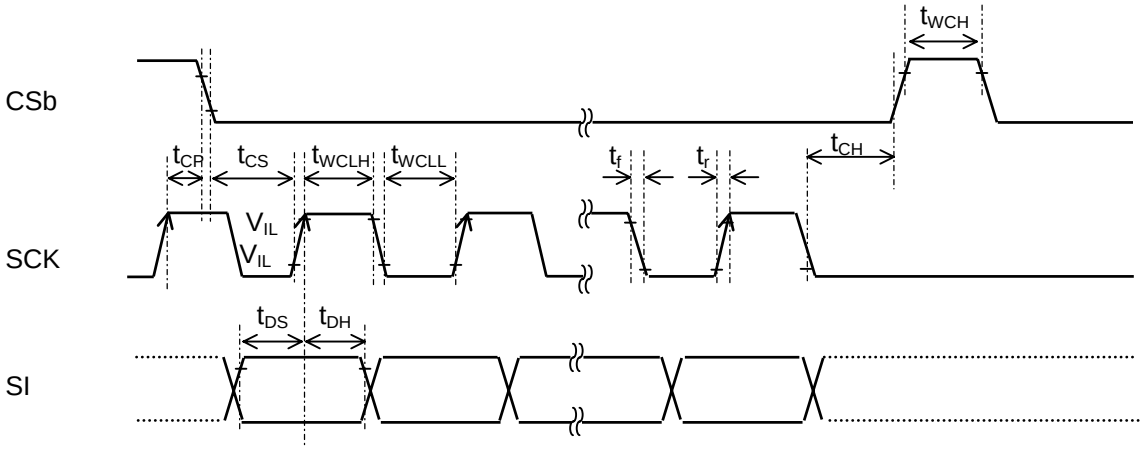
Note-8) ["H" Level Input Voltage], ["L" Level Input Voltage], [Hysteresis Voltage], ["H" Level Input Current], ["L" Level Input Current], [External Clock Frequency] and [External Clock Duty] are as the same as if V_{DD}=2.7 to 3.6V.

- AC characteristics

(V_{DD}=V_{LCD}=2.7 to 5.5V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
"L" Level Clock Pulse Width	t_{WCLL}		230			ns	
"H" Level Clock Pulse Width	t_{WCLH}		230			ns	
Data Setup Time	t_{DS}		60			ns	
Data Hold Time	t_{DH}		60			ns	
CSb Setup Time	t_{CS}		150			ns	
CSb Hold Time	t_{CH}		150			ns	
CSb"H" Level Pulse Width	t_{WCH}		150			ns	
Rising Time	t_r				20	ns	
Falling Time	t_f				20	ns	

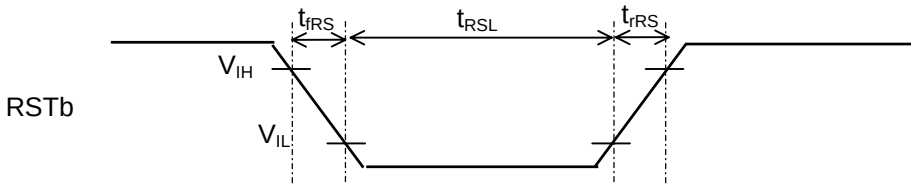
- Input Timing



- Input condition when hardware reset circuit is used

(Ta=-40 to 105°C)

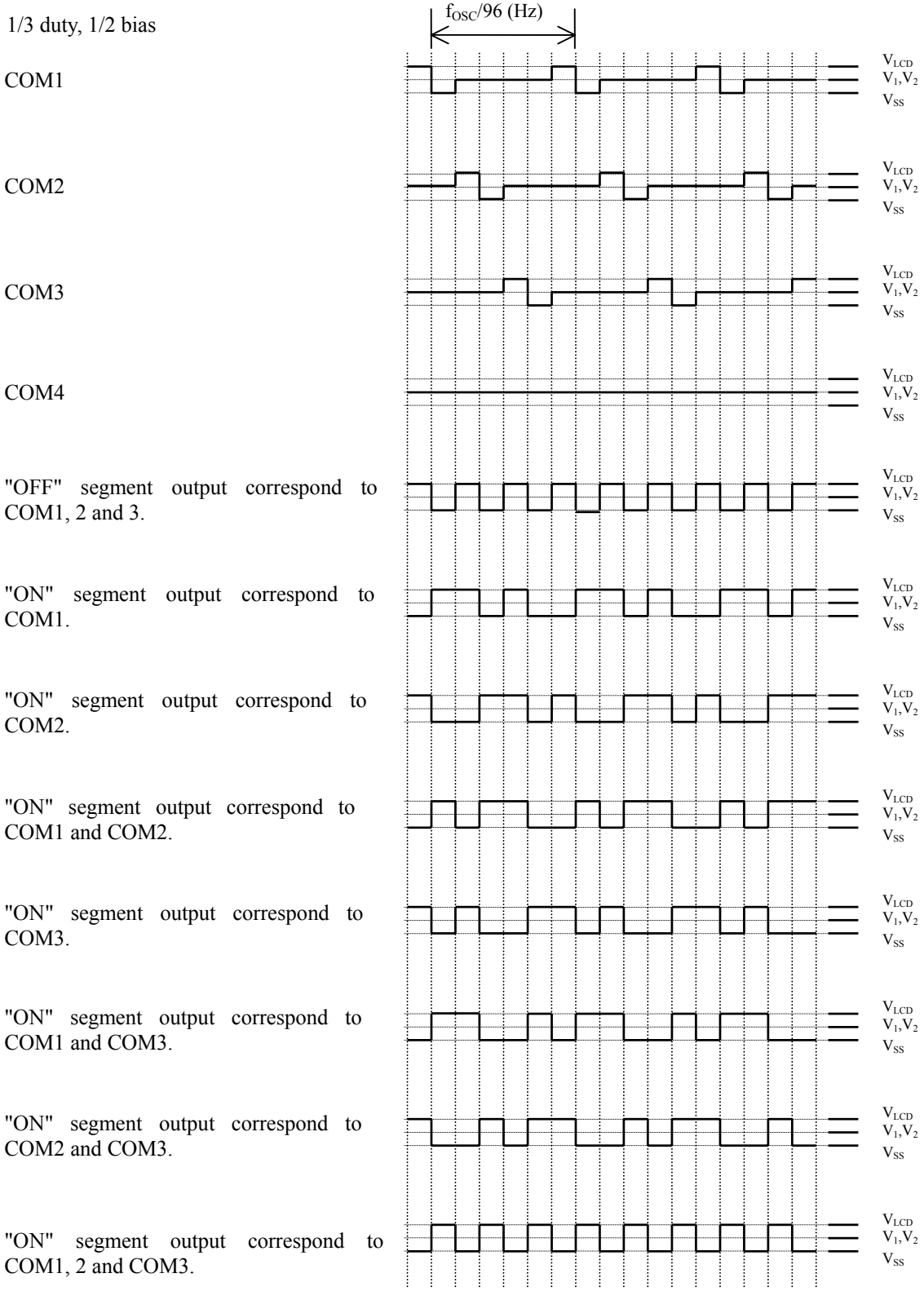
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reset Input “L” Level Width	t_{RSL}	f_{OSC}= 7.7kHz	1.5			Ms
Reset Rising Time	t_{rRS}				100	Ns
Reset Falling Time	t_{fRS}				100	Ns



Input the external clock when you use hardware reset when the external clock is input.
Internal is not reset for the clock not to be input.
The width of reset is changeable depend on the oscillatory frequency.

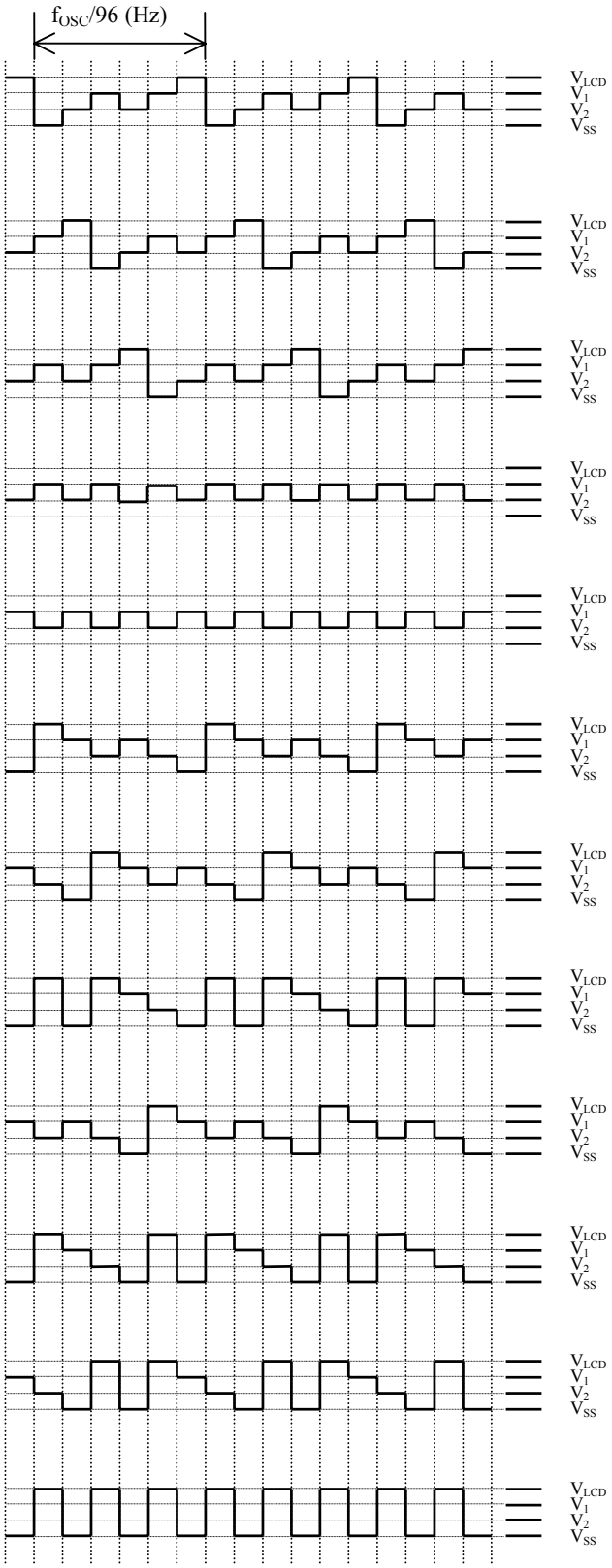
■ LCD DRIVING WAVEFORM

(a) 1/3 duty, 1/2 bias



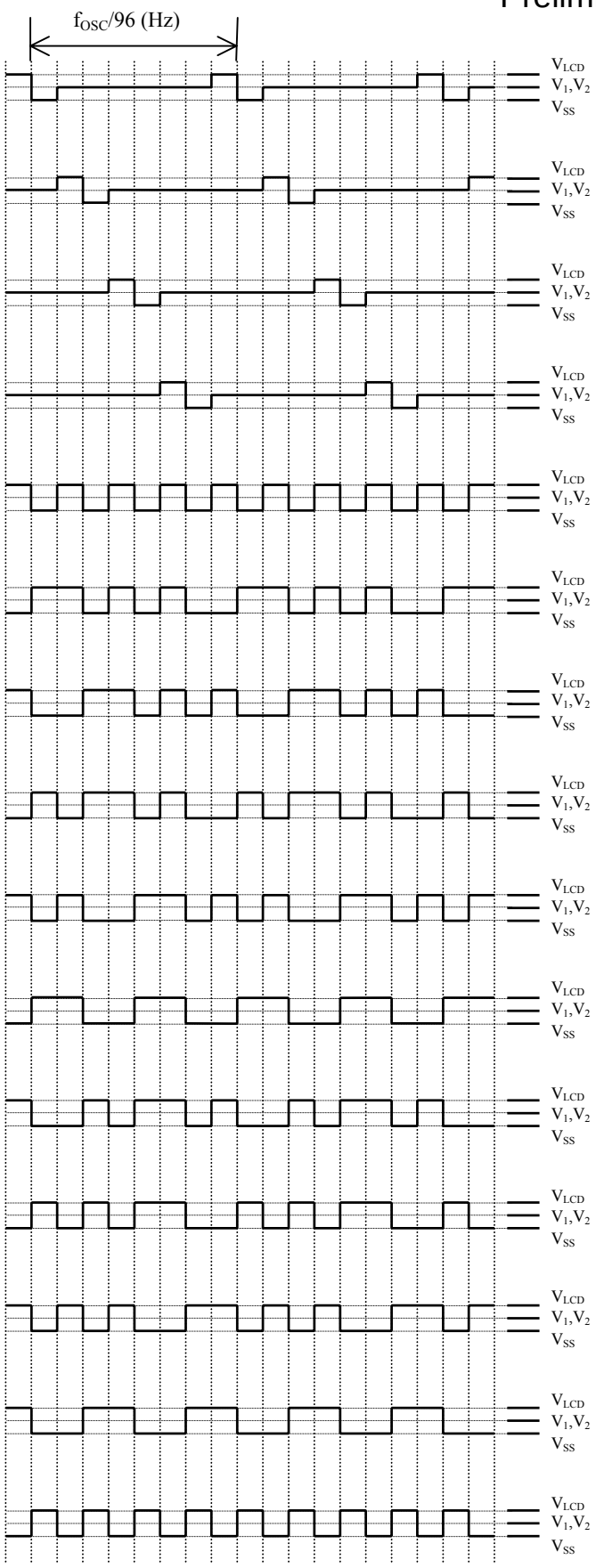
1/3 duty, 1/2 bias

(b) 1/3 duty, 1/3 bias



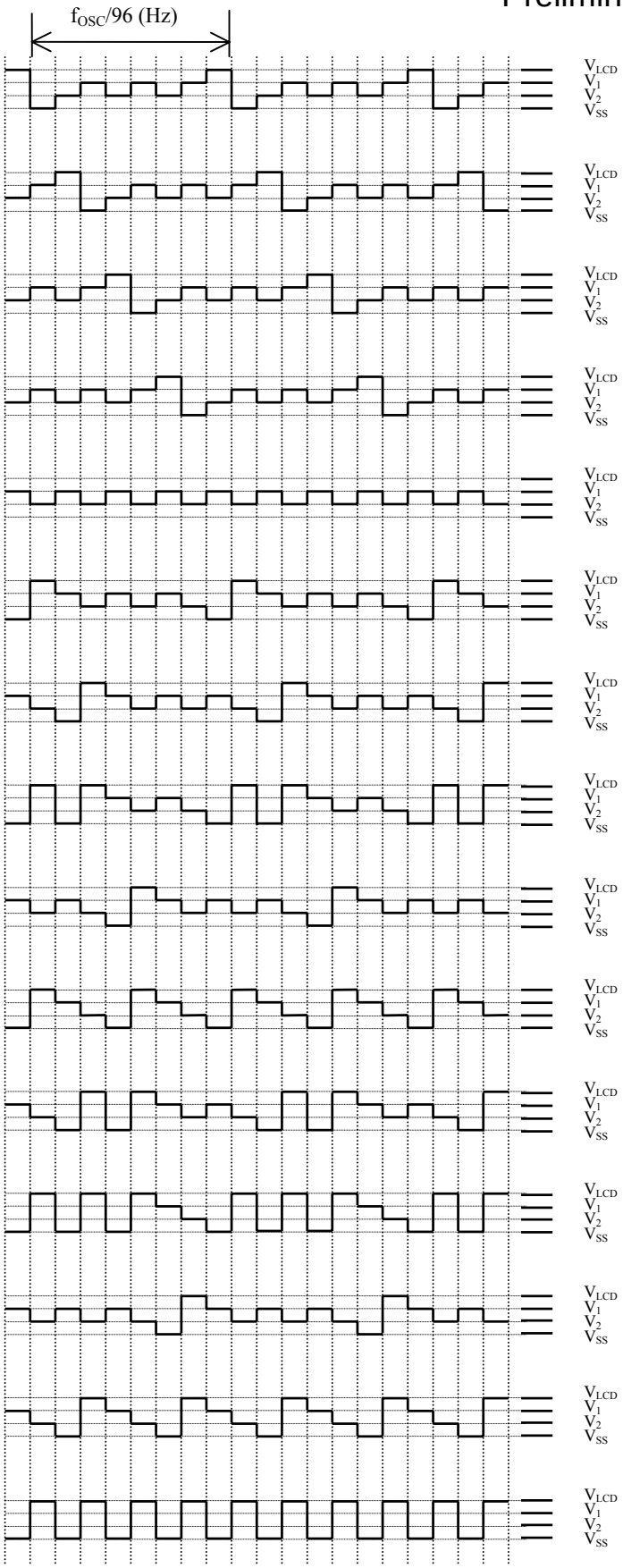
1/3 duty, 1/3 bias

(c) 1/4 duty, 1/2 bias



1/4 duty, 1/2 bias

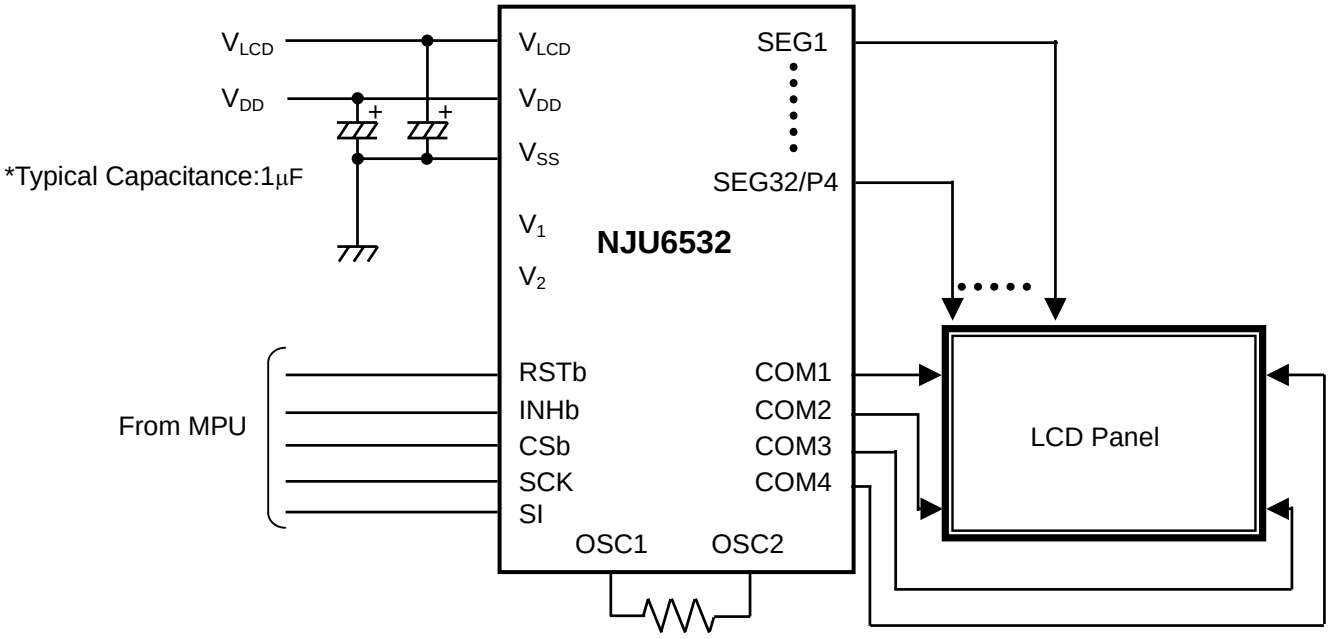
(d) 1/4 duty, 1/3 bias



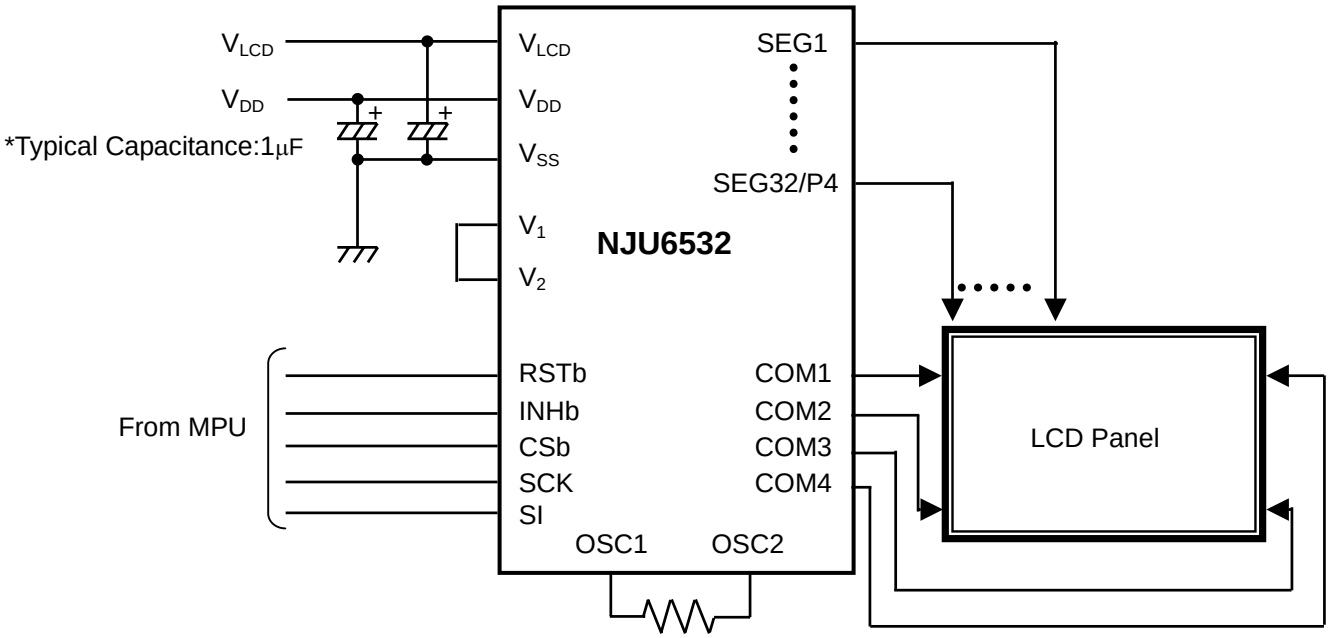
1/4 duty, 1/3 bias

■ APPLICATION CIRCUIT

• 1/4 duty, 1/3 bias



• 1/4 duty, 1/2 bias



Note) Because display data is not yet stable just after V_{DD} on, if LCD panel is turned on, unexpected pattern will be displayed, therefore, keep INHb terminal to "L" level until data transfer from MPU is over.