Quad PIN-Electronics Drivers / Comparators / Analog Switches

■ GENERAL DESCRIPTION

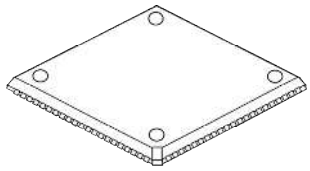
NJU6496 includes four-channel PIN Driver, Comparator, and Analog Switch for kelvin connection. It is designed specifically for Test During Burn-In (TDBI) applications where cost, functional density, and power are all at a premium. Driver is able to set up threshold voltage, and control high level and low level output voltage, and high impedance independently. Comparator is able to control threshold voltage independently at each channel, and set up high level and low level output voltage. Analog Switch that includes two switches for a SENSE and FORCE in each channel is a switch for making Kelvin connection for current detection.

This device has a 15V driver output range and comparator input range. NJU6496 is suitable for an interface to circuits, such as TTL, ECL, CMOS (3V, 5V and 7V), and LVCMOS, not only various tests of a Flash Devices.

■ FEATURES

- 15V Input and Output Voltage Range
- Low Consumption Current
- Low Output Leakage Current : Ileak<2nA
- 45 MHz Operation
- Driver DC Output Current : Io=125mA
- Package : QFN84-D4 (10.2mm x 10.2mm , t=0.2mm)
- CMOS Structure

■PACKAGE OUTLINE

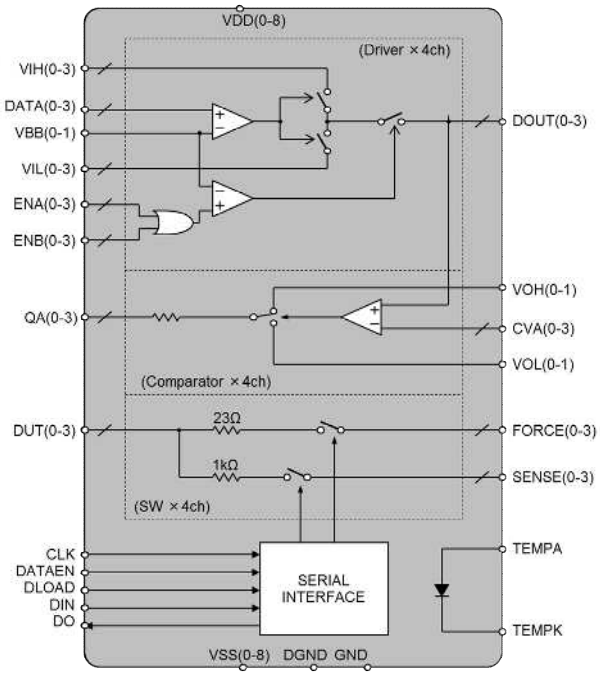


NJU6496KD4

■ APPLICATION

- Burn-In Testers
- ATE
- Measuring Instrument

■ BLOCK DIAGRAM

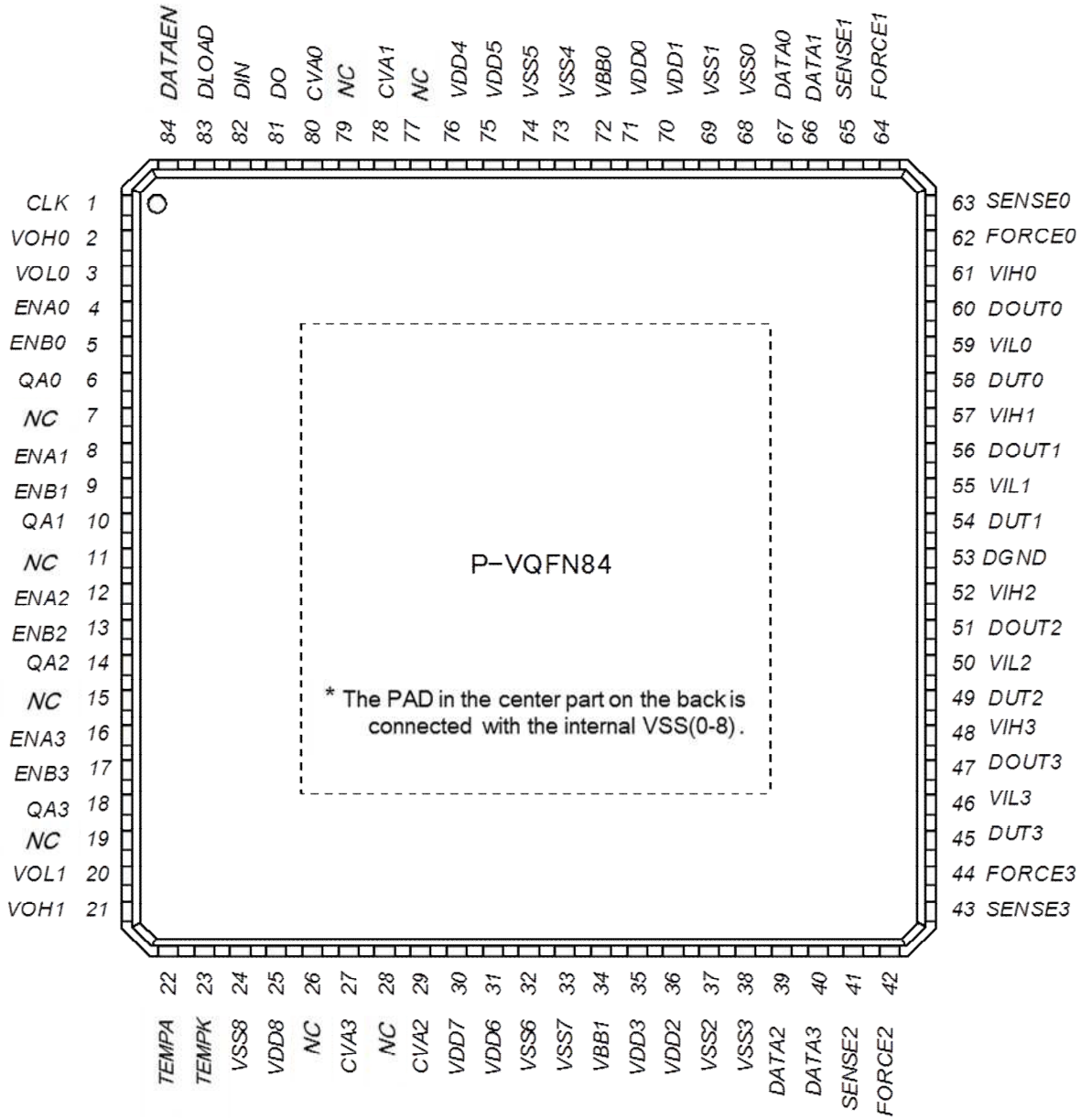


*1) Driver, Comparator and SW shows per 1 channel.

*2) (0-3) is applied to one of a figure 0 to 3, and it shows each channel.

*3) (0-1) and (0-8) is applied to one of a 0 to 1 or 0 to 8, and it is shortened within the IC.

■ **PIN INFORMATION**



No	Symbol	Function
39,40,66,67	DATA(0-3)	Driver Mode Input (0-3ch)
4,8,12,16 5,9,13,17	ENA(0-3) ENB(0-3)	Driver Output Enable / Hi-Z Setting Input(0-3ch)
47,51,56,60	DOUT(0-3)	Driver Output, Comparator Input(0-3ch)
48,52,57,61	VIH(0-3)	Driver Output High Level Voltage Input (0-3ch)
46,50,55,59	VIL(0-3)	Driver Output Low Level Voltage Input (0-3ch)
34,72	VBB(0-1)	Driver Input (DATA,EN) Threshold Voltage Input
27,29,78,80	CVA(0-3)	Comparator Threshold Voltage Input (0-3ch)
2,21	VOH(0-1)	Comparator Output High Level Voltage Input
3,20	VOL(0-1)	Comparator Output Low Level Voltage Input
6,10,14,18	QA(0-3)	Comparator Output (0-3ch)
45,49,54,58	DUT(0-3)	DUT Connecting (0-3ch)
41,43,63,65	SENSE(0-3)	PMU Sense Connecting (0-3ch)
42,44,62,64	FORCE(0-3)	PMU Force Connecting (0-3ch)
81	DO	Serial Data Output
82	DIN	Serial Data Input
83	DLOAD	Serial Data Load
84	DATAEN	Serial Data Input Enable
1	CLK	Serial Data Input Clock
25,30,31,35,36,70,71,75,76	VDD(0-8)	Positive Power Supply
24,32,33,37,38,68,69,73,74	VSS(0-8)	Negative Power Supply
22	TEMPA	Thermal Diode (Anode)
23	TEMPK	Thermal Diode (Cathode)
53	DGND	Digital GND
7,11,15,19,26,28,77,79	NC	not connected to internal circuits

■ ABSOLUTE MAXIMUM RATINGS (Ta=25˚C)

PARAMETER	SYMBOL	CONDITION	RATINGS	UNIT
Supply Voltage	V_{DD} - V_{SS}	V_{DD},V_{SS} total Voltage	17.0	V
Input Voltage	V_{IN}	Each Input Terminal	V_{SS} – 0.3 to V_{DD} (Note1)	V
Power Dissipation	P_D	(Note2)	4400	mW
Output Current	I_{OUT}		130	mA
Operating Temperature Range	T_{opr}		-20 to +85	
Storage Temperature Range	T_{stg}		-40 to +150	˚C

(Note 1) For supply voltage less than 17V, the maximum input voltage is equal to the supply voltage.

(Note 2) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers) Back side center PAD mounting
(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATION CONDITIONS (Ta=25˚C)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply	V_{DD} - V_{SS}	10.0 to 15.0 (total)	V

■ ELECTRICAL CHARACTERISTICS

VDD=10V, VSS=－3V, VBB=1.5V, DATA=1.5±1.5V, VIH=5V,VIL=0V, ENA=ENB=0V, CL=33pF, RL=1kΩ, Ta=25˚C unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Driver DC Characteristics						
High Level Output Voltage	D_{OUTH}	DATA=5.0V	4.75	-	-	V
Low Level Output Voltage	D_{OUTL}	DATA=0V	-	-	0.25	V
Output Leak Current (HiZ)	Ileak	ENA=3V, DUT=9.5V or –3V	-2	-	2	nA
Output Resistance	Rout		19.8	22.8	25.8	Ω
DC Output Current (source)	Isource DC		125	-	-	mA
DC Output Current (sink)	Isink DC		125	-	-	mA
High Level Input Voltage	V_{IH}		2.0	-	-	V
Low Level Input Voltage	V_{IL}		-	-	1.0	V
Input Bias Current	Iin		-100	-	100	nA
Driver AC Characteristics (f=10MHz)						
Propagation Delay						
DATA to DUT Fig.1	Tpdr,Tpdf	VIH=3V, VIL=0V	15.4	16.9	18.4	ns
EN to DUT (Active to HiZ) Fig.2	Taz	VIH=3V, VIL=0V, DATA=3 .0V, ENA=0V to 3.0V,f =500kHz	18	19.5	21	ns
EN to DUT (HiZ to Active) Fig.2	Tza	VIH=3V, VIL=0V, DATA=3 .0V, ENA=3.0V to 0V,f =500kHz	15.5	17.0	18.5	ns
Propagation Delay Mismatch Fig.1	|Tpdr - Tpdf |	VH=3V, VL=0V	-	-	1	ns

VDD=10V, VSS= -3V, VBB=1.5V, DATA=1.5±1.5V 10MHz, VIH=3V,VIL= 0V, ENA=ENB=0V, CL=33pF, RL=1kΩ,Ta=25°C, unless otherwise noted

PARAMETER		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Driver AC Characteristics (f=10MHz)							
Rise / Fall Time							
1V Swing	Fig.3	Tr 1/ Tf1	VIH=1V, VIL=0V, 20% to 80%	-	4.8	11.0	ns
3V Swing	Fig.3	Tr 3/ Tf3	VIH=3V, VIL=0V, 10% to 90%	-	6.7	15.5	ns
5V Swing	Fig.3	Tr 5/ Tf5	VIH=5V, VIL=0V, 10% to 90%	-	6.8	15.5	ns
10V Swing	Fig.3	Tr 10/ Tf10	VIH=10V, VIL=0V,10% to 90%	-	7.2	-	ns
15V Swing	Fig.3	Tr15 / Tf15	VDD=12V ,VIH=12V VIL=－3V, 10% to 90%	-	7.4	-	ns
Rise / Fall Time Mismatch	Fig.3	| Tr - Tf |		-	-	2	ns
Overshoot, Undershoot, Preshoot		Vshoot	VIH=3V, VIL=0V,CL=33pF	-	150	-	mV
Max. Operating Frequency	Fig.4	Fmax	VIH=5V, VIL=0V	45	-	-	MHz
Min. Pulse Width	Fig.4	Tpw	VIH=5V, VIL=0V	-	-	11	ns

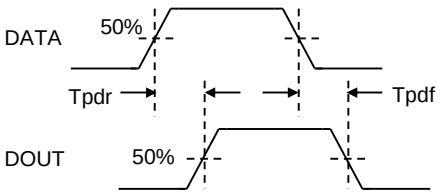


Fig.1

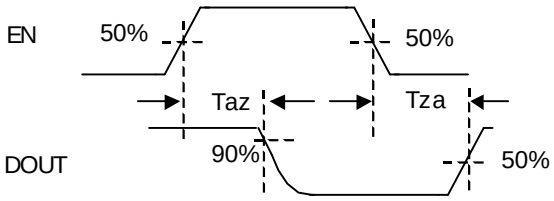


Fig.2

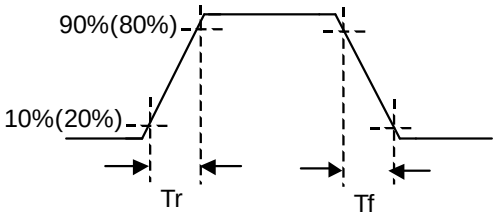


Fig.3

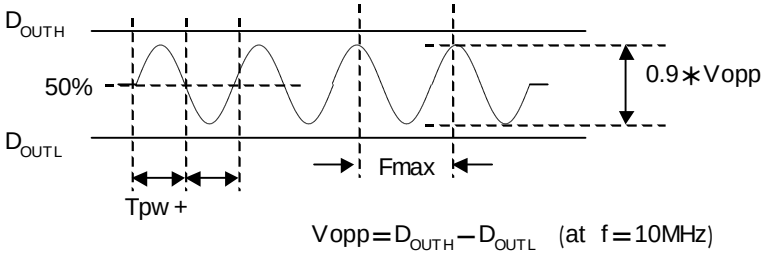


Fig.4

VDD=10V, VSS= -3V, ENA=ENB=3V, CVA=1.5V, DOUT=1.5±1.5V 10MHz, VOH=3V, VOL= 0V, CL=33pF, RL=1kΩ, Ta=25°C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Comparator DC Characteristics						
High Level Output Voltage	Vch		2.75	3.0		V
Low Level Output Voltage	Vcl			0	0.25	V
Input Offset Voltage	Voff		-50	0	50	mV
Output Resistance	Rcout		25	35	45	Ω
Comparator AC Characteristics						
Propagation Delay						
DUT to QA,QB	Tcpdr, Tcpdf		9	12	15	ns
Overdrive Voltage Variation	ΔTpd/ ΔDUTamp1	DOUT=1.5V±[100mV〜1V]	-	8	10	ns/V
	ΔTpd/ ΔDUTamp2.5	DOUT=1.5V±[1V〜2.5V]	-	0.8	1.5	ns/V
Common Voltage Variation	ΔTpdcm	CVA=0V〜3.0V, DOUT=CVA±1.5V	-	-	2	ns
Propagation Delay Mismatch	|Tcpdr-Tcpdf|		-	-	2	ns
Others						
Rise / Fall Time Fig.3	Tcr / Tcf	10% to 90%	-	3.0	-	ns
Max. Operating Frequency Fig.4	Fmax	VOH=3V, VOL=0V	60	-	-	MHz
Min. Pulse Width Fig.4	Tpw	VOH=3V, VOL=0V	-	-	8	ns

VDD=10V, VSS= -3V, Ta=25°C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Analog Switch Characteristics						
FORCE Switch Resistance	Rf	V_{FORCE}=0V, I_{DUT}=10mA	18	23	28	Ω
SENSE Switch Resistance	Rs	V_{SENSE}=0V, I_{DUT}=1mA	0.7	1	1.3	kΩ
FORCE Capacitance	Cf	SW open		9		pF
SENSE Capacitance	Cs	SW open		8		pF
DUT Capacitance	Cd	SW open		10		pF
Switch Current Leakage	Iswleak	V_{DUT}=0V, V_{SENSE}=-3 or 9.5V, V_{FORCE}=-3 or 9.5V	-2	-	2	nA

VDD=10V, VSS= -3V, VBB=1.5V, DATA=0V, VIH=3V, VIL=0V, ENA=ENB=0V, RL=1kΩ, CL=33pF, CVA=1.5V, VOH=3V, VOL=0V, Ta=25˚C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supplies						
Positive Power Supply DC Current	I_{DD}	No Signal	-	45	65	mA
Negative Power Supply DC Current	I_{SS}	No Signal	-65	-45	-	mA

VDD=10V, VSS= -3V, Ta=25˚C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Data Interface						
Setup Time	Tst		-	200	-	ns
High Level Data Pulse Width Fig.5	Tpwh		-	33	-	ns
Low Level Data Pulse Width Fig.5	Tpwl		-	33	-	ns
DATAEN Low Hold Timing Fig.5	Tcel		5	-	20	ns
DATAEN High Hold Timing Fig.5	Tceh		5	-	20	ns
CLK Max. Input Frequency	Fclk		15	-	-	MHz
DO Output Propagation Delay Fig.5	Tco		-	-	30	ns
Max. Logic Setting Time Fig.5	Tel		-	20	-	ns
DLOAD Data Pulse Width Fig.5	Tlw		30	-	-	ns
High Level Input Voltage	Vdh		2.4	-	10	V
Low Level Input Voltage	Vdl		-3	-	0.6	V
DO Rise / Fall Time	Trdo, Tfdo	CL=10pF	-	6	-	ns

■ TRUTH TABLES

Driver

DATA, ENA, ENB	Status
≧VBB+0.5V	H
≦VBB-0.5V	L

ENA	ENB	DATA	DOUT
H	X	X	HiZ(OPEN)
X	H	X	HiZ(OPEN)
L	L	H	VIH
L	L	L	VIL

Comparator

DOUT	Status
≧CVA+0.1	H
≦CVA-0.1	L

DOUT	QA
H	VOH
L	VOL

■ SWITCH CONTROL

Timing Table

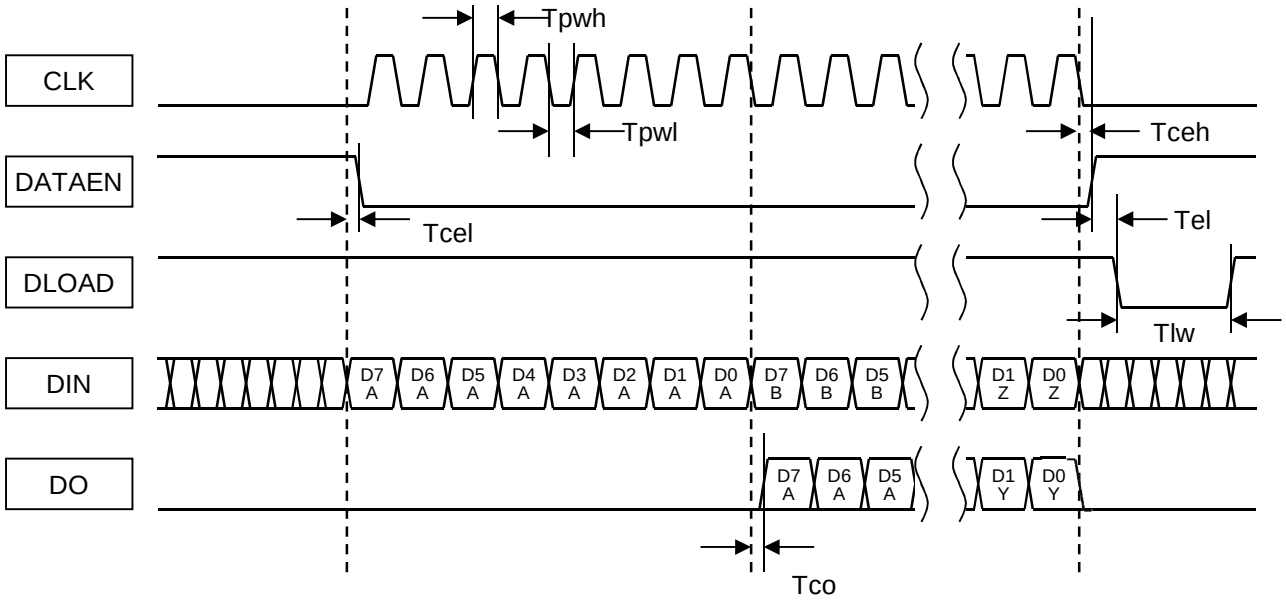


Fig.5 Data Input Timing Table

Input Data Table

DATA	FUNCTION	BIT STATE		DEFAULT
		0	1	
D0	CH3 FORCE SW	OPEN	CLOSE	0
D1	CH3 SENSE SW	OPEN	CLOSE	0
D2	CH2 FORCE SW	OPEN	CLOSE	0
D3	CH2 SENSE SW	OPEN	CLOSE	0
D4	CH1 FORCE SW	OPEN	CLOSE	0
D5	CH1 SENSE SW	OPEN	CLOSE	0
D6	CH0 FORCE SW	OPEN	CLOSE	0
D7	CH0 SENSE SW	OPEN	CLOSE	0

Data Interface

NJU6496 includes the serial interface for analog switch control.
This serial interface consists of an 8-bit shift register and a switch control register.
Data input is CLK, DATAEN, DLAOD, and DIN, and a data output is DO.

- Data input
  While DATAEN is set as LOW, data input and an output will be in an active state.
  DIN is loaded to a shift register by the rising edge of CLK.

- Data output
  The data of a shift register is outputted through DO.
  DO is a buffer output of the last bit of a shift register, and is outputted with the voltage level of VDD and VSS.
  It is possible to carry out daisy chain connection of multiple devices using DO.

- Loading of switch (or Switch Loading)
  The load timing of an analog switch is controlled by DLOAD.
  The data of a shift register is loaded to a switch control register with the falling edge of DLOAD, and the state of an analog switch is changed.
  The data loaded to the switch control register holds data, as long as there is no rewriting of data.

- OFF state
  While DATAEN is set as HIGH, data is not loaded but DO is simultaneously fixed to LOW.
  Moreover, it is not necessary to input CLK.

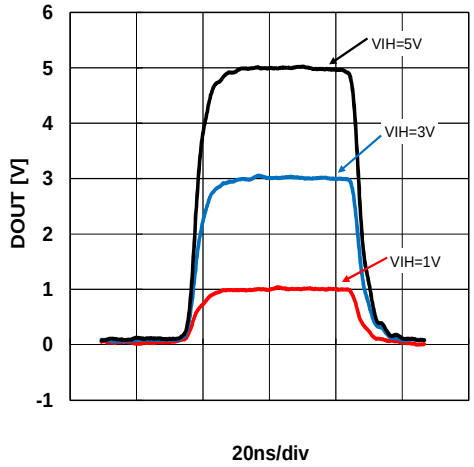
- Power-on state
  The switch control register immediately after power activation is set as LOW, and an analog switch will be in a OPEN (OFF) state.

■ TYPICAL CHARACTERISTICS

VDD=10V, VSS=−3V, VBB=1.5V, ENAx=ENBx=0V, VIHx=3V, VILx=0V, CVAx=1.5V, VOH=3V, VOL=0V, RL=1kΩ, CL=33pF, Ta=25℃ unless otherwise specified.

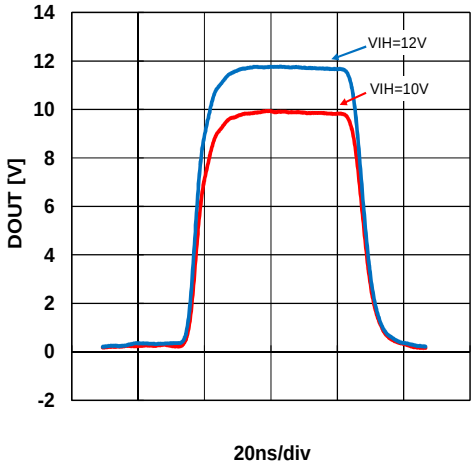
[Driver] Output Response

VIH=1, 3, 5V、VIL=0V



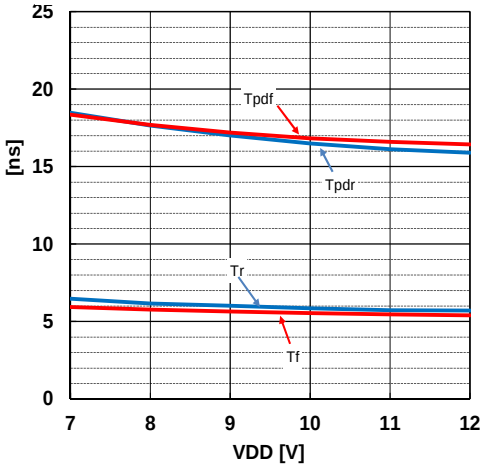
[Driver] Output Response

VIH=10, 12V、VIL=0V



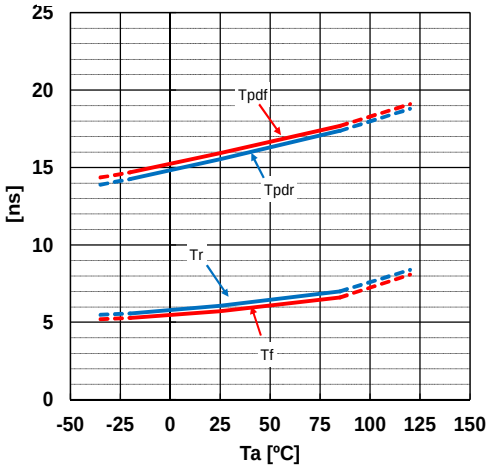
[Driver] Propagation Delay, Rise/Fall Time

vs Power Supply Voltage



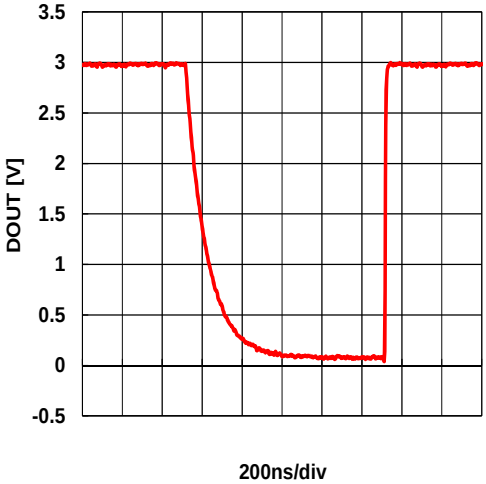
[Driver] Propagation Delay, Rise/Fall Time

vs Temperature



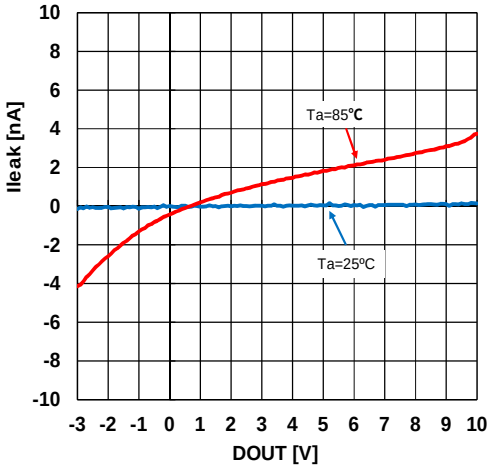
[Driver] Output Response

ENA=ENB=3V

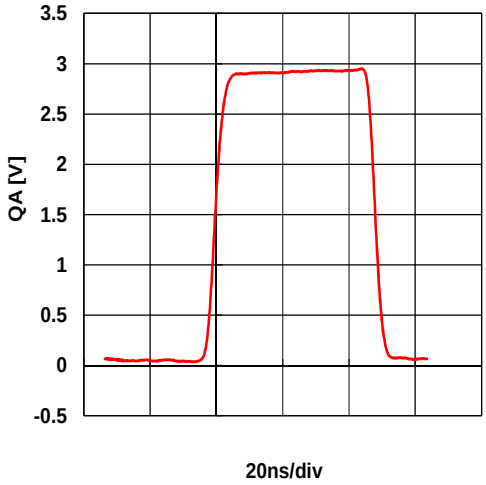


[Driver] DOUT Output Leakage Current

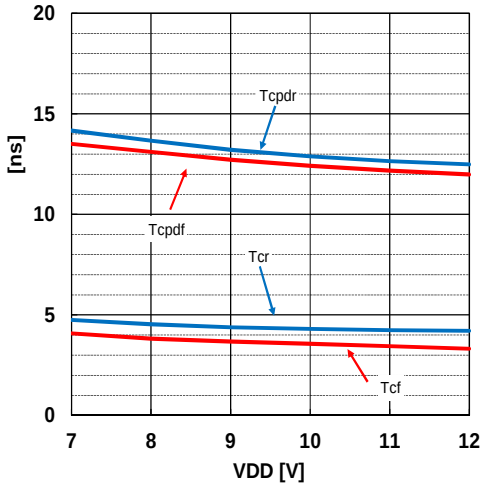
vs Output Voltage



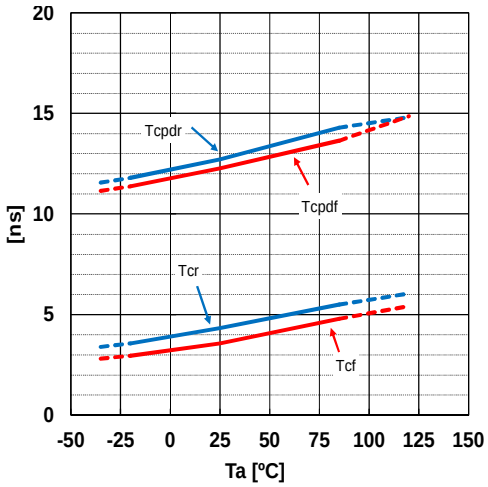
[Comparator] Output Response



[Comparator] Propagation Delay, Rise/Fall Time
vs Power Supply Voltage

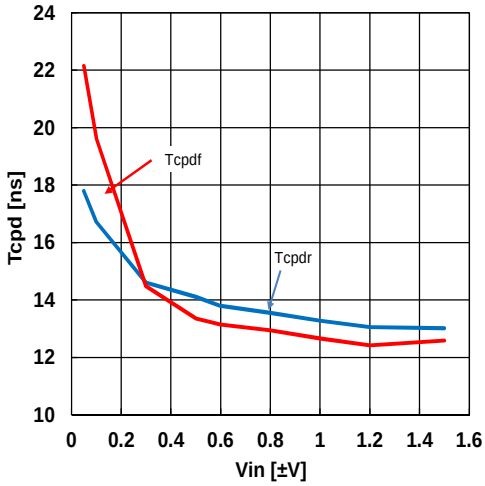


[Comparator] Propagation Delay, Rise/Fall Time
vs Temperature



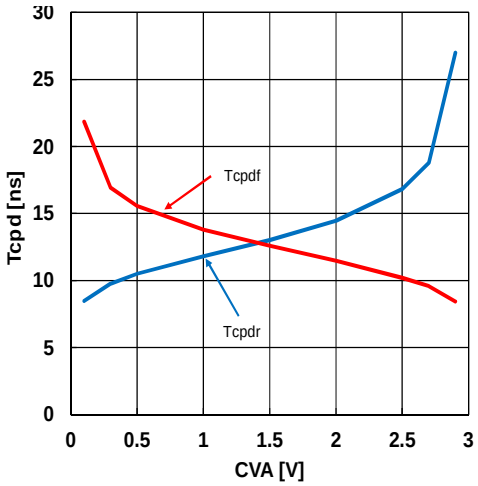
[Comparator] Propagation Delay Overdrive Voltage Variation

DOUT=1.5V±Vin

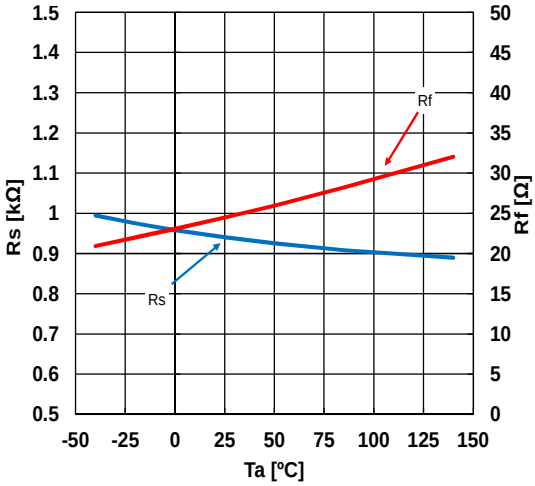


[Comparator] Propagation Delay Common Voltage Variation

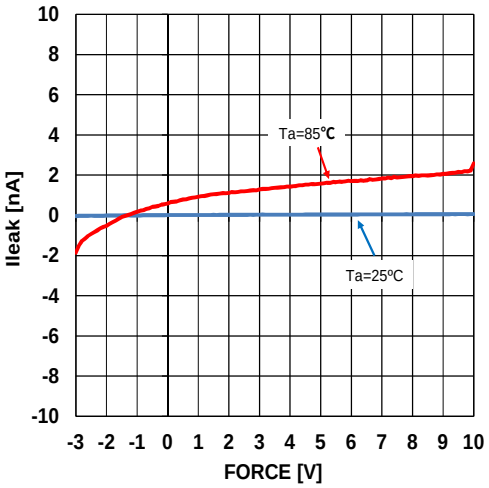
DOUT=1.5V±1.5V, VOH=3V, VOL=0V



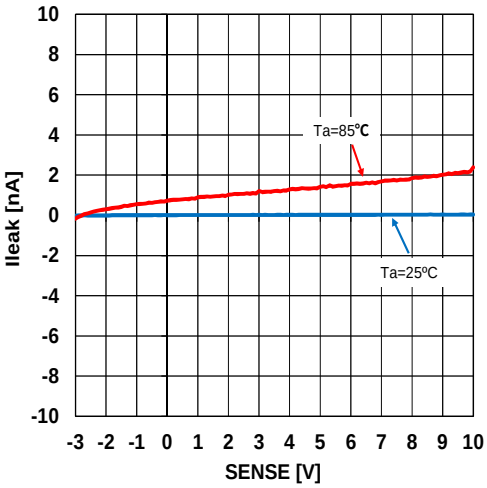
[SW] Switch Resistance vs Temperature



[SW] FORCE Leakage Current

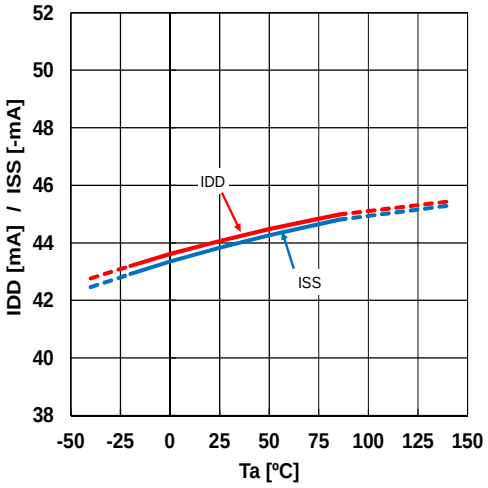


[SW] SENSE Leakage Current



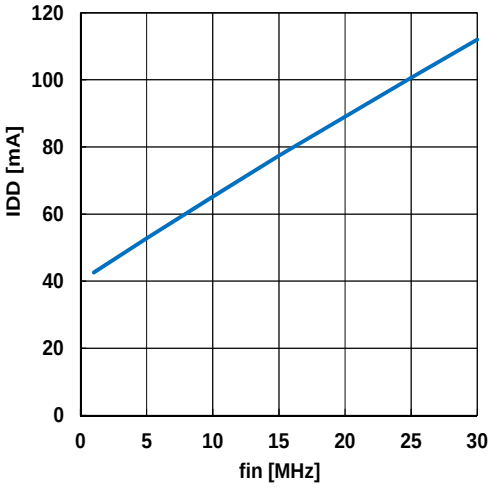
Supply Current vs Temperature

No Signal



Supply Current vs Operating Frequency

4ch Operation



■ NOTICE, CAUTIONS

1) Short pins in IC and connection to them on the board

VSS(0-8),VDD(0-8),VBB(0-1) and VOH(0-1),VOL(0-1) are shorted in the IC, respectively. But you should connect all of the pins to decrease the impedance of power supplies.

2) Power-on Sequence

You should power on with the following sequence: first VSS(0-8), second VDD(0-8), third VBB(0-1) and CVA(0-3), then power on the other inputs.

Otherwise sequence may cause a permanent damage to the IC.

3) Leak Current in HiZ Mode

The leak current might exceed 2nA in case of the following:

1. When DOUT(0-3) or VIH(0-3) or VIL(0-3) voltage set near VDD voltage
2. When the junction temperature is high.