Low phase noise Fundamental Quartz Crystal Oscillator IC

■GENERAL DESCRIPTION

The NJU6222 series is a C-MOS quartz crystal oscillator IC (20MHz to 50MHz) realized very low phase noise**.** It is consisted of an oscillation amplifer, divider (f_0, $f_0/2$), and 3-state output buffer.

There are 2-type of pad location for Flip chip and Wire bonding that apply SMD's 2016-package and more miniature. The NJU6222 in low voltage operation features low phase noise, it is suitable for high quality Hi-Fi sound device, Communication device, and others by battery drive.

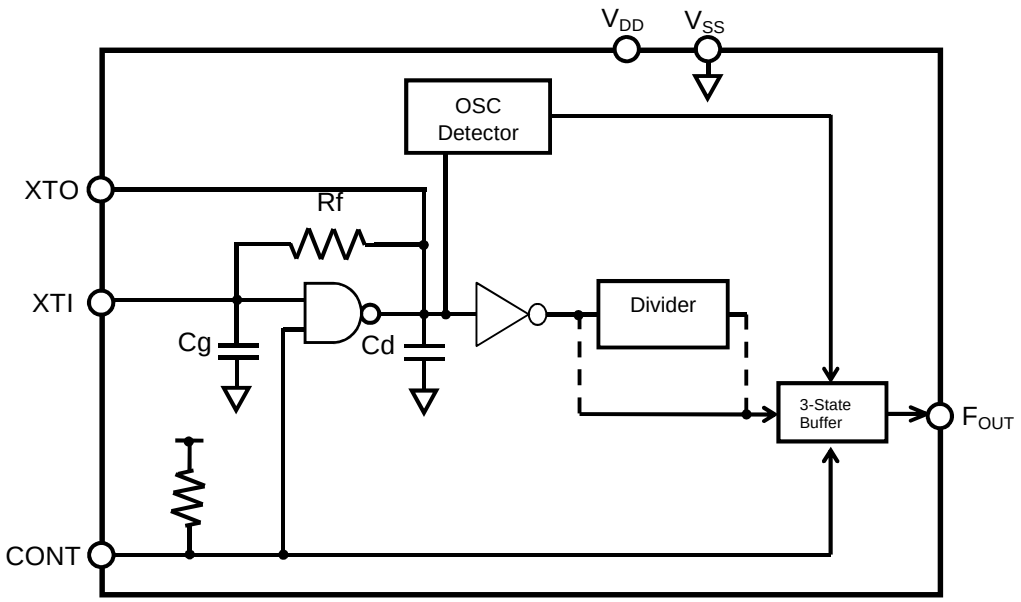
■PACKAGE OUTLINE

NJU6222XxC-V

■FEATURES

●Oscillation Frequency	20~50MHz(Fundamental)
●Frequency Stability	±1ppm@V_{DD}=1.8V±10%, V_{DD}=3.3V±10%
●Wide Operating Voltage	1.62 to 3.63V
●Very Low Phase Noise	-103dBc/Hz(Typ.) @49.152MHz,10Hz offset, V_{DD}=1.8V -158dBc/Hz (Typ.) @49.152MHz, 1kHz offset, V_{DD}=1.8V -103dBc/Hz(Typ.) @49.152MHz, 10Hz offset, V_{DD}=3.3V -163dBc/Hz(Typ.) @49.152MHz, 1kHz offset, V_{DD}=3.3V
●RMS Jitter	0.10psec(Typ.) 12kHz~20MHz, V_{DD}=1.8V 0.05psec(Typ.) 12kHz~20MHz, V_{DD}=3.3V
●Low Operating Current	3.1mA (Typ.) @49.152MHz, V_{DD}=1.8V, CL=15pF
●Built-in Divider	f_0, $f_0/2$ (Factory set)
●Stand-by Function (CONT terminal: L)	Oscillation Stop and High Impedance Output "F_{OUT}" terminal
●3-State Output Buffer	
●Built-in Variable Pull-up Resistance (CONT: Pull-up Resistance large at the Stand-by mode.)	
●Built-in Oscillation Capacitors Cg and Cg	
●C-MOS Technology	
●Package Outline	Die / 8-inch Wafer / 1/4 cut wafer

■BLOCK DIAGRAM

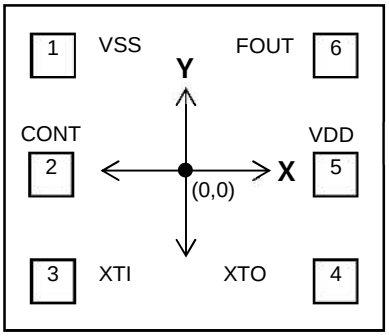


■LINE-UP TABLE

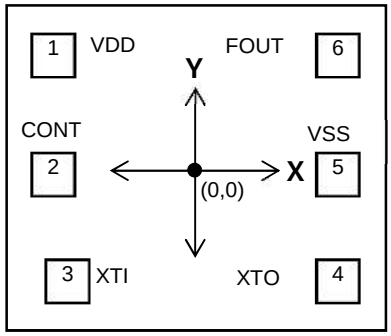
Type No.	F_{OUT}	Version	
		Type A	Type C
NJU6222	f_0	A1	C1
	$f_0/2$	A2	C2

■PAD LOCATION

Type A
(For Flip Chip Bonding)



Type C
(For Wire Bonding)



■COORDINATES

Pad No.	X	Y
1	-174	190
2	-186	0
3	-174	-190
4	174	-190
5	186	0
6	174	190

■PART NUMBER

NJU6222 □□ □-□

W-V: Wafer (130µm)
C-V: Die (130µm)

Version

Device name

Starting Point: Die Center Unit[µm]
Die Size: 0.580x0.588mm
Die Thickness (C-V): 130±15µm
Wafer Thickness (W-V): 130±20µm
Pad size: 80x80µm
Die Substrate: V_{SS} level

■VIRSION DISCRIMINATION INTERNAL COMPONENTS

PAD layout version of the NJU6222 series is determined by the version name in chip. Divide version of the NJU6222 series is determined by the internal fuse trimming.

Laser-trimmed versions are identified externally by the combination of the version name marking (1) and the locations of trimmed fuses (2). (Table 1 shows the chip version identification)

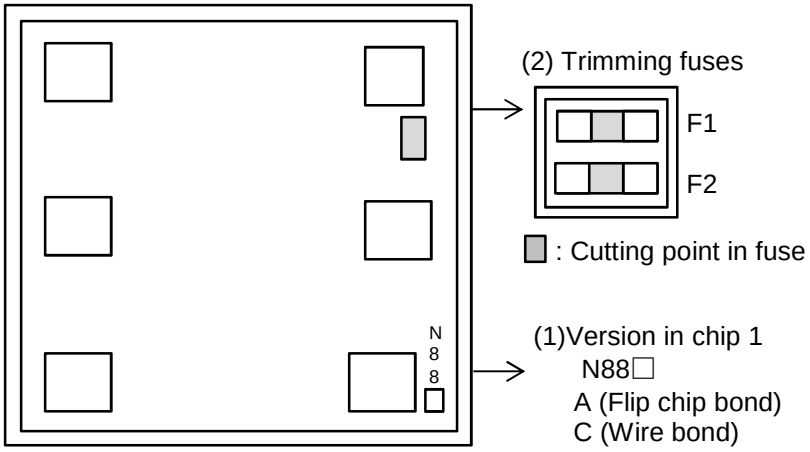


Table 1: Frequency version and Cutting point in fuse.

Version name	Mask / Version set by trimming fuses		
	Mask	Trimming fuses	
	Version	F1	F2
NJU6222A1	A	-	-
NJU6222A2	A	*	-
NJU6222C1	C	-	-
NJU6222C2	C	*	-

Note 1) "-": Uncut, "*": Cutting

■TERMINAL DESCRIPTION

SYMBOL	FUNCTION
CONT	Oscillation and 3-state Output Buffer Control CONT: H or OPEN → F_{OUT}: Output one frequency selected out of f0 and f0/2 Note1) CONT: L → F_{OUT}: Oscillation Stop and High impedance Output
XTI	Quartz Crystal Connection terminals
XTO	
V_{SS}	GND terminal (V_{SS}=0V)
F_{OUT}	Frequency Output terminal (3-State Output Buffer)
V_{DD}	Power Supply terminal V_{DD}=1.62 to 3.63V

Note1) Refer to the line-up table.

■FUNCTIONAL DESCRIPTION

●Standby Function

When CONT Terminal is “Low”, the F_{OUT} Terminal output is High impedance.

CONT	F_{OUT}	Oscillator
High(Open)	Frequency output	Normal operation
Low	High impedance	Stop

When not using Stand-by function, CONT terminal is recommended to connect to V_{DD}.

●Built-in Variable Pull-up Resistance of CONT terminal

The built-in pull-up resistance value of CONT Terminal changes in response to the input level. When CONT is “LOW” level, the pull-up resistance value is large to reduce the current consumption by the resistance. When CONT is open or connected to V_{DD}, the pull-up resistance value is small to decrease the input susceptibility to external noise. It works to prevent an unexpectedly stopping of the output by external noise.

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.6 to +6.0	V
Input Voltage	V_{IN}	-0.6 to +V_{DD}+0.6 and ≦6.0V	V
Output Voltage	V_O	-0.6 to V_{DD}+0.6	V
Input Current	I_{IN}	±10	mA
Output Current	I_O	±25	mA
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Note2) If the LSI used condition above the absolute maximum ratings, the LSI may be destroyed.
Use beyond the electric characteristics conditions will cause mal-function and poor reliability.

■ELECTRICAL CHARACTERISTICS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}	fosc=50MHz	1.62	-	3.63	V
Input Voltage	V_{IN}	CONT	0	-	3.63	V
Output Voltage	V_{OUT}	F_{OUT}	0	-	V_{DD}	V
Output Frequency Stability	df/f	V_{DD}±10%	-	±1	-	ppm

(V_{DD}=1.62 to 3.63V, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	x1 version (f_0) No load MEASURMENT CIRCUIT(1) f_0=49.152MHz Fout=49.152MHz	V_{DD}=1.8V	-	1.8	2.9	mA
			V_{DD}=2.5V	-	3.3	4.8	
			V_{DD}=3.3V	-	5.5	7.7	
		x2 version (f_0/2) No load MEASURMENT CIRCUIT(1) f_0=49.152MHz Fout=24.576MHz	V_{DD}=1.8V	-	1.4	2.4	
			V_{DD}=2.5V	-	2.7	4.1	
			V_{DD}=3.3V	-	4.8	6.6	
		x1 version (f_0) CL=15pF MEASURMENT CIRCUIT(1) f_0=49.152MHz Fout=49.152MHz	V_{DD}=1.8V	-	3.1	4.1	
			V_{DD}=2.5V	-	5.1	6.6	
			V_{DD}=3.3V	-	7.9	9.9	
		x2 version (f_0/2) CL=15pF MEASURMENT CIRCUIT(1) f_0=49.152MHz Fout=24.576MHz	V_{DD}=1.8V	-	2.0	3.0	
			V_{DD}=2.5V	-	3.6	4.9	
			V_{DD}=3.3V	-	5.9	7.7	
Stand-by Current	I_{STB}	MESURMENT CIRCUIT(1) CONT=V_{SS}	V_{DD}=1.8V	-	3.0	25.0	µA
			V_{DD}=2.5V	-	5.0	30.0	
			V_{DD}=3.3V	-	9.0	35.0	
Output Voltage	V_{OH}	MEASURMENT CIRCUIT(2)		V_{DD}-0.4	-		V
	V_{OL}			-	-	0.4	V
Input Voltage	V_{IH}	MEASURMENT CIRCUIT(3)		0.7V_{DD}	-	-	V
	V_{IL}					0.3V_{DD}	V
Input Current	I_{IN}	MEASURMENT CIRCUIT(4) V_{DD}=1.62V, CONT=V_{DD}		-	-	0.065	µA
		MEASURMENT CIRCUIT(4) V_{DD}=1.62V, CONT=V_{SS}		-	-	-0.5	
		MEASURMENT CIRCUIT(4) VDD=3.63V, CONT=V_{SS}		-	-	0.150	
		MEASURMENT CIRCUIT(4) VDD=3.63V, CONT=V_{SS}		-10	-	-	
3-state Off Leakage Current	I_{OZ}	MEASURMENT CIRCUIT(5) CONT=V_{SS}, F_{OUT}= V_{DD} or V_{SS}		-	-	±0.1	µA

(V_{DD}=1.62 to 3.63V, V_{SS}=0V, Ta=25°C)

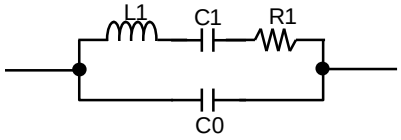
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Feedback Resistance	Rf			-	50	-	kΩ
Built-in Oscillation Capacitor	Cg	fosc=50MHz		-	8	-	pF
	Cd	fosc=50MHz		-	17	-	pF
Oscillation Frequency	fosc	Recommendation		-	-	50	MHz
Output Signal Symmetry	SYM	MEASURMENT CIRCUIT(1),@V_{DD}/2		45	50	55	%
Phase Noise	SSB	x1 Version (f_0) f_{OSC}=49.152MHz. V_{DD}=1.8V Fout=49.152MHz	10Hz offset	-	-103	-	dBc/ Hz
			1kHz offset	-	-158	-	
			Floor	-	-166	-	
		x1 Version (f_0) f_{OSC}=49.152MHz. V_{DD}=3.3V Fout=49.152MHz	10Hz offset	-	-103	-	
			1kHz offset	-	-163	-	
			Floor	-	-172	-	
Output Signal Rise Time	Tr	C_L=15pF 0.1V_{DD} to 0.9V_{DD}	V_{DD}=1.8V	-	3.1	4.7	ns
			V_{DD}=2.5V	-	1.8	2.7	ns
			V_{DD}=3.3V	-	1.3	2.0	ns
Output Signal Fall Time	Tf	C_L=15pF 0.9V_{DD} to 0.1V_{DD}	V_{DD}=1.8V	-	2.8	4.2	ns
			V_{DD}=2.5V	-	1.8	2.7	ns
			V_{DD}=3.3V	-	1.4	2.1	ns
Output Disable time	t_{POZ}	MEASURMENT CIRCUIT(6)		-	-	200	ns
Output Enable time	t_{PZO}	MEASURMENT CIRCUIT(6)		-	-	1.0	ms
Oscillation Start time	t_{OSC}	MEASURMENT CIRCUIT(1)		-	-	1.0	ms

Note3) Decoupling capacitor (≥0.01μF) should be connected between V_{DD} and V_{SS} due to the stabilized operation the circuit.

Note4) Phase noise: Apply to NJU6222A1/C1 (f_0) version.

Note5) The oscillation frequency range has used NJRC's standard crystal for measurement. However it is not guaranteed. (Refer to EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS)

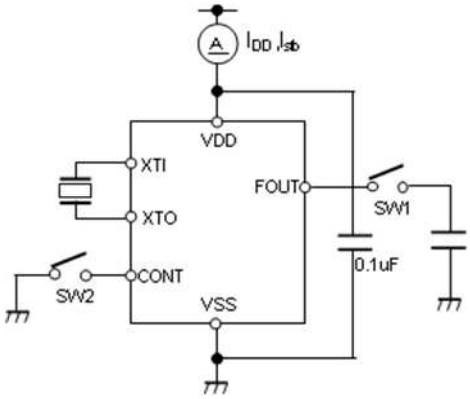
■EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS



f[MHz]	R1[Ω]	L1[mH]	C1[fF]	C0[pF]
49.152	17.7	3.83	2.74	1.23

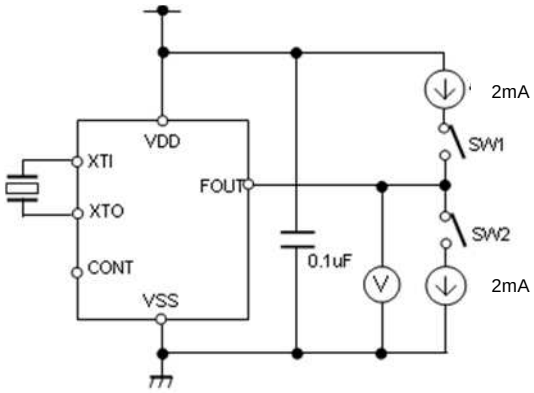
■MEASUREMENT CIRCUITS

(1) Operating Current, Stand-by Current, Output Signal Symmetry, Output Signal Rise/Fall Time (C_L=0pF, 15pF)



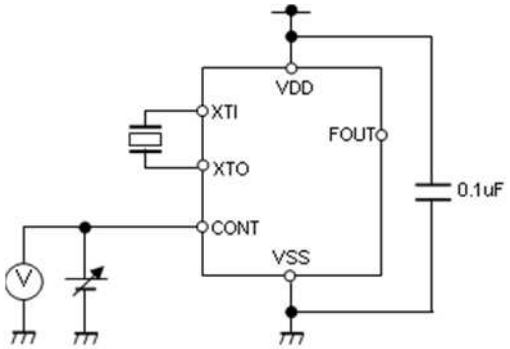
ITEM	SW1	SW2
I_{DD}(CL=0pF)	OFF	OFF
I_{DD}(CL=15pF)	ON	OFF
Istb	ON or OFF	ON
SYM, tr, tf	ON	OFF
t_{OSC}	ON	OFF

(2) H Level, L Level Output Voltage



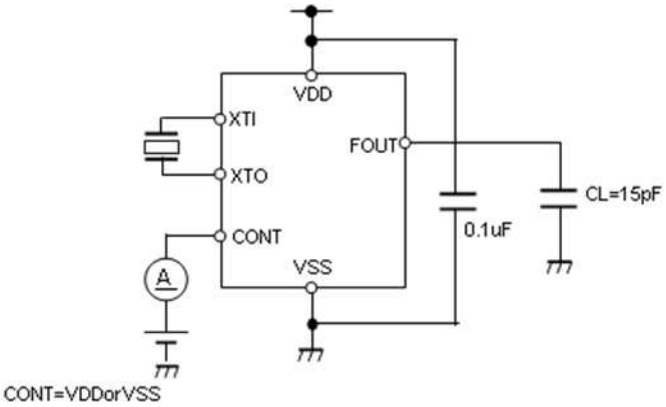
ITEM	SW1	SW2
V_{OH}	OFF	ON
V_{OL}	ON	OFF

(3) H Level, L Level Input Voltage

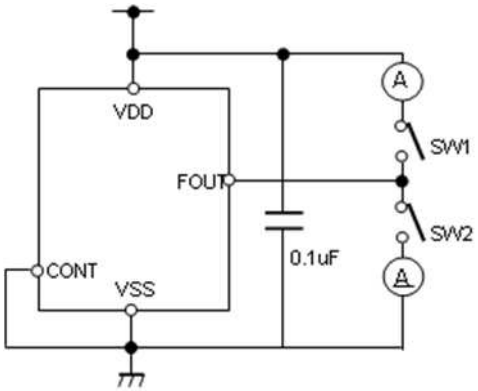


ITEM	F_{OUT}
CONT≥0.7V_{DD}	Oscillation
CONT≤0.3V_{DD}	Stop

(4) Input Current (C_L=15pF)

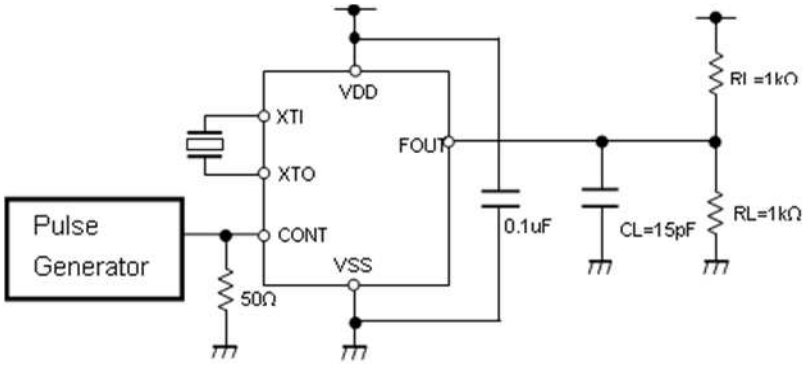


(5) 3-state Leakage Current



ITEM	SW1	SW2
I_{OZH}	ON	OFF
I_{OZL}	OFF	ON

(6) Output Disable Time (CL=15pF, RL=1kΩ)



■TIMING CHART

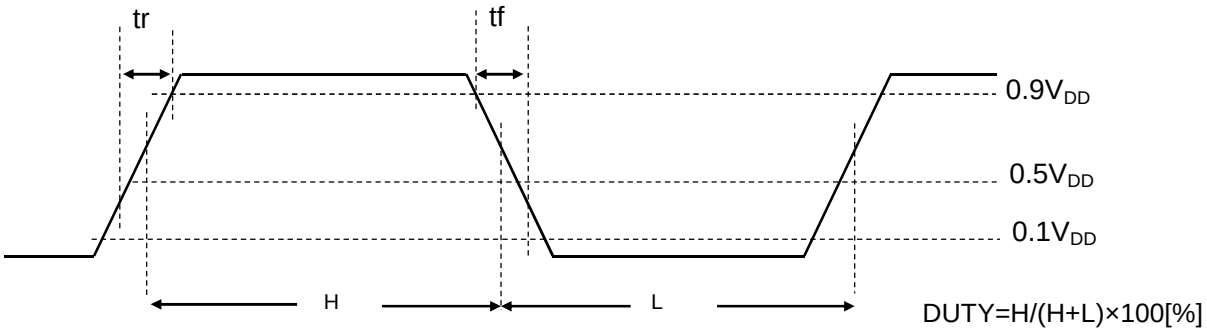


Fig.1 Output Signal Rise Time, Output Signal Fall Time, Output Symmetry

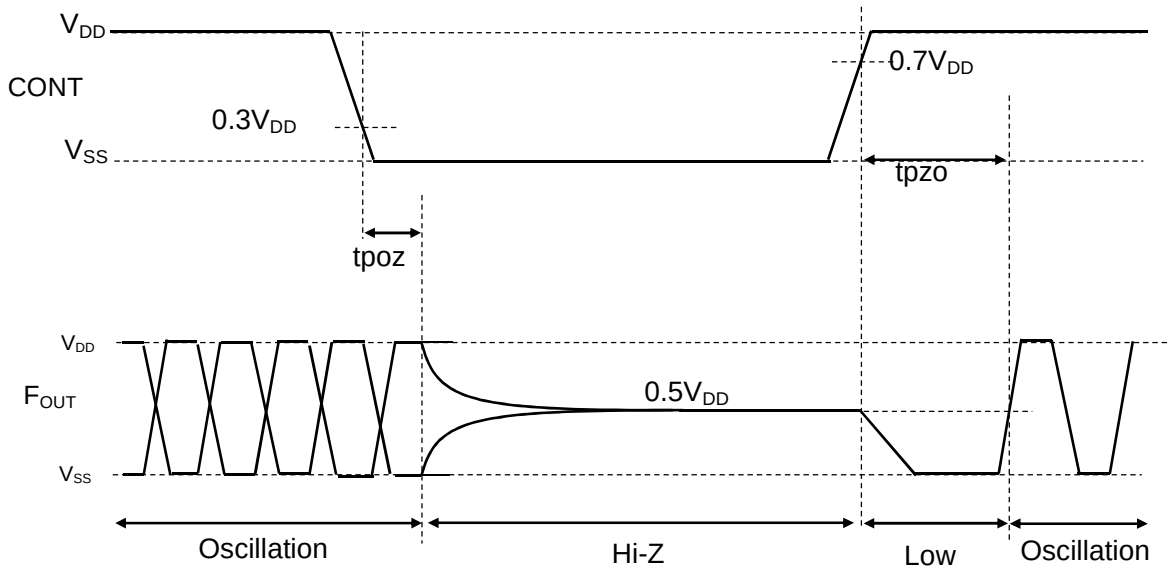


Fig.2 Output Disable time: tpoz, Output Enable time: tpzo, Timing Chart

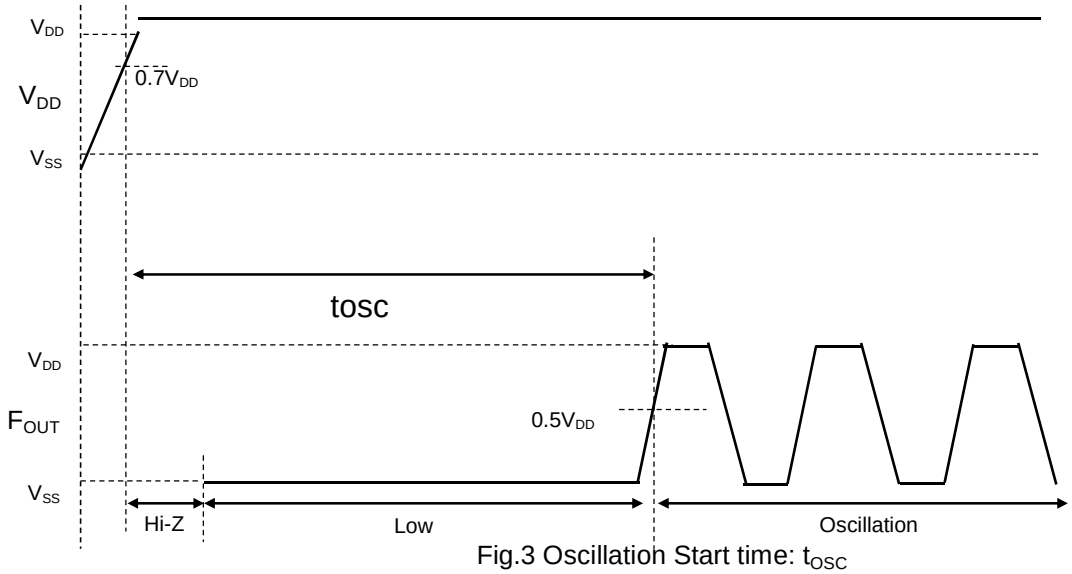
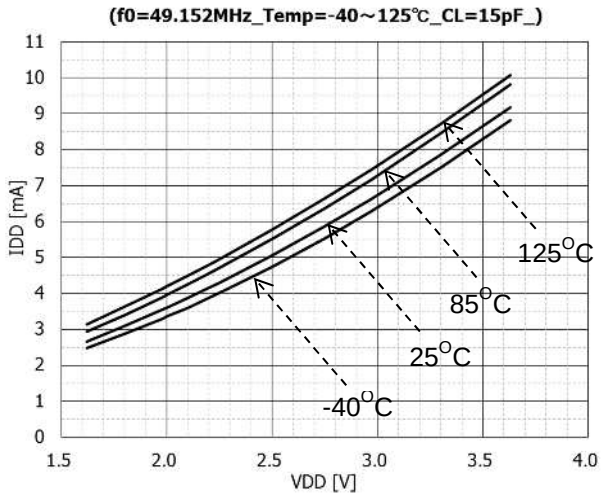


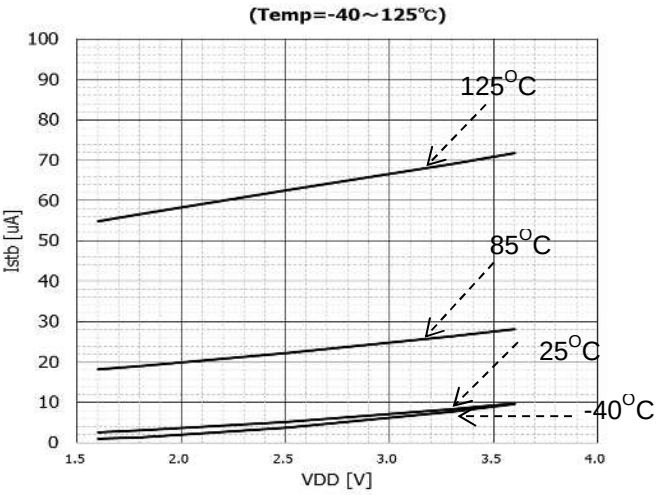
Fig.3 Oscillation Start time: t_{OSC}

■TYPICAL CHARACTERISTICS

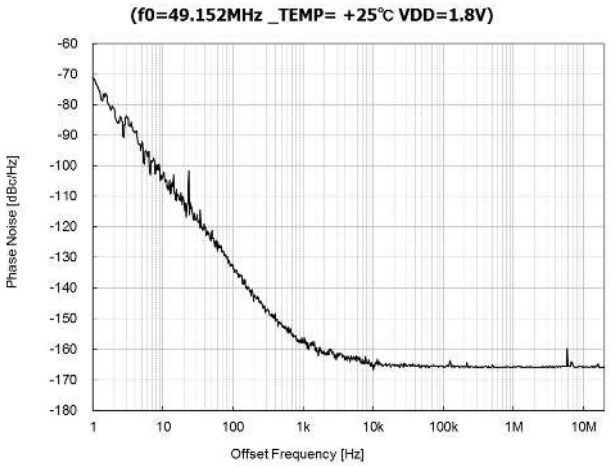
I_{DD}(CL=15pF)

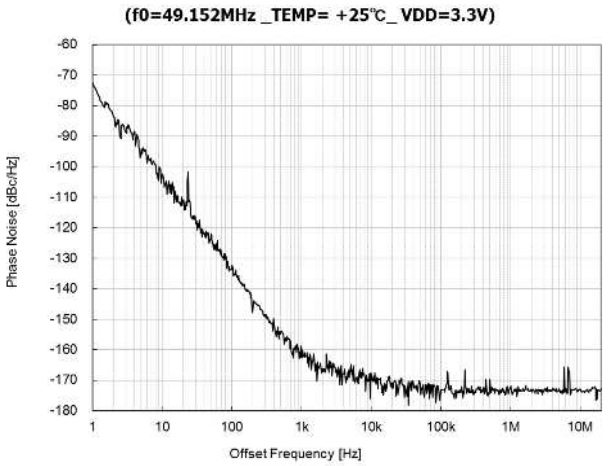


Istb

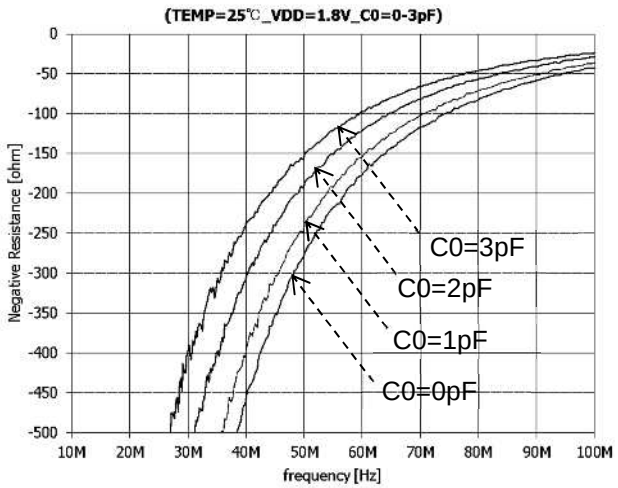


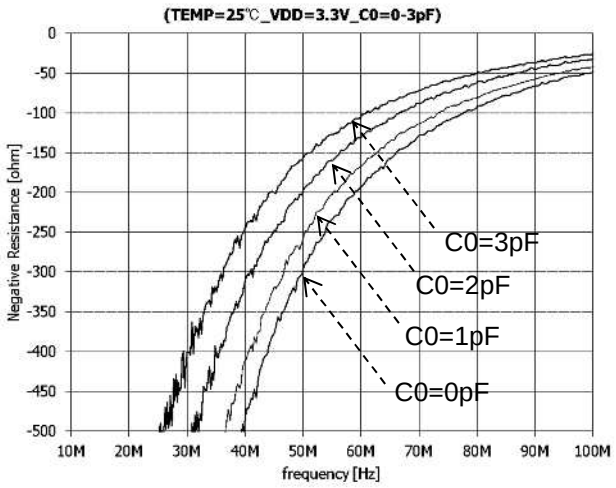
Phase Noise

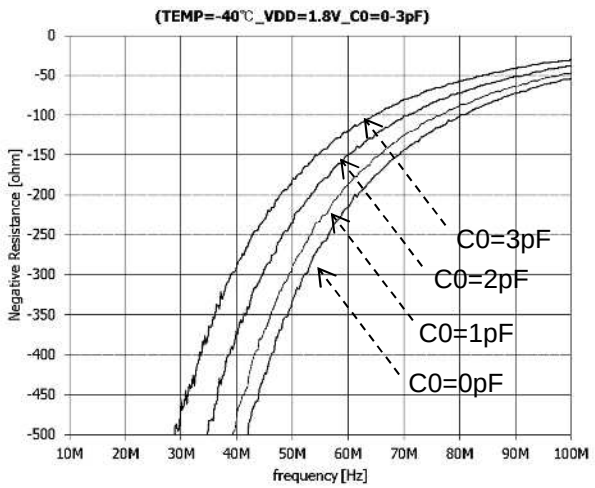


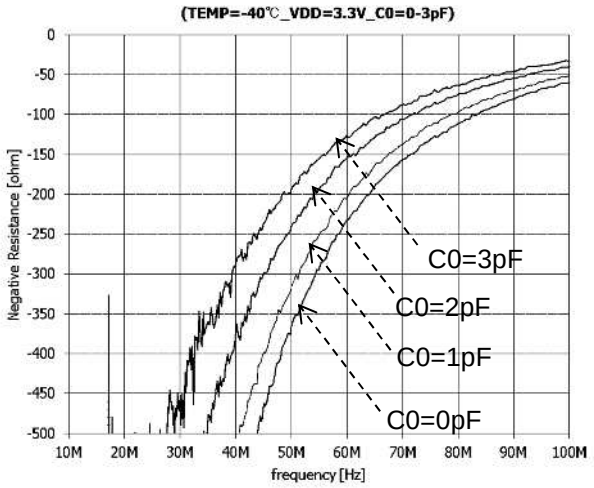


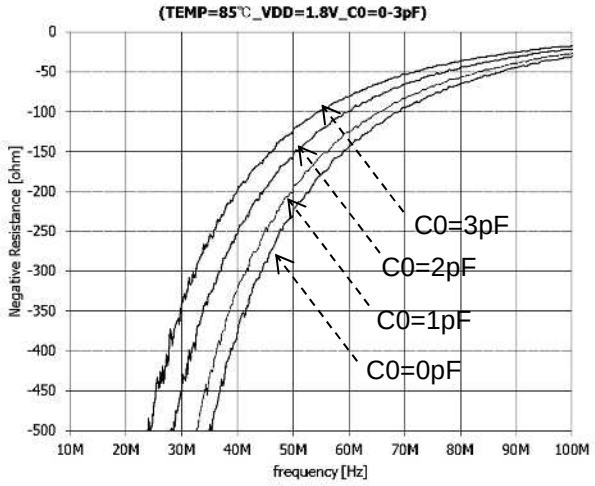
Negative Resistance

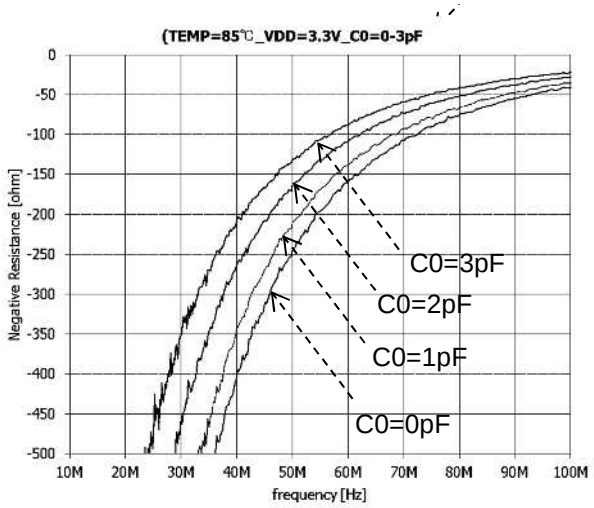


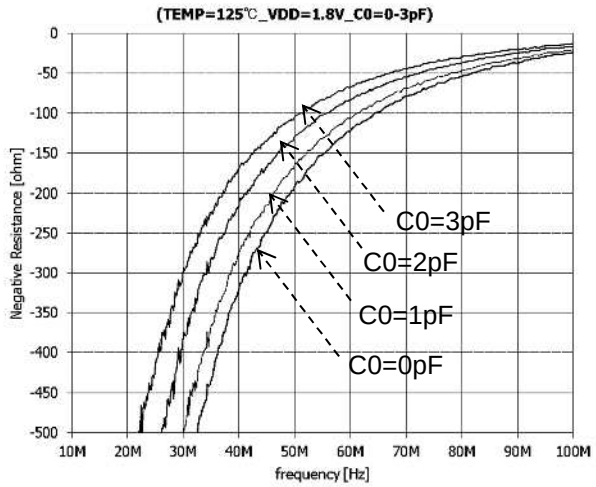


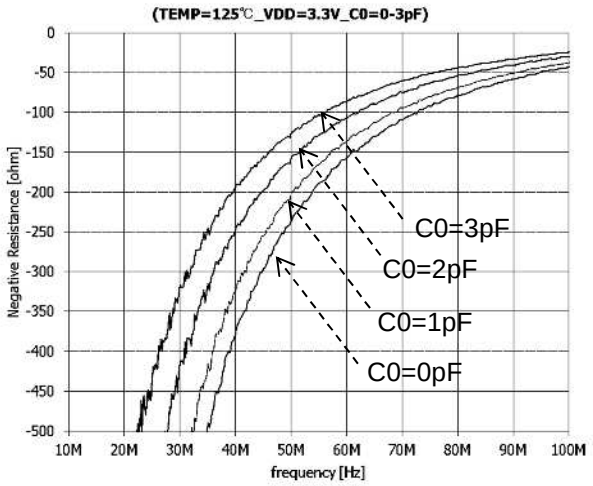






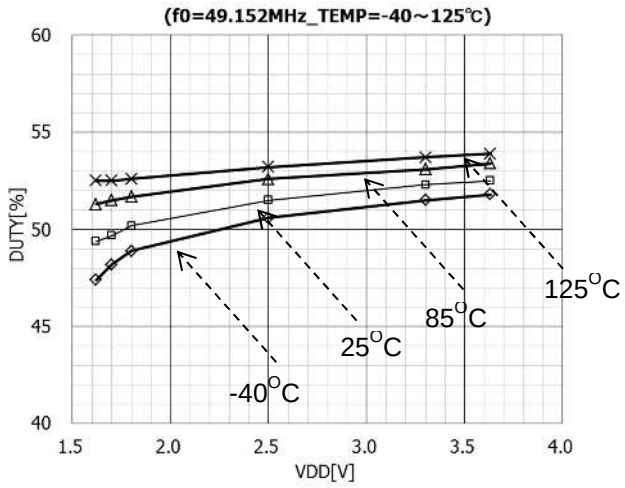




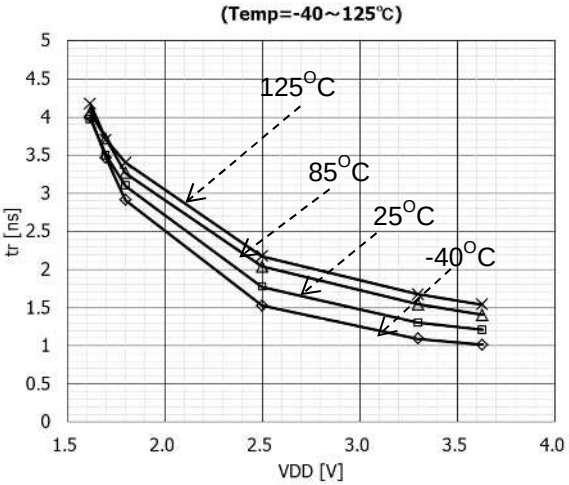


Note; A negative resistance 3 to 5 times the equivalent series resistance is said to be required for sufficient oscillation margin.

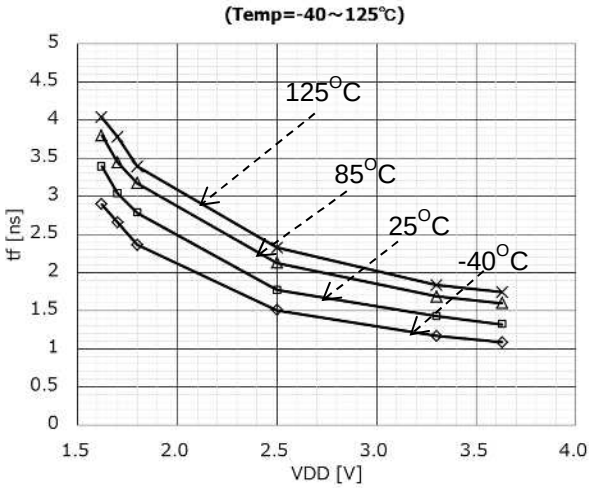
・SYM



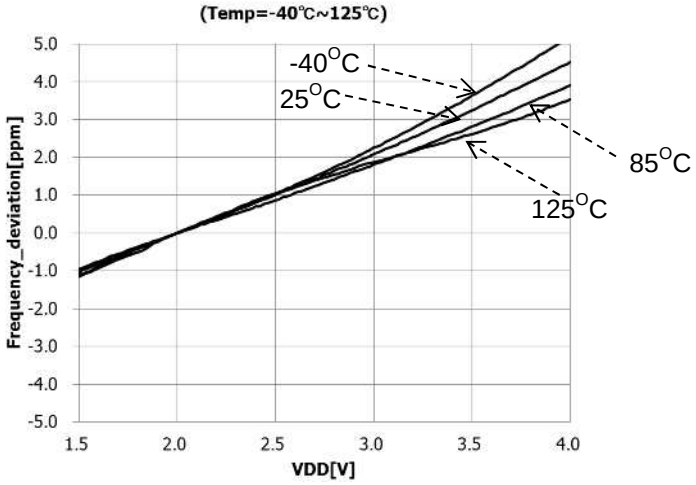
・ tr



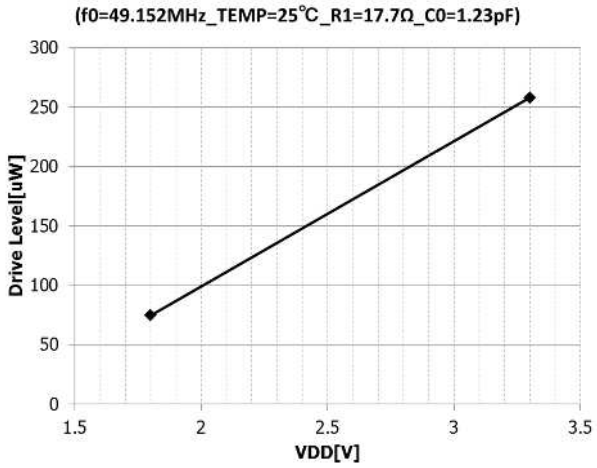
・ tf



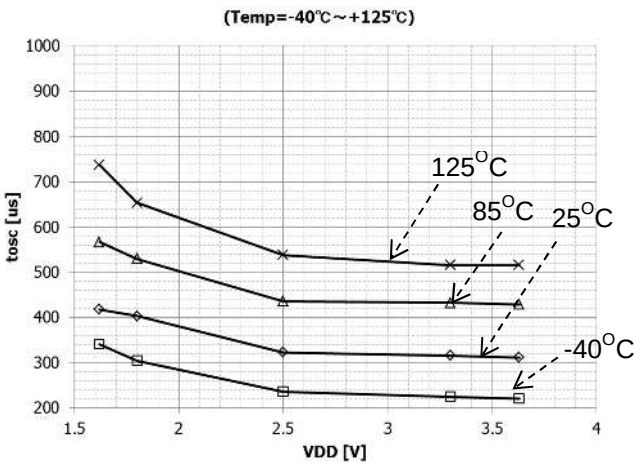
・ df/f



・ Drive Level



・ t_{OSC}



・Waveform

Fosc=49.152MHz、V_{DD}=1.8V、CL=15pF、Temp=25℃

Fosc=49.152MHz、V_{DD}=3.3V、CL=15pF、Temp=25℃