24 keys input key-scan IC

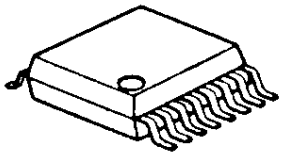
■ GENERAL DESCRIPTION

The NJU6010 is 24 keys input key-scan IC with internal oscillation.

It scans the maximum 4x6 key matrix. And the key data transmit to CPU.

The microprocessor interface circuits that operate 2MHz(Max.) frequency, can be connected directly to serial microprocessor.

■ PACKAGE OUTLINE

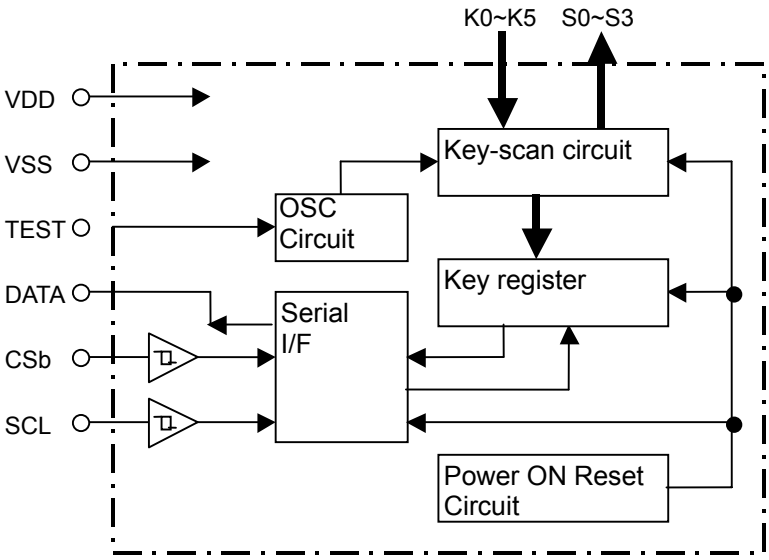


NJU6010

■ FEATURES

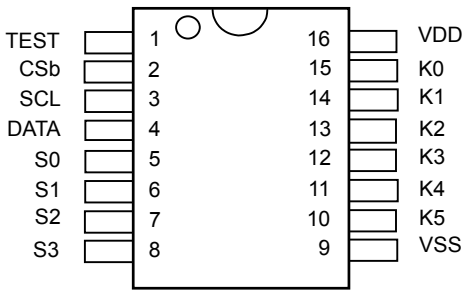
- Key-scan Function (Maximum matrix 4 x 6 = 24-key)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip
- Power On Reset Function
- Operating Voltage 2.4 to 5.5V
- C-MOS Technology P-Sub
- Package Outline SSOP16

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

- SSOP16



■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION
1	TEST	Oscillation Circuit Test Terminal. Keep open
2	CSb	Data output is available by "L".
3	SCL	Serial Clock Input Terminal
4	DATA	Serial Data Output Terminal (This terminal outputs both the serial data and REQ signals.) CSb="H" : Request signal output, CSb="L" : Key data output
5 ~ 8	S0 ~ S3	Key Scanning Output Terminals
9	VSS	GND Terminal
10 ~ 15	K0 ~ K5	Key Scanning Input Terminals
16	VDD	Power Source Terminal

■ FUNCTIONAL DESCRIPTION

(1) Description for Each Blocks

- Serial I/F
  The Serial I/F operates control of output signal.

- Power ON Reset Circuit
  The Power ON Reset Circuit initializes the key register automatically at Power ON.

- Key-scan Circuit
  When the key pressed, the Key-scan Circuit output the request signal from DATA terminal. The key data is kept in the key register until CPU starts reading key data.

- Key Register
  The Key Register keeps the read key data.

- Oscillation Circuit
  The oscillation circuit is built-in.

(2) Key-scan Circuit

The Key-scan Circuit consists of a detector block of key pressing (S0~S3) and a fetching block of key status (K0~K5). The Key-scan Circuit connects the 4x6 key-matrix and reads the data of 24 keys maximum as shown in Fig1. Furthermore, it operates correctly against the multiple key inputs. (Conditional)

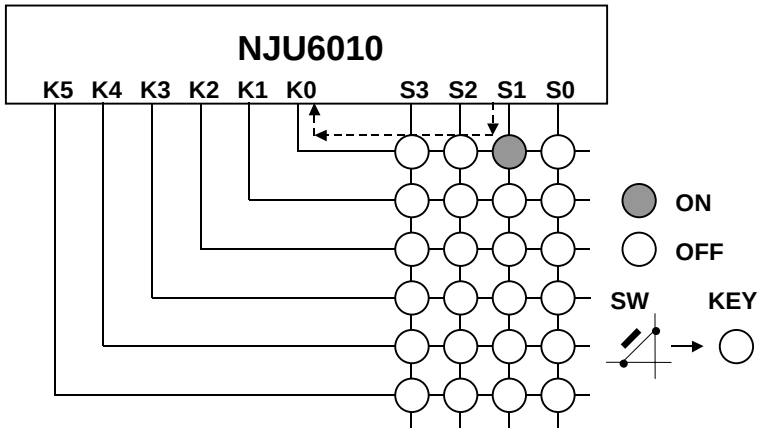


Fig. 1 Key-scan Matrix

(2-1) Timing of Key-scan

The key-scan cycle is 512 x T[s] (T=1/fosc). The key data is detected by executing key-scan operation of 2 times. This operation prevents the miss-recognition. (Refer to Fig. 2)

The key-scan operation is available by status of CSb="H". The key-scan operation is not executed at status of CSb="L".

If the key data of 2-time is same, the NJU6010 recognizes that the key was pressed. Then, the DATA terminal outputs "H" as request (REQ signal) to CPU after 1408 x T[s] maximum from key input. When the DATA terminal outputs "H", the key data is kept in the internal register until CPU starts reading key data.

The key-scan is not executed until reading the key data finishes.

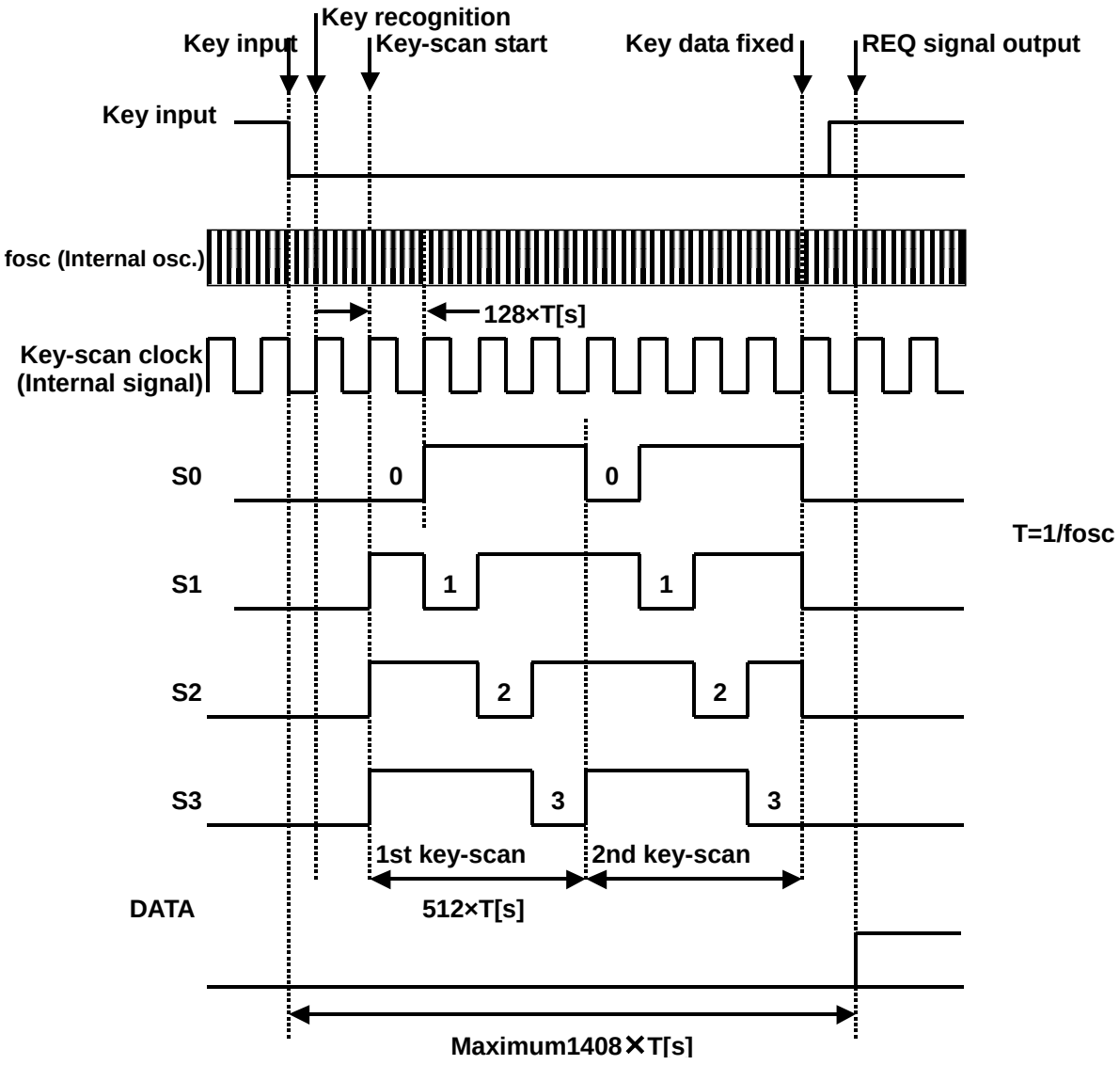


Fig. 2 Key-scan Timing

(2-2) Method of Checking the key

The method of checking the key judges the key pressed by fetching the key scanning output signal (S0~S3) with terminal K0~K5 (Refer to Fig. 2). S0~S3 are fixed at "L" level usually. K0~K5 are input terminals in the state of the pull-up.

When the key between S1 and K0 is pressed as an example, the K0 is changed from "H" to "L" (Refer to Fig. 3). NJU6010 detects the pressed key by the change in this K0 signal. And which key was pressed is checked, the key-scan signal is output from S0~S3 (Refer to Fig. 4).

The scan signal of S1 is input to the terminal K0 by this scan operation (Dot-line in Fig. 3). As a result, NJU6010 is checked as the key was pressed between S1 and K0.

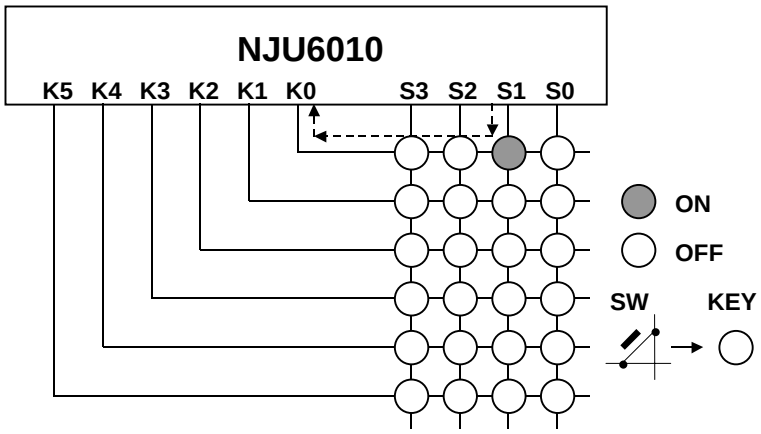


Fig. 3 Key-scan Checking (Example 1)

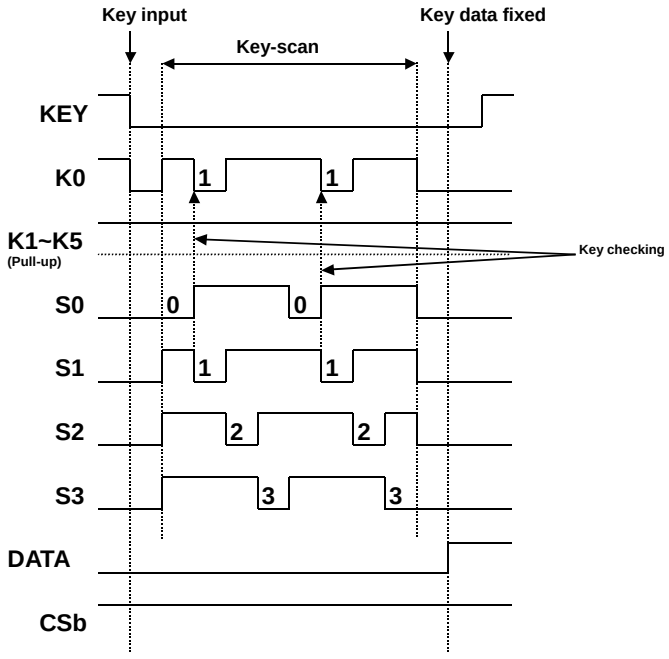


Fig. 4 Key-scan Checking (Example 2)

(2-3) Example of Key-scan Data Output

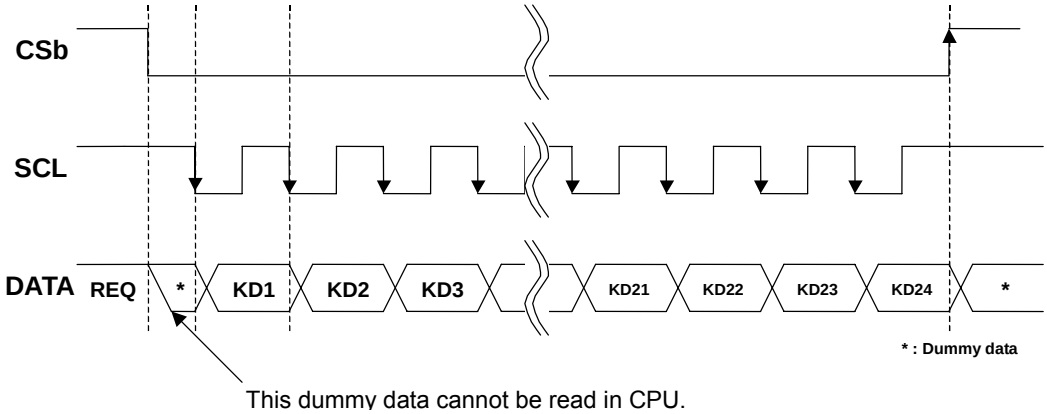
When CSb="L", the key data is output in order of "dummy → KD1~KD24 → dummy" from DATA terminal by the falling edge of SCL (Refer to Fig. 5). Therefore, the key data reading with CPU is fetched by the rising edge of SCL. When the CSb is falling edge, NJU6010 reads the key data regardless of the state of SCL ("H" or "L") (Refer to Fig. 5 (1) (2)). In case of (1), the 1st dummy data is not read with CPU. In case of (2), it is necessary to read the 1st dummy data. Therefore, the setting to read the dummy data with CPU is necessary.

The key data is output as 24-bit of KD1~KD24. The bit corresponding to the pressed key is output as "H", and the other bits are output as "L". (Refer to (2-4) The Relation Between Key Matrix and Key Data.)

When the CSb="H", NJU6010 outputs the key data reading request as becoming the DATA="H" (REQ flag). After this REQ flag is checked, the key data requires reading. In case of reading the key data in the state of the CSb="H" and DATA="L", the unexpected data is output.

After finished reading of the key data in CPU, read-out of key data is released by CSb="H", and NJU6010 waits for the next key input. When the CSb="H" before reading 24 bits of all the key data, the key data in a register is lost, a REQ flag is also released, and NJU6010 waits for the next key input.

(1) In case of SCL="H"



(2) In case of SCL="L"

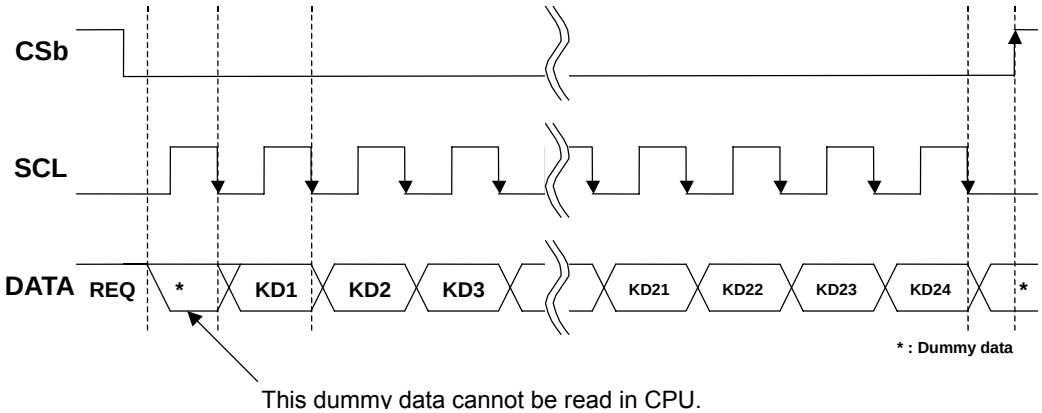
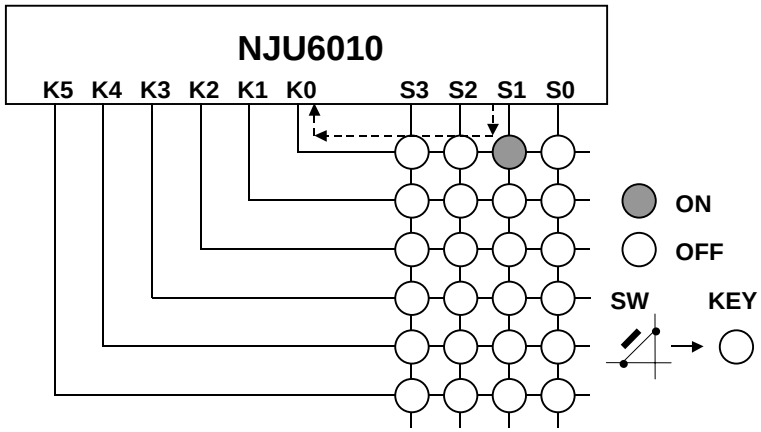


Fig. 5 Key Data Transfer Timing

(2-4) The Relation Between Key Matrix and Key Data

The relation between key matrix and key data is shown in Fig. 6.



	K0	K1	K2	K3	K4	K5
S0	KD1	KD2	KD3	KD4	KD5	KD6
S1	KD7	KD8	KD9	KD10	KD11	KD12
S2	KD13	KD14	KD15	KD16	KD17	KD18
S3	KD19	KD20	KD21	KD22	KD23	KD24

Fig. 6 Relation Between Key Matrix and Key Data

(2-5) The Relation Between Key Matrix and Key Data

No-pressed key data may change pressed key data in triple or more key input as shown in Fig. 7, and incorrect key data may be output to external CPU. For prevention of miss-recognition by incorrect key data, diodes should be inserted in front of keys as shown in Fig. 8 or control program of CPU should ignore the combination of key data miss-recognition.

In case of the key input as shown in Fig. 9, the recognition of multiple key inputs is realized without a diode.

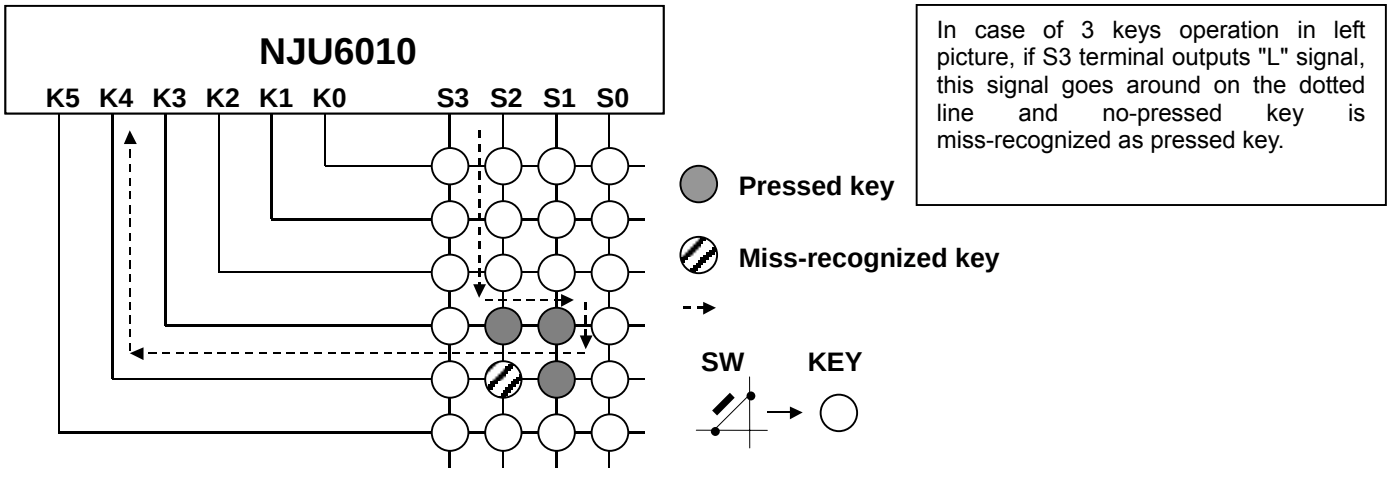
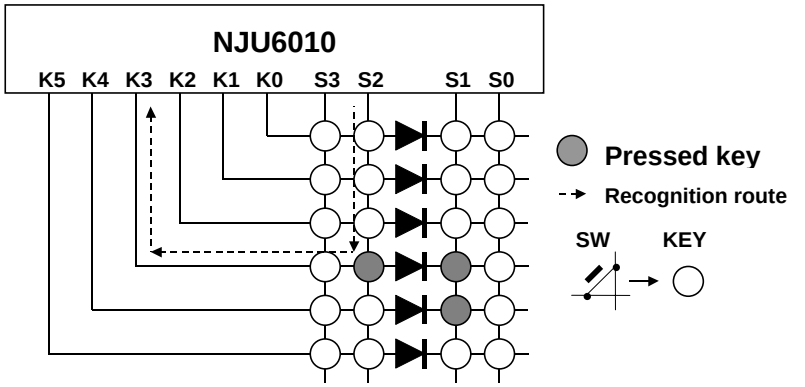


Fig. 7 Multiple Key Inputs



In order to prevent miss-recognition of Fig. 7, a diode is inserted as shown in the left picture.
As a result, the miss-recognition route of Fig. 7 is improved and the exact key recognition is realized.

Fig. 8 Example of Connection for Miss-recognition Prevention Diodes at Fig. 7

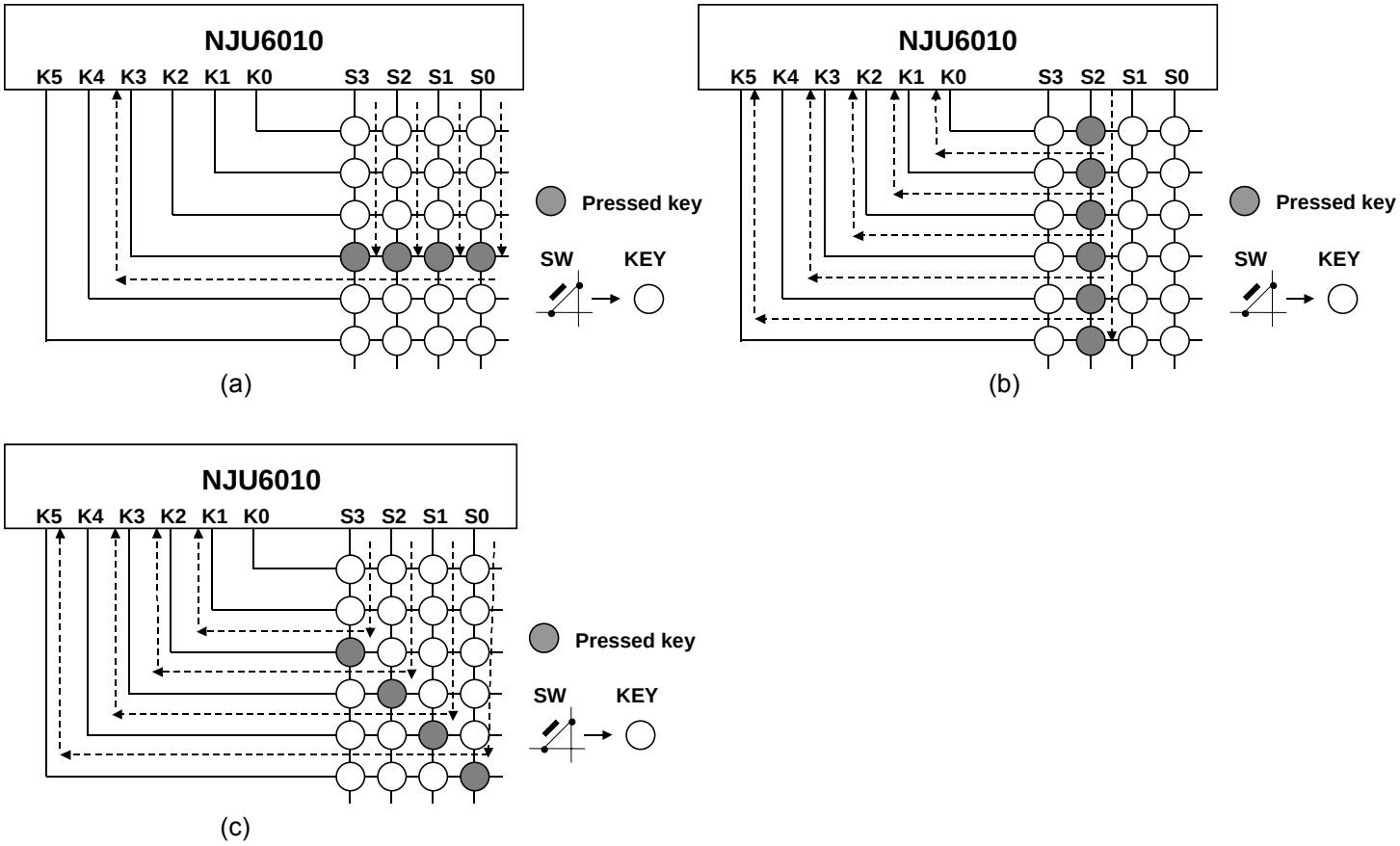


Fig. 9 Recognized multiple key inputs pattern

(2-6) Example of Key-scan Operating

Example of key-scan operating is shown in Fig. 10.

(1) Normal key-scan

The key input is detected and the key-scan starts. After checking the key data, the DATA becomes "H" (REQ flag).

After a REQ flag becomes effective even if the key is input, the key-scan is not executed.

The key data is read by CSb="L", and the read-out of key data is released by CSb="H".

(2) The key-scan after the key data reading is released (CSb="H")

When the key input continues after reading the key data finishes, NJU6010 executes the key-scan again.

(3) The key-scan as CSb="L"

When the CSb="L", the key-scan is not working even if there is no REQ flag.

The key-scan is effective at the CSb="H" and state of no REQ flag.

(4) Unexpected data

When the key data is read without REQ flag, the key data is unexpected data.

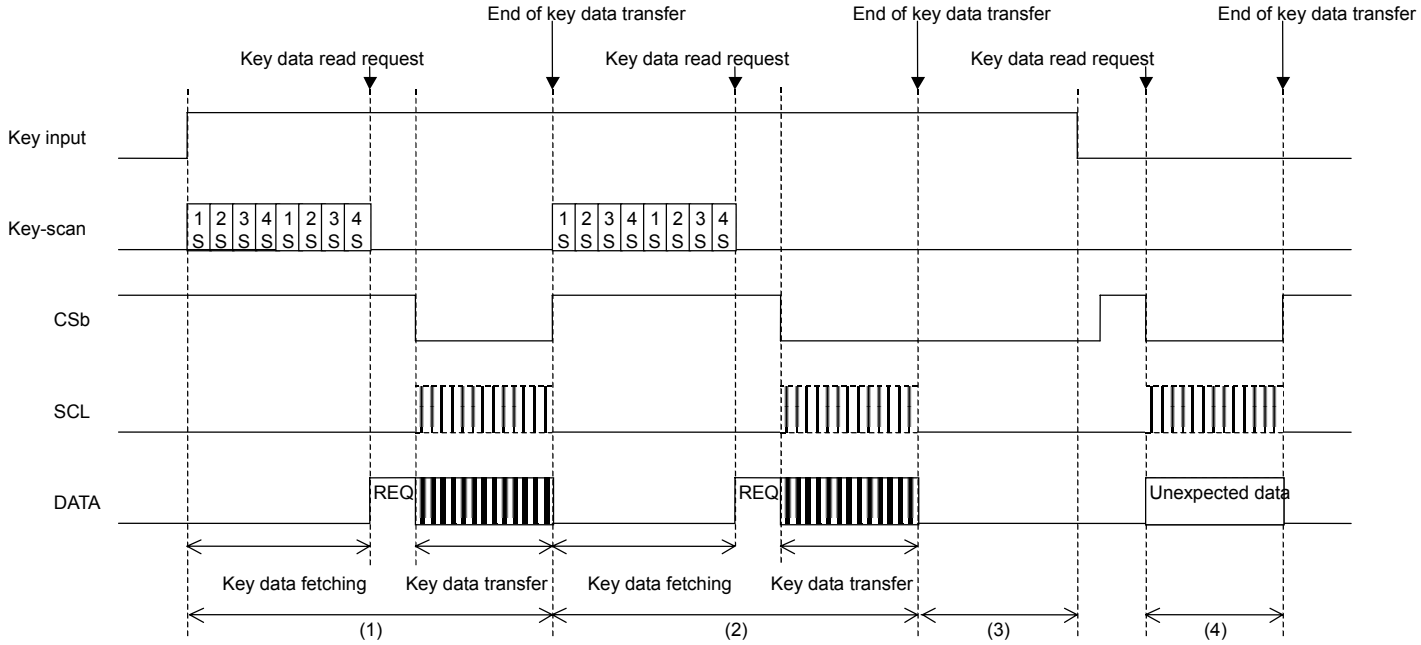


Fig. 10 Example of Key-scan Operating

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITION
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V	
Input Voltage	V_{IN1}	-0.3 ~ V_{DD}+0.3	V	CSb, SCL, TEST terminals
Operating Temperature	Topr	-40 ~ +105	°C	
Storage Temperature	Tstg	-55 ~ +125	°C	
Power Dissipation	P_D	300	mW	

Note 1) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as VSS = 0V.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics 1

(V_{DD}=2.4~3.6V, V_{SS}=0V, Ta=-40~+105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Power Supply	V_{DD}		2.4		3.6	V	
"H" Level Input Voltage (1)	V_{IH1}	CSb, SCL, TEST	0.8V_{DD}		V_{DD}	V	
"L" Level Input Voltage (1)	V_{IL1}	CSb, SCL, TEST	0		0.2V_{DD}	V	
"H" Level Input Voltage (2)	V_{IH2}	K0~K5	0.8V_{DD}		V_{DD}	V	
"L" Level Input Voltage (2)	V_{IL2}	K0~K5	0		0.2V_{DD}	V	
Hysteresis Voltage	V_H	CSb, SCL		0.2V_{DD}		V	
"H" Level Input Current	I_{IH}	V_{IN}=V_{DD} CSb, SCL			1.0	uA	
"L" Level Input Current	I_{IL}	V_{IN}=V_{SS} CSb, SCL			1.0	uA	
"H" Level Output Voltage (1)	V_{OH1}	I_O=-10uA, V_{DD}=3.0V, S0~S3	0.8V_{DD}		V_{DD}	V	
"L" Level Output Voltage (1)	V_{OL1}	I_O=+250uA, V_{DD}=3.0V, S0~S3	V_{SS}		0.2V_{DD}	V	
"H" Level Output Voltage (2)	V_{OH2}	DATA, I_O=1mA, V_{DD}=3.0V	2			V	
"L" Level Output Voltage (2)	V_{OL2}	DATA, I_O=-1mA, V_{DD}=3.0V			0.5	V	
Pull-up Resistance Current	I_p	V_{DD}=3.0V, V_{IN}=V_{DD}, K0~K5	-5	-15	-25	uA	
Oscillating Frequency	fosc		45	65	85	kHz	
Operating Current	I_{DD}	VDD=3V, Ta=25°C		20	40	uA	

• DC Characteristics 2

(V_{DD}=4.5~5.5V, V_{SS}=0V, Ta=-40~+105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Power Supply	V_{DD}		4.5		5.5	V	
"H" Level Input Voltage (1)	V_{IH1}	CSb, SCL, TEST	0.8V_{DD}		V_{DD}	V	
"L" Level Input Voltage (1)	V_{IL1}	CSb, SCL, TEST	0		0.2V_{DD}	V	
"H" Level Input Voltage (2)	V_{IH2}	K0~K5	0.8V_{DD}		V_{DD}	V	
"L" Level Input Voltage (2)	V_{IL2}	K0~K5	0		0.2V_{DD}	V	
Hysteresis Voltage	V_H	CSb, SCL		0.2V_{DD}		V	
"H" Level Input Current	I_{IH}	V_{IN}=V_{DD} CSb, SCL			1.0	uA	
"L" Level Input Current	I_{IL}	V_{IN}=V_{SS} CSb, SCL			1.0	uA	
"H" Level Output Voltage (1)	V_{OH1}	I_O=-20uA, V_{DD}=5.0V, S0~S3	0.8V_{DD}		V_{DD}	V	
"L" Level Output Voltage (1)	V_{OL1}	I_O=+500uA, V_{DD}=5.0V, S0~S3	V_{SS}		0.2V_{DD}	V	
"H" Level Output Voltage (2)	V_{OH2}	DATA, I_O=1mA, V_{DD}=5.0V	4			V	
"L" Level Output Voltage (2)	V_{OL2}	DATA, I_O=-1mA, V_{DD}=5.0V			0.5	V	
Pull-up Resistance Current	I_p	V_{DD}=5.0V, V_{IN}=V_{DD}, K0~K5	-10	-25	-65	uA	
Oscillating Frequency	fosc		45	65	85	kHz	
Operating Current	I_{DD}	VDD=5V, Ta=25°C		45	80	uA	

• AC Characteristics 1

(V_{DD}=2.4~3.6V, V_{SS}=0V, Ta=-40~+105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
"L" Level Clock Pulse Width	t_{WCLL}		260			ns	
"H" Level Clock Pulse Width	t_{WCLH}		260			ns	
CSb Wait Time	t_{CP}		50			ns	3
CSb Set-up Time	t_{CS}		180			ns	
CSb Hold Time	t_{CH}		100			ns	
Rise Time	t_r				20	ns	
Fall Time	t_f				20	ns	
Key Data Output Delay Time	t_{KDD}	DATA terminal, CL=50pF			230	ns	

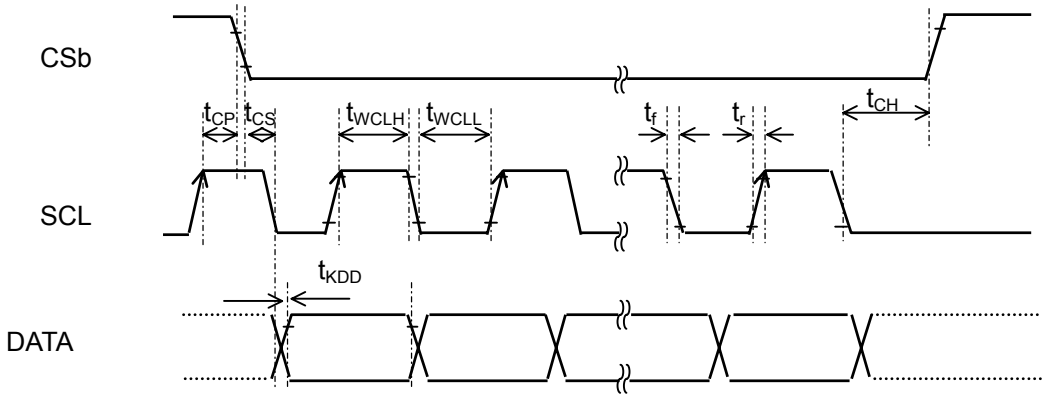
• AC Characteristics 2

(V_{DD}=4.5~5.5V, V_{SS}=0V, Ta=-40~+105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
"L" Level Clock Pulse Width	t_{WCLL}		230			ns	
"H" Level Clock Pulse Width	t_{WCLH}		230			ns	
CSb Wait Time	t_{CP}		50			ns	3
CSb Set-up Time	t_{CS}		180			ns	
CSb Hold Time	t_{CH}		100			ns	
Rise Time	t_r				20	ns	
Fall Time	t_f				20	ns	
Key Data Output Delay Time	t_{KDD}	DATA terminal, CL=50pF			200	ns	

Note 3) t_{CP} is the time when SCL is kept at “H” during CSb changed from “H” to “L”. When SCL is “L”, this specification is not applied.

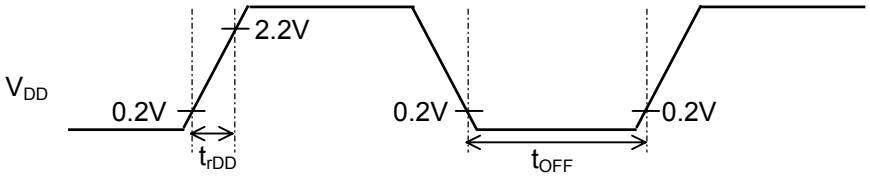
• Output Timing



- Power supply condition when hardware reset circuit is used

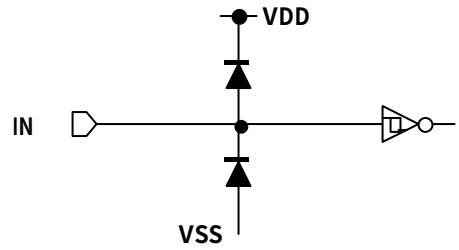
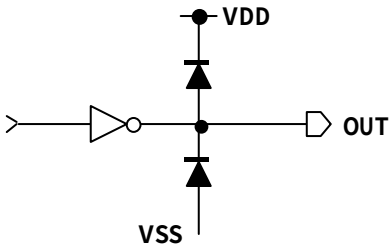
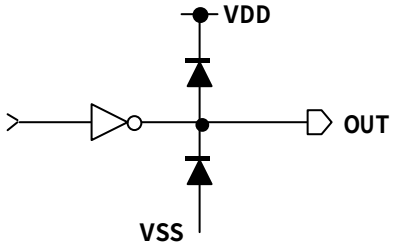
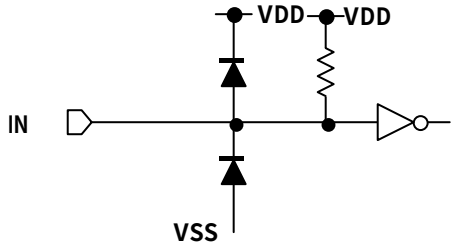
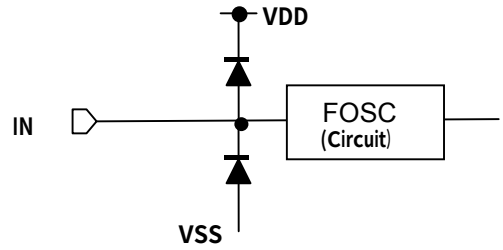
(Ta=-40~105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power-on Rising Time	t_{rDD}		0.1		5	ms
Power-off Time	t_{OFF}		1			ms



Note 4) t_{OFF} is the off time when power-supply turns off suddenly or cycles on/off.

Input and Output terminal structure

	
CSb, SCL	DATA
	
S0～S3	K0~K5
	
TEST	

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