1bit Delta-Sigma Stereo ADC

■ General Description

The NJU3610 is the stereo Analog to Digital Convector (ADC) that covers from 8 to 192 kHz sampling frequency. The NJU3610 provides 1bit Delta-Sigma technology with high accuracy and low power consumption. The analog inputs are differential signal and stereo 4-1 selectors are provided. The NJU3610 provides two power-supply 1.8V / 3.3V(typical) or single power-supply 3.3V(typical) application.

■ Package

NJU3610FR3

■ Features

- 1bit Delta-Sigma stereo ADC
- 64fs over sampling (MCK=256fs, 384fs)
- 32fs over sampling (MCK=128fs)
- Digital Filter
- High-pass filter
- Stereo 4-1 selectors
- Sampling Rate : 8 to 192kHz
- Dynamic Range : 100dB(typ@3.3V, 96kHz)
- S/N : 100dB(typ@3.3V, 96kHz)
- S/(N+D) : 90dB(typ@3.3V, 48kHz, -1.0dBFS)
- Master Clock : 128fs(8 to 192kHz), 256fs / 384fs(8 to 96kHz)
- Power Supply : Single power supply 3.0 to 3.6V(3.3Vtyp) Built-in regulator using together
  : Two power supply 3.0 to 3.6V(Analog, I/O:3.3Vtyp)
  1.65 to 2.0V(Digital:1.8Vtyp)
- Digital Audio Format : 24/16bit Left-justified, I^2S Master/Slave
- Operating Temperature : -40 to +85°C
- Package : LQFP48-R3 (Pb-Free)

■ Function Block Diagram

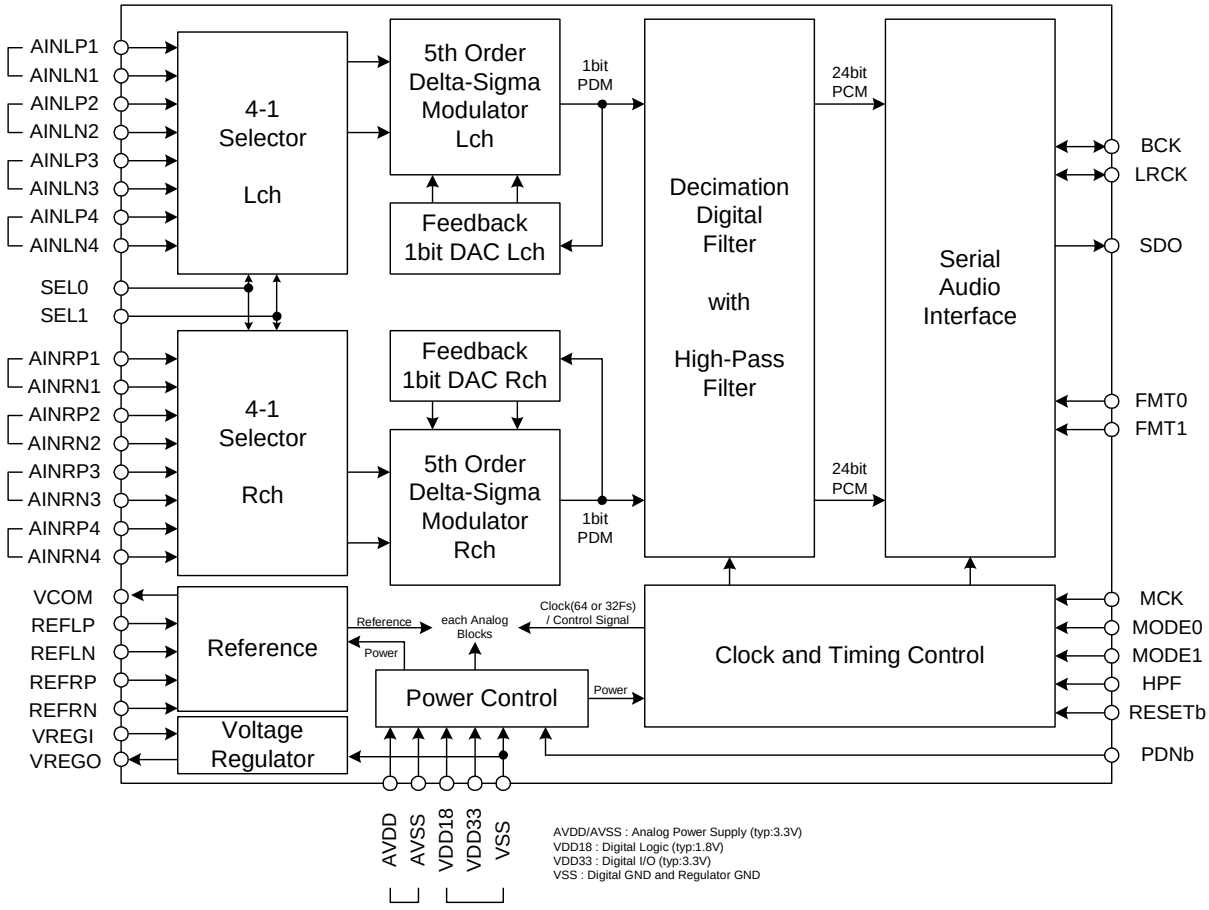


Fig. 1 NJU3610 Block Diagram

■ **Pin Configuration**

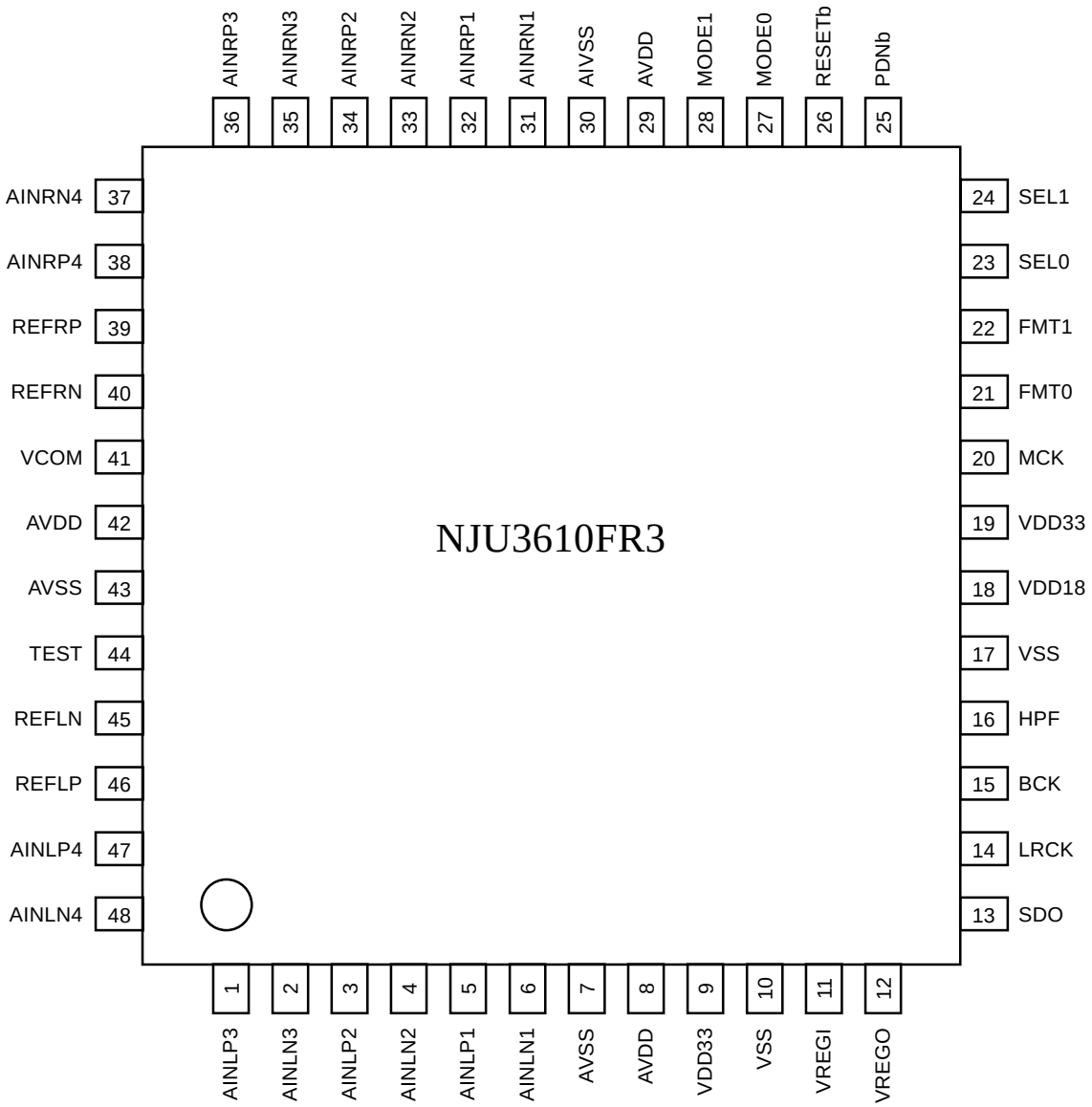


Fig.2 NJU3610 Pin Configuration

■ Pin Description

Table.1 Pin Description

Pin No.	Symbol	I/O	Description
1	AINLP3	AI	Lch Analog Positive Input 3 Pin
2	AINLN3	AI	Lch Analog Negative Input 3 Pin
3	AINLP2	AI	Lch Analog Positive Input 2 Pin
4	AINLN2	AI	Lch Analog Negative Input 2 Pin
5	AINLP1	AI	Lch Analog Positive Input 1 Pin
6	AINLN1	AI	Lch Analog Negative Input 1 Pin
7	AVSS	AG	Analog Ground Pin
8	AVDD	AP	Analog Power Supply Pin, 3.3V
9	VDD33	DP	Digital Power Supply Pin, 3.3V
10	VSS	DG	Digital Ground Pin
11	VREGI	RI	Built-in Regulator Input Pin, 3.3V
12	VREGO	RO	Built-in Regulator Output Pin, 1.8V (typ)
13	SDO	DO	Audio Serial Data Output Pin
14	LRCK	DIO	LR Clock
15	BCK	DIO	Bit Clock
16	HPF	DI	HPF for Off-set Cancel (“H”: ON, “L”: OFF)
17	VSS	DG	Digital Ground Pin
18	VDD18	DL	Digital Power Supply Pin, 1.8V
19	VDD33	DP	Digital Power Supply Pin, 3.3V
20	MCK	DI	Master Clock Input Pin
21	FMT0	DI	Control Serial Data Format 0 Pin
22	FMT1	DI	Control Serial Data Format 1 Pin
23	SEL0	DI	Control Input Selector 0 Pin
24	SEL1	DI	Control Input Selector 1 Pin
25	PDNb	DI	Power Down Mode Pin (”H”: Power up, “L”: Power down)
26	RESETb	DI	Reset Pin (“H”: Reset OFF, “L”: Reset ON)
27	MODE0	DI	Control Mode 0 Pin
28	MODE1	DI	Control Mode 1 Pin
29	AVDD	AP	Analog Power Supply Pin, 3.3V
30	AVSS	AG	Analog Ground Pin
31	AINRN1	AI	Rch Analog Negative Input 1 Pin
32	AINRP1	AI	Rch Analog Positive Input 1 Pin
33	AINRN2	AI	Rch Analog Negative Input 2 Pin
34	AINRP2	AI	Rch Analog Positive Input 2 Pin
35	AINRN3	AI	Rch Analog Negative Input 3 Pin
36	AINRP3	AI	Rch Analog Positive Input 3 Pin
37	AINRN4	AI	Rch Analog Negative Input 4 Pin
38	AINRP4	AI	Rch Analog Positive Input 4 Pin
39	REFRP	AI	Rch Voltage Reference Input Pin, AVDD
40	REFRN	AI	Rch Voltage Reference Input Pin, GND
41	VCOM	AO	Common Voltage Output Pin, AVDD/2 Connected to AVSS with a 10uF electrolytic capacitor.
42	AVDD	AP	Analog Power Supply Pin, 3.3V
43	AVSS	AG	Analog Ground Pin
44	TEST	AI	Test Pin (Connected to AVSS)
45	REFLN	AI	Lch Voltage Reference Input Pin, GND
46	REFLP	AI	Lch Voltage Reference Input Pin, AVDD
47	AINLP4	AI	Lch Analog Positive Input 4 Pin
48	AINLN4	AI	Lch Analog Negative Input 4 Pin

* AP : Analog power supply, 3.3V
AG : Analog ground
AI : Analog input
AO : Analog output
DP : Digital power supply, 3.3V
DL : Digital power supply, 1.8V
DG : Digital ground and built-in regulator ground
RI : built-in regulator input
RO : built-in regulator output
DI : Digital input
DO : Digital output
DIO : Bi-directional of Digital

■ Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings (VSS=AVSS=0V=GND, Ta=25°C)

Parameter		Symbol	Rating	Units
Power supplies	Analog	AVDD	-0.3 to +4.2	V
	Digital	VDD33	-0.3 to +4.2	
		VDD18	-0.3 to +2.3	
	Built-in Regulator Input	VREGI	-0.3 to +4.2	
	Built-in Regulator Output	VREGO	-0.3 to +2.3	
Pin Voltage	Digital Input	$V_{x(IN)}$	-0.3 to +5.5 (VDD33≥3.0V) -0.3 to +4.2 (VDD33<3.0V)	
	Digital Output	$V_{x(OUT)}$	-0.3 to VDD33 + 0.3	
	Analog Input	$V_{x(AIN)}$	-0.3 to AVDD + 0.3	
	VCOM Output	$V_{x(VCOM)}$		
Power Dissipation		P_D	800 Mounted on two-layer board of based on the JEDEC.	mW
Operating Temperature		T_{OPR}	-40 to +85	°C
Storage Temperature		T_{STR}	-40 to +125	°C

* AVDD : 8, 29, 42pin
* VDD33 : 9pin
* VDD18 : 18pin
* VREGI : 11pin
* VREGO : 12pin
* $V_{X(IN)}$: 16, 20-28pin, and 14-15pin (set in the state of the input.)
* $V_{X(OUT)}$: 13pin, and 14-15pin (set in the state of the output.)
* $V_{X(AIN)}$: 1-6, 31-40, 44-48pin
* $V_{X(VCOM)}$: 41pin

Note 1) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 2) Please do not open the digital input terminal. Moreover, please do not open the digital I/O terminal set in the state of the input.

■ Recommended operating conditions

Table 3. Recommended operating conditions

Parameter		Symbol	Recommended operating conditions	Units
Power Supplies	Analog	AVDD *1	3.0 to 3.6 AVDD33≥VDD33	V
	Digital	VDD33 *1		
		VDD18 *2	1.65 to 2.0 (Or, a built-in regulator supplies the voltage.)	
	Built-in Regulator Input	VREGI *3	3.0 to VDD33	

*1 VDD33 is recommended to be turned on from AVDD and simultaneous or AVDD back.
*2 The power up sequence VDD18 is not critical.
*3 When a built-in regulator is used, VREGI is connected with VDD33. When a built-in regulator is not used, VREGI and VREGO are connected with VSS.

■ Electric Characteristics

Table 4. Analog Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Full-scale voltage level *1	AIN*** Pin (Differential one side)	AVDD x 0.7			Vpp
	AIN*** Pin (Between differential motions)	AVDD x 1.4			
S/(N+D) (-1.0dBFS)	fs=48kHz	85	90	-	dB
	fs=96kHz	-	90	-	
	fs=192kHz	-	90	-	
Dynamic Range (-60dBFS, A-weighted)	fs=48kHz	93	99	-	dB
	fs=96kHz	-	100	-	
	fs=192kHz	-	100	-	
S/N (A-weighted)	fs=48kHz	93	99	-	dB
	fs=96kHz	-	100	-	
	fs=192kHz	-	100	-	
Cross Talk (During the selection and non-selection)	fs=48kHz, 1kHz BPF	-	110	-	dB
Channel Separation (Between L and R)	fs=48kHz, 1kHz BPF	97	110	-	dB
Equivalent input impedance (Selection input terminal)	fs=48kHz	-	100	-	kOhm
	fs=96kHz	-	50	-	
	fs=192kHz	-	50	-	
Input impedance *2 (Non-Selection input terminal)	fs=48kHz	40	58	-	KOhm
	fs=96kHz	40	58	-	
	fs=192kHz	40	58	-	
Gain Mismatch	fs=48kHz	-0.1	-	0.1	dB

(Ta=25°C, AVDD=VDD33=3.3V, VDD18=VREGO, HPF=ON, Input signal=1kHz(AINL*4/AINR*4), BCK=64fs, MCK=256fs(48/96kHz), 128fs(192kHz), Measurement frequency=20Hz-20kHz at fs=48kHz, 20Hz-40kHz at fs=96kHz, 20Hz-40kHz at fs=192kHz)

*1 The full-scale voltage level indicates full-scale value (0dBFS) of the analog input voltage. A full-scale voltage is proportional to the AVDD voltage. The meaning between differential motions is an operation result of the differential input signal. The input voltage of the terminal is up to AVDD voltage.

*2 The analog input terminal of non-selection does the bias to VCOM by the resistance of this value.

Table 5. Power Supply Current （Ta=25°C, AVDD=VDD33=3.3V, VDD18=1.8V）

Parameter	Condition	Min.	Typ.	Max.	units
3.3V, Power Supply Current: I_{DD} + I_{DDA} (Not contain a built-in regulator)	fs=48kHz	-	7.0	-	mA
	fs=96kHz	-	8.0	-	
	fs=192kHz	-	8.0	12	
1.8V, Power Supply Current: I_{DDL} (Not contain a built-in regulator)	fs=48kHz	-	2.0	-	mA
	fs=96kHz	-	4.0	-	
	fs=192kHz	-	8.0	10	
Power down mode: I_{DDQ}+I_{DDLQ} (Not contain a built-in regulator)	Clock stop PDNb=Low	-	-	100	μA
Built-in regulator Current: I_{RIN}	VREGI=3.3V I_{OUT}=0mA	-	50	70	μA

Table 6. Digital DC Characteristics (Ta=25°C, VDD33=3.3V, VDD18=1.8V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{IH}		2.2	-	VDD33 *1	V
Low-Level Input Voltage	V_{IL}		0	-	0.8	V
High-Level Output Voltage	V_{OH}	I_{OH}=-1mA	VDD33 x 0.8	-	VDD33	V
Low-Level Output Voltage	V_{OL}	I_{OL}=1mA	0	-	VDD33 x 0.2	V
Input Leakage Current	I_{IN}	V_{IN}=VSS, VDD	-10	-	10	μA

*1 The digital input terminal and the input digital I/O terminal are 5V tolerant only at VDD33 ratings.

Table 7. Reset AC Characteristics (Ta=25°C, VDD33=3.3V, VDD18=1.8V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Reset Time	t_{RESETb}	RESETb	100	-	-	ns

Table 8. Digital Filter Characteristics (Ta=25°C, VDD33=3.3V, $VDD18_L$=1.8V)

Parameter	Condition	Min.	Typ.	Max.	Units
Cut-off frequency (HPF=High)	-3.0dB	-	fs/44100	-	Hz
LPF Pass band		0	-	0.454	fs
LPF Pass band ripple		-	-	±0.005	dB
LPF Stop band		0.546	-	-	fs
LPF Stop band attenuation		-80	-	-	dB
Group Delay		-	27	-	1/fs

Table 9. Clock Timing (Ta=25°C, VDD33=3.3V, VDD18=1.8V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
MCK Frequency *1	f_{MCK}	128fs	1.024	-	24.576	MHz
		256fs	2.048	-	24.576	
		384fs	3.072	-	36.864	
BCK Frequency *2	f_{SCK}	Slave	0.256	-	12.288	MHz
LRCK Frequency *2	f_{LRCK}	Slave	8.0	-	192	kHz
MCK Pulse Width Low	t_{MIL}		$0.475/f_{MCK}$	$0.5/f_{MCK}$	$0.525/f_{MCK}$	ns
MCK Pulse Width High	t_{MIH}		$0.475/f_{MCK}$	$0.5/f_{MCK}$	$0.525/f_{MCK}$	
BCK Pulse Width Low	t_{SIL}	Slave	35	$0.5/f_{MCK}$	-	ns
BCK Pulse Width High	t_{SIH}	Slave	35	$0.5/f_{MCK}$	-	
BCK to LRCK *3	t_{SLI}	Slave	20	-	-	ns
LRCK to BCK *3	t_{LSI}	Slave	20	-	-	ns

*1 For fs=8 to 192kHz at 128fs mode. For fs=8 to 96kHz at 256fs/384fs mode.
*2 MCK should synchronized with BCK and LRCK. (Not necessary to phase it.)
*3 BCKI rising edge must not occur at the same time as LRCK edge

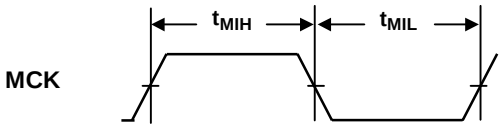


Fig.3 MCK Timing diagram

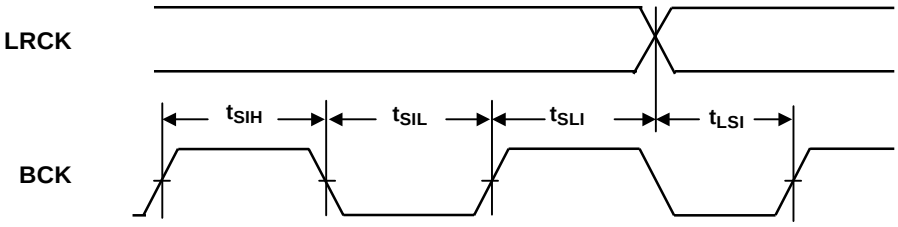


Fig.4 BCK, LRCK Timing Diagram

Table 10. Serial Audio Output Timing (Ta=25°C VDD33=3.3V, VDD18=1.8V)

Parameter	symbol	Condition	Min.	Typ.	Max.	Units
BCK to LRCK Time *1	t_{SLO}	CL=25pF	-20	-	20	ns
Data Output Delay	t_{DOD}	CL=25pF	-	-	20	ns

*1 It is regulation in Master mode.

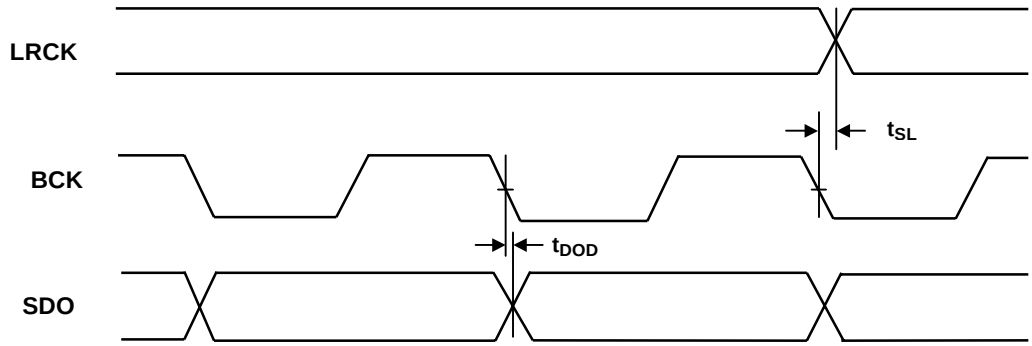


Fig.5 Serial Audio Output Timing Diagram

1. Power-supply, RESET , Power Down

1.1 Power-supply

The power-supply should be used under the recommended condition. The power-on level procedure should increase monotonously. During the operation, the power-supply should not become out of the recommended condition.

The large size decoupling capacitor should be implemented near the NJU3610. The analog/digital power line should be taken from this large capacitor. Also the power-supply terminals should have enough decoupling capacitors to the terminals.

The REFLP, REFLN, REFRP, REFRN are the reference voltage terminals of the 1bit-feedback-DAC. The REFLP and REFRP should be connected to AVDD power line. The REFLPN and REFRN should be connected to AVSS line. These terminals affect the analog performance, so the decoupling capacitor is very important.

The VCOM output is the half of the AVDD voltage level with the voltage-follower buffer. The VCOM voltage level is the internal reference. The non-selected input terminals are pull-upped to the internal reference via 58k-ohm resistors. The 10uF capacitor is recommended to improve noise and channel separation performance. This terminal output is available for the analog reference level of the input circuit.

The NJU3610 provides the internal voltage regulator for internal digital circuit. The VREGI terminal is the input to the internal regulator. The input to VREGI should be the same voltage as VDD33 input. The output of the internal voltage regulator is VREGO. If the VREGO output is connected to VDD18, no other 1.8V power-supply is necessary.

If the internal voltage regulator is used, put the capacitor (around 4.7 to 10uF) between VREGO and VSS.

If the internal voltage regulator is not used, connect both VREGI and VREGO to VSS.

The internal voltage regulator is provided for the NJU3610 circuit, do not use it for the other circuit.

If the VDD33 and AVDD are different power-supply, follow the next power-on procedure.

First power on analog power-supply (AVDD). Next power on digital power-supply (VDD33).

Also it is possible to power on analog and digital power-supply simultaneously.

Power-on Timing Condition: AVDD (before) ≥ VDD33 (same or after)

There is no constraining on VDD18 power-on procedure. Also there is no constraining on power-down procedure for all power-supplies.

1.2 Digital Input Terminal

All digital input terminals are 5V tolerant under the recommended VDD33 power-on condition. Also BCK and LRCK that are assigned as input mode are 5V tolerant under the recommended VDD33 power-on condition.

Input/output setting of BCK and LRCK are defined by FMT1 terminal. These terminals are input mode in case of FMT1 = “Low” and output mode in case of FMT1 = “High”.

During RESETb terminal = ”Low”, BCK and LRCK are input mode regardless of FMT1 condition.

1.3 RESET and Power Down

During RESETb terminal = ”Low”, digital filter and analog integrator are initialized and SDO output is low level.

The internal reference voltage generator is operating during RESETb terminal = ”Low”.

If the terminal setting or clock is changed under ADC operation, RESETb should be initialized again.

In case of PDNb = ”Low”, all analog circuit become power-down mode. The digital filter is operating under PDNb = ”Low”, but the clock to analog circuit is stopped. If power-down mode is not used, PDNb should be “high”.

After power-on, the next reset procedure should be done at least one time to initialize the NJU3610. RESETb should be “Low” level and become “High” level again. Changing PDNb from “Low “level to “High” level makes VCOM reference level generated. The setup time of VCOM-reference-level depends on the attached capacitor.

The procedure to change RESETb level (“Low” to “High”) should be done, after VCOM level becomes stable.

The procedure of SDO audio data output is as following: First RESET is released from “Low” to “High” level. After RESET release, wait 136±8fs period and SDO generates audio data. But to get the accurate output data, VCOM reference level should become half of AVDD level.

If the High Pass Filter is used to cancel offset (HPF=”High”), some more time (max. 8192fs) after generating audio data is necessary to get accurate output data.

In order to power down the NJU3610 completely, PDNb should be “Low” and, also clocks to MCK, BCK and LRCK should be stopped.

Notice:

The internal regulator does not provide power-down mode. As far as power is supplied to VREG1, it generates output voltage with consuming power.

2. ADC Function

2.1 Clock and Digital Audio Interface

The NJU3610 requires MCK, BCK and LRCK audio clock. BCK and LRCK can be generated by MCK in Master mode. MCK, BCK and LRCK are synchronized in Master mode.

In Slave mode, BCK and LRCK are inputted from the outside. In Slave mode, MCK, BCK and LRCK should be synchronized. But it is not necessary that the phase of these three clocks are synchronized.

MCK frequency should be one of 128fs, 256fs or 384fs. If fs>96KHz, MCK should be 128fs. The ADC operates with the next frequency. The operate frequency is 64fs in case of fs≦96KHz. The operate frequency is 32fs in case of fs>96KHz.

Mode0 and mode1 terminals select the MCK frequency and ADC operating frequency.

In case that ADC operating frequency is 32fs, the effective bandwidth is 1/4fs. Between 1/4fs and 1/2fs, ADC shaping noise exists.

The NJU3610 digital audio format provides Left-justified and I^2S 24bit(BCK=64clocks/fs) in Master mode. The NJU3610 digital audio format provides Left-justified, I^2S 16bit (BCK=32clocks/fs) and I^2S 24bit(BCK=64clocks/fs) in Slave mode.

FMT0 and FMT1 terminals select the above digital audio format. When FMT0, FMT1, MODE0 and MODE1 are changed, RESET should be done again.

MCK, BCK and LRCK frequency is shown in table11. Digital Audio Format and operation mode is shown in table12. In Master mode, BCK and LRCK terminals generate clocks. BCK output clock is fixed at 64fs in Master mode. In Slave mode, BCK and LRCK terminals are assigned input.

Table 11. MCK, BCK, LRCK (1)

LRCK(kHz) Master: Generation from MCK Slave: From outside	MCK (MHz)			BCK(MHz)	
	128fs	256fs	384fs	32fs Slave only: from outside	64fs Master: Generation from MCK Slave: From outside
8	-*2	2.048	3.072	0.256	0.512
16	-*2	4.096	6.144	0.512	1.024
22.05	-*2	5.6448	8.4672	0.7056	1.4112
32	-*2	8.192	12.288	1.024	2.048
44.1	-*2	11.2896	16.9344	1.4112	2.8224
48	-*2	12.288	18.432	1.536	3.072
64	-*2	16.384	24.576	2.048	4.096
88.2	-*2	22.5792	33.8688	2.8224	5.6448
96	-*2	24.576	36.864	3.072	6.144
176.4 *1	22.5792	-	-	5.6448	11.2896
192 *1	24.576	-	-	6.144	12.288

*1 It is only a setting of "CKMODE[1:0]=10,11". At this time, frequency bandwidth is up to 1/4fs. The shaping noise of the ADC is included in the band from 1/4fs to 1/2fs.

*2 Because an effective bandwidth is limited, it is not practicable.

Table 12. MCK,BCK,LRCK (2)

CMKODE		FMT		Master / Slave	A/D mode	MCK (fs)	Format
1	0	1	0				
0	0	0	0	Slave	64fs	256fs (≦96kHz)	I^2S (32 or 64fs)
0	0	0	1				Left-justified(32 or 64fs)
0	0	1	0	Master			I^2S (64fs)
0	0	1	1				Left-justified(64fs)
0	1	0	0	Slave	64fs	384fs (≦96kHz)	I^2S (32 or 64fs)
0	1	0	1				Left-justified(32 or 64fs)
0	1	1	0	Master			I^2S (64fs)
0	1	1	1				Left-justified(64fs)
1	0	0	0	Slave	32fs	256fs (>96kHz)	I^2S (32 or 64fs)
1	0	0	1				Left-justified(32 or 64fs)
1	0	1	0	Master			I^2S (64fs)
1	0	1	1				Left-justified(64fs)
1	1	0	0	Slave	32fs	128fs (>96kHz)	I^2S (32 or 64fs)
1	1	0	1				Left-justified(32 or 64fs)
1	1	1	0	Master			I^2S (64fs)
1	1	1	1				Left-justified(64fs)

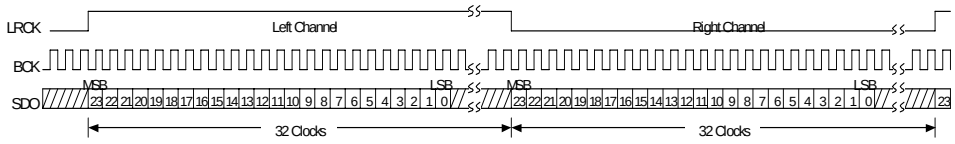


Fig.6 Left-justified Data Format 64fs, 24bit Data

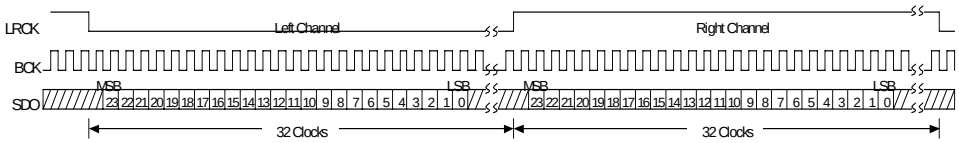


Fig.7 I^2S Data Format 64fs, 24bit Data

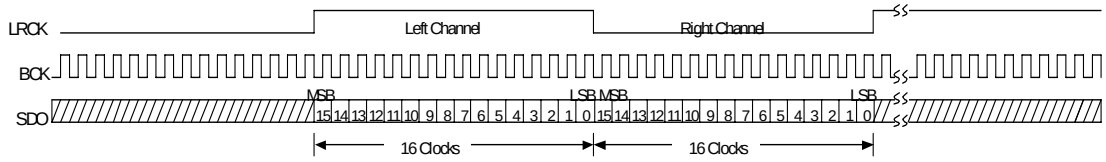


Fig.8 Left-justified Data Format 32fs, 16bit Data

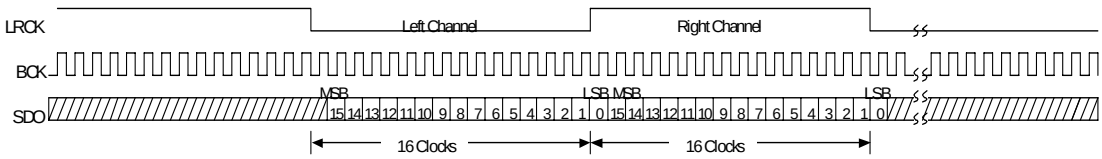


Fig.9 I^2S Data Format 32fs, 16bit Data

2.2 High Pass Filter for offset-cancel

The NJU3610 provides High Pass Filter (digital filter) to cancel offset. Normally HPF terminal is set “High”. In case of HFP=”High”, High Pass Filter is active. The frequency characteristics are shown in table 8. The cutoff frequency is set at low frequency. But sampling rate changes the cutoff frequency. HFP terminal setting can be changed during NJU3610 operating. But changing HPF setup makes pop noise that is caused by offset change.

2.3 Analog Input and 4-1 Selector

The NJU3610 provides four differential-stereo-inputs. SEL0 and SEL1 terminals select one of four stereo-input. After this selector, input signal goes to ADC input. SEL0 and SEL1 combination is shown in table13.

Table 13. SEL1, SEL0 combination

SEL1	SEL0	Lch		Rch	
		Non−reversing input	Reversing input	Non−reversing input	Reversing input
0	0	AINLP1	AINLN1	AINRP1	AINRN1
0	1	AINLP2	AINLN2	AINRP2	AINRN2
1	0	AINLP3	AINLN3	AINRP3	AINRN3
1	1	AINLP4	AINLN4	AINRP4	AINRN4

Each differential-signal input should be biased with VCOM reference level. The half of AVDD level is available instead of VCOM reference level. Input full-scale level (0dBFS) is “AVDDx0.7Vpp”. In differential signal, Input full-scale level is “AVDDx1.4Vpp”. Maximum available input range is from GND to AVDD with distortion. But in this case, the distortion occurs. When AMP with high voltage power-supply is used before the ADC, the input level should not exceed the ADC input range.

SEL0 and SEL1 settings are taken in at MCK rising edge. In case of RESETb=”Low”, AINLP1, AINLN1, AINRP1 and AINRN1 are selected regardless of SEL0/SEL1 settings. In case that PDNb level is changed from “high” to “Low”, the latest condition is maintained.

The terminals that are not selected by SEL0/SEL1 are pull-upped by VCOM bias via 58ohm resisters. The analog input terminals that are not used should be left open or adds the capacitors between terminals and GND. If these terminals connect directly to power-supply or GND, VCOM fluctuates and the NJU3610 does not operate properly.

The NJU3610 operates with 32fs over sampling at Mode1=”High”. The NJU3610 operates with 64fs over sampling at Mode1=”Low”. If noise exists around over sampling frequency, the noise folds back. To avoid this folding back noise, passive RC filter is required.

The example of input buffer circuit is shown in figure10. VCOM output is used for bias level. The J1 selects RCA or XLR input. The RC-passive-filter is consist of Ra/Rb(220ohm), Ca/Cb(100pF) and Cc(200pF). The cutoff frequency of RC-passive-filter is 1447KHz.
This input buffer circuit should be implemented to analog input terminals as far as short distance. The layout pattern should be symmetric.

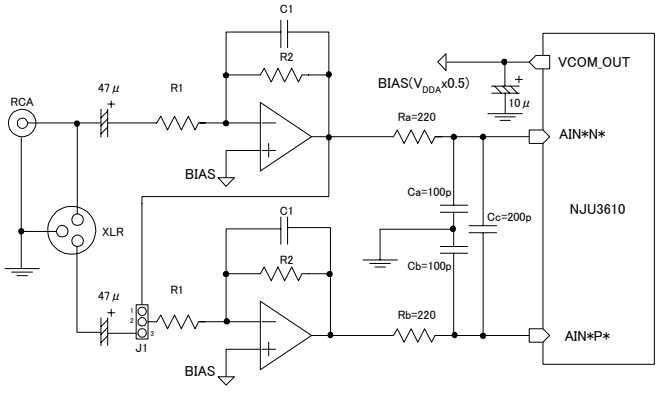
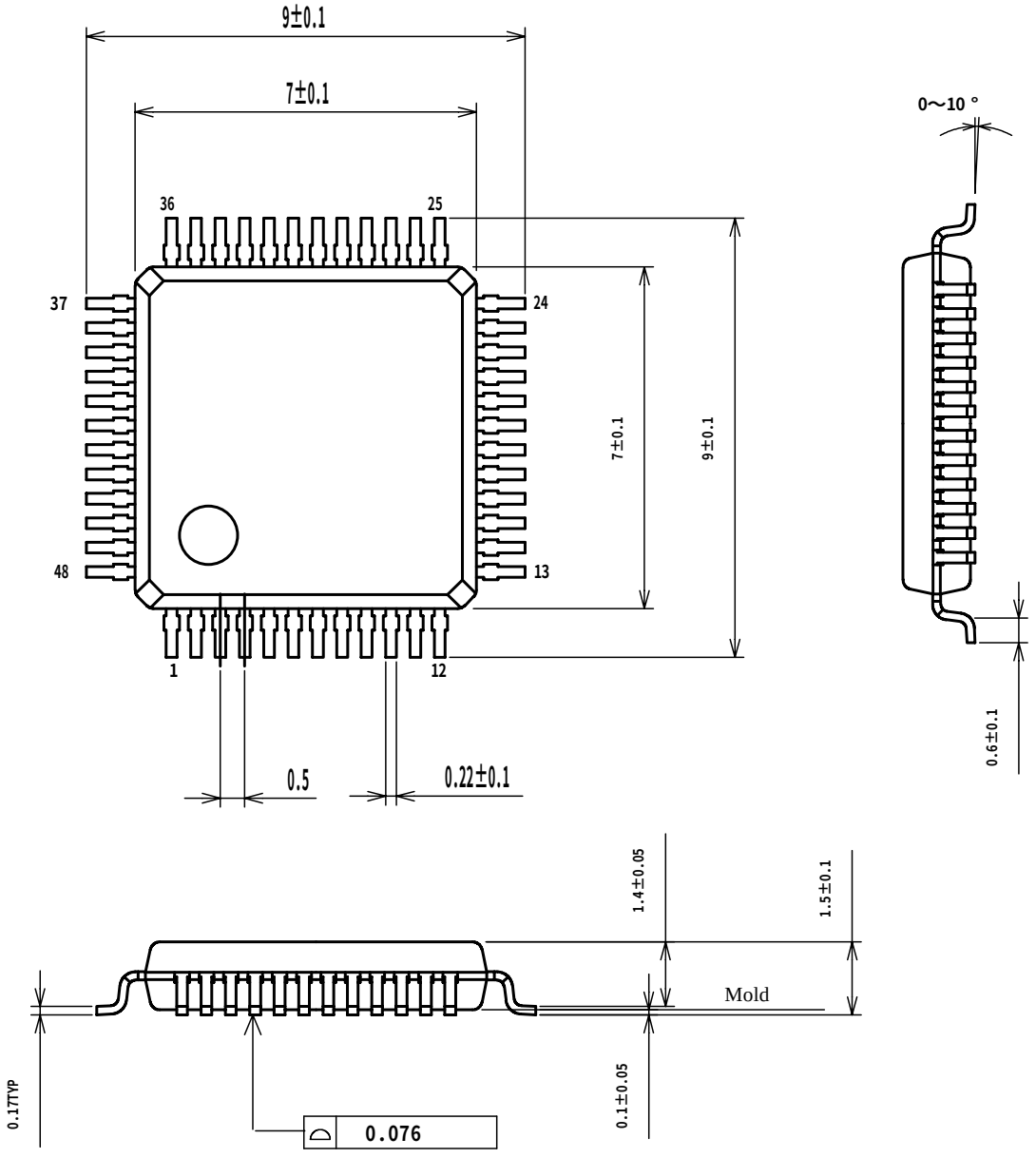


Fig.10 Input buffer example

■ Package dimension

LQFP48-R3 (Pb-Free)



Plating: Sn-Bi