Dolby Virtual Speaker / Dolby Headphone with Dolby Pro Logic IIx Decoder

■ General Description

NJU26226 expand stereo or 5.1 surround signal to 6.1 or 7.1 channel surround sound by Dolby® Pro Logic® IIx technology. NJU26226 provides a highly realistic multi channel speaker surround sound listening environment from as few as headphone or two speakers using Dolby® Pro Logic® IIx and Dolby® Headphone / Dolby® Virtual Speaker technology.
NJU26226 is suitable for Gaming Headsets, digital TVs, stereo mini-components, PCs, and any audio/visual products.

■Package

NJU26226V

■ Features

-Software

- Dolby® Pro Logic® IIx (Max 7.1ch Output)
- Dolby® Virtual Speaker *
- Dolby® Headphone
- Bass Management system *
- Pink Noise Generator
- Multi-channel signals input (Max 7.1ch Input)

*: Dolby Virtual Speaker and Bass Management effective only up to 5.1 channels.

-Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 4 Output ports
- Digital Audio Format : I^2S 24bit, left-justified, right-justified, BCK : 32fs/64fs
- Master / Slave Mode
  - In Master mode, MCK : 256fs @fs=48kHz / 384fs @fs=32kHz
- Microcomputer Interface
  - I^2C Bus (Standard-mode/100kbps, Fast-mode/400kbps)
  - 4 -Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Operating Voltage : V_{DD} = V_{DDPLL} = 1.8V
  : V_{DDIO} = 3.3V
- Input Terminal : 5.0V Input tolerant
- Package : SSOP44 (Pb-Free)

* The detail hardware specification of the NJU26226 is described in the " NJU26200 Series Hardware Data Sheet".

■ Block Diagram

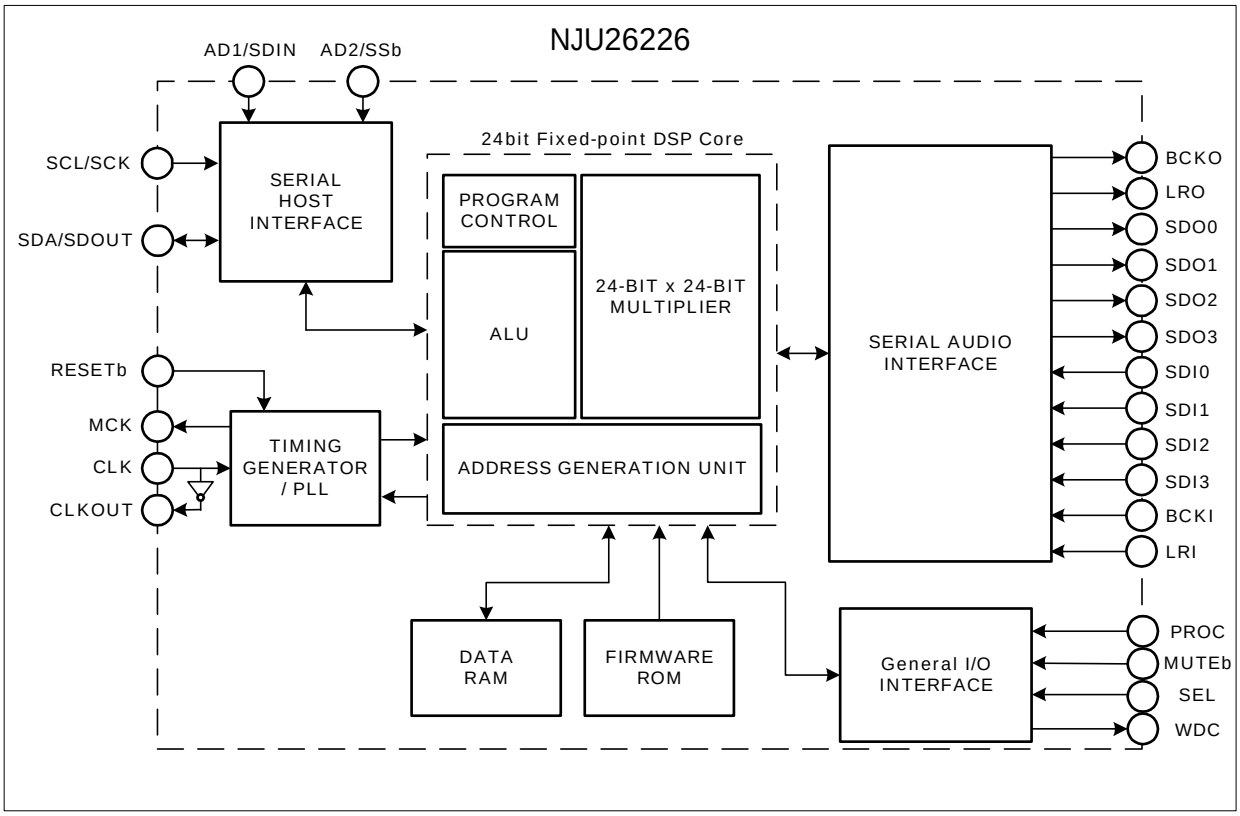


Fig. 1 NJU26226 Hardware Block Diagram

■ Function Block Diagram

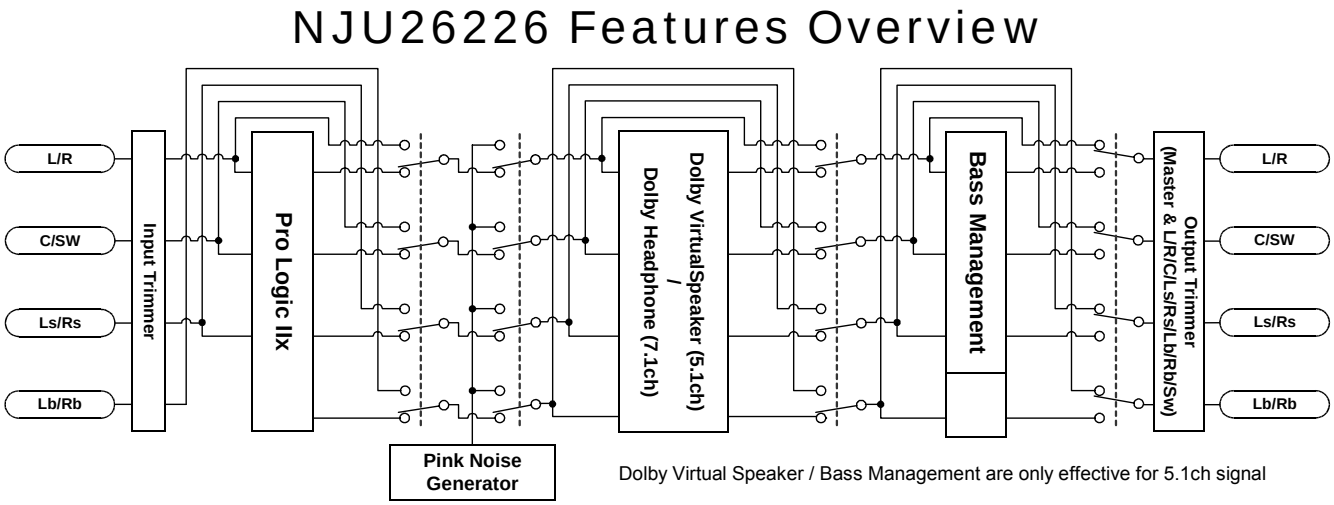


Fig. 2.1 NJU26226 Block Diagram (Outline)

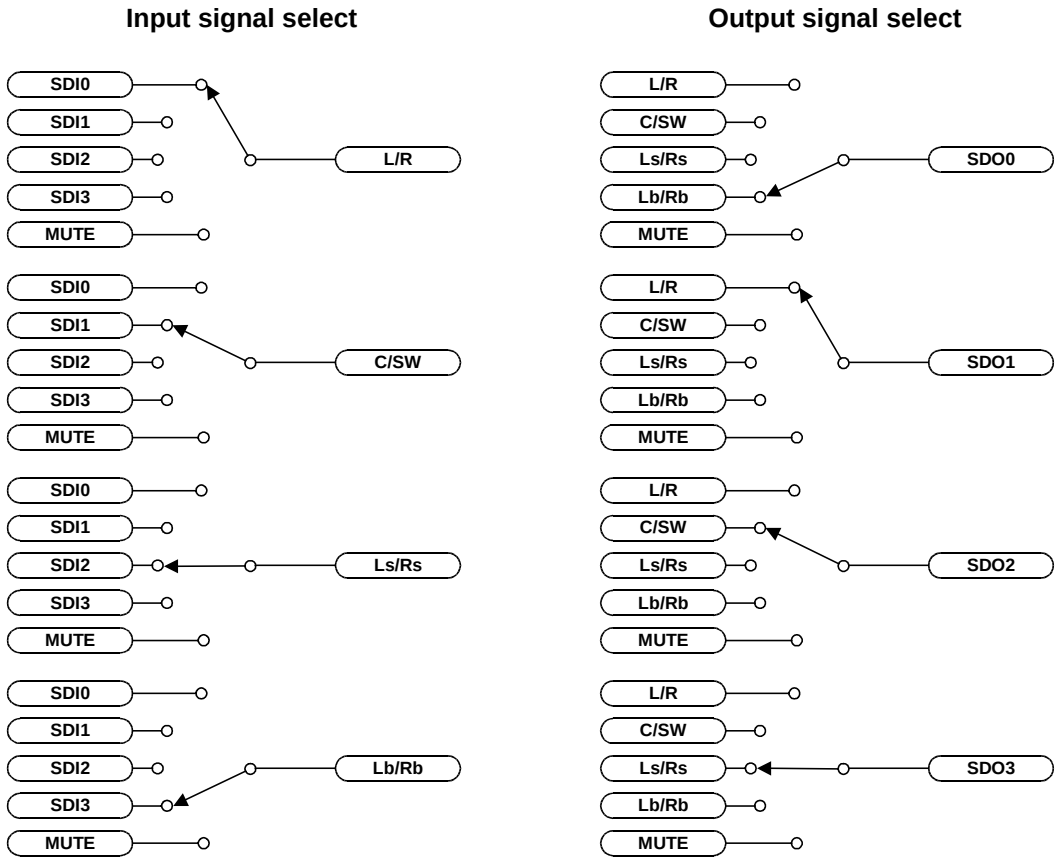
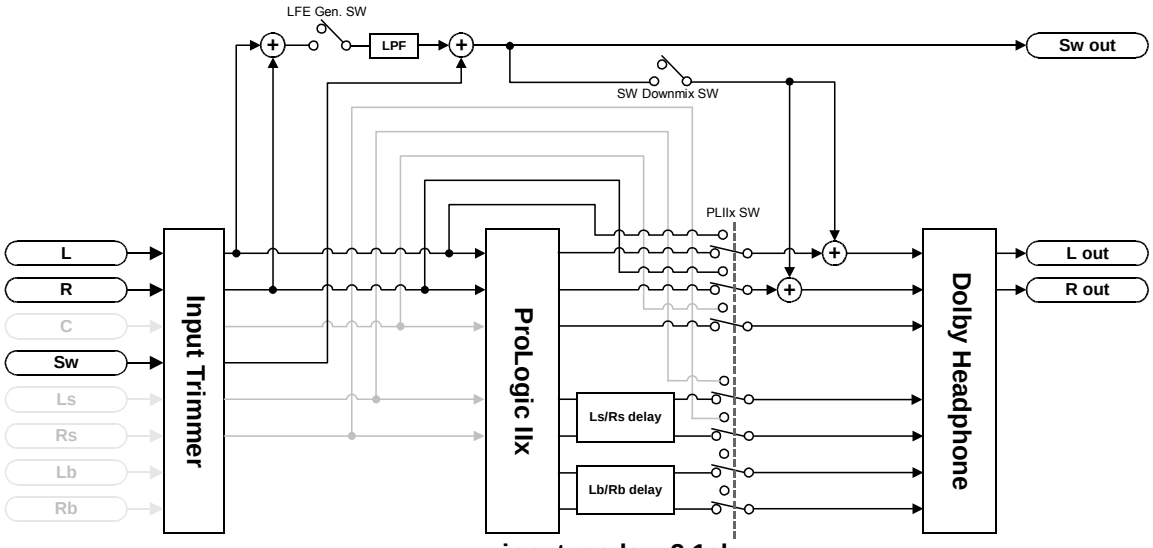
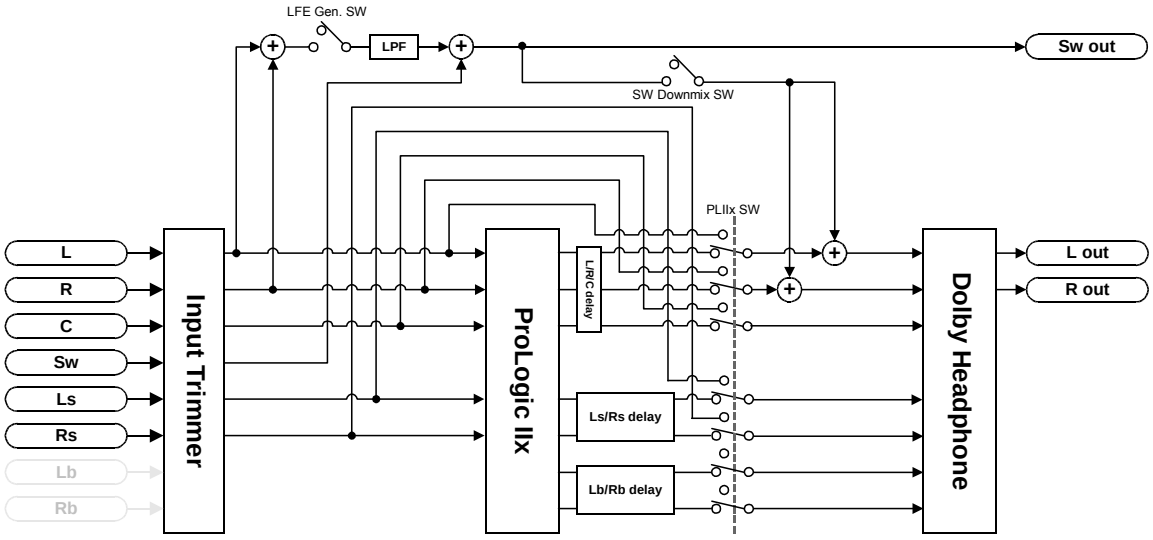


Fig. 2.2 NJU26226 Block Diagram (Input Select block, Output Select block)



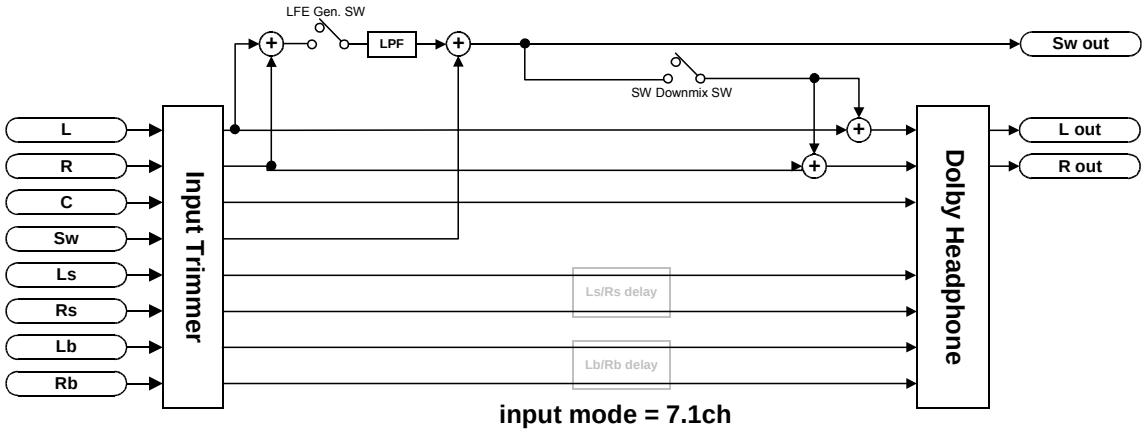
input mode = 2.1ch
DolbyHeadphone enable

Fig. 2.3 NJU26226 Block Diagram (detail)



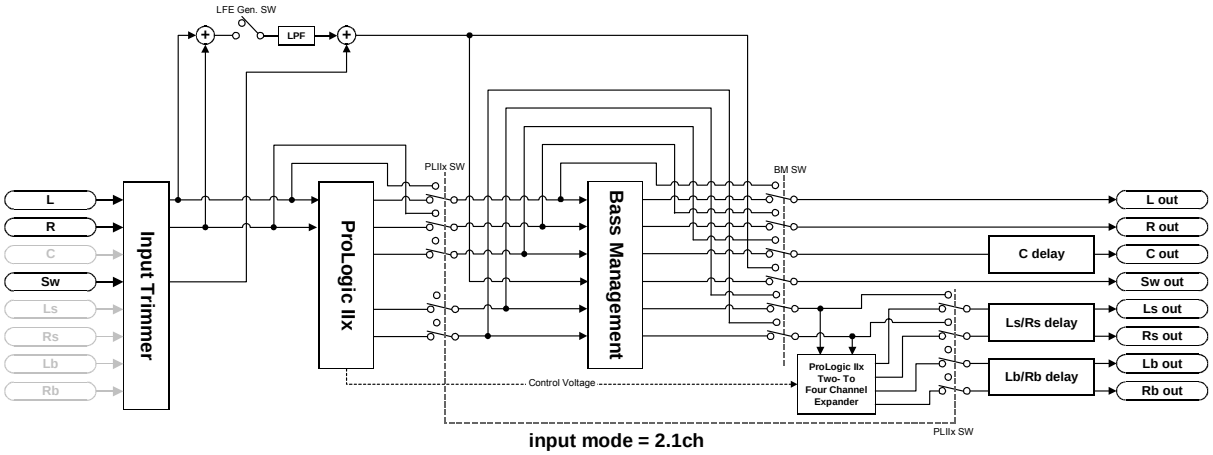
input mode = 5.1ch
DolbyHeadphone enable

Fig. 2.4 NJU26226 Block Diagram (detail)



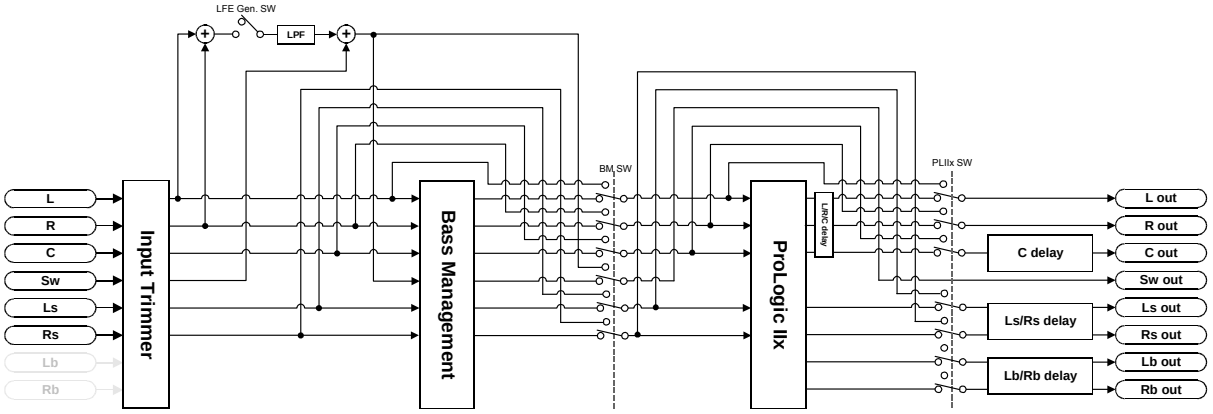
input mode = 7.1ch
DolbyHeadphone enable

Fig. 2.5 NJU26226 Block Diagram (detail)



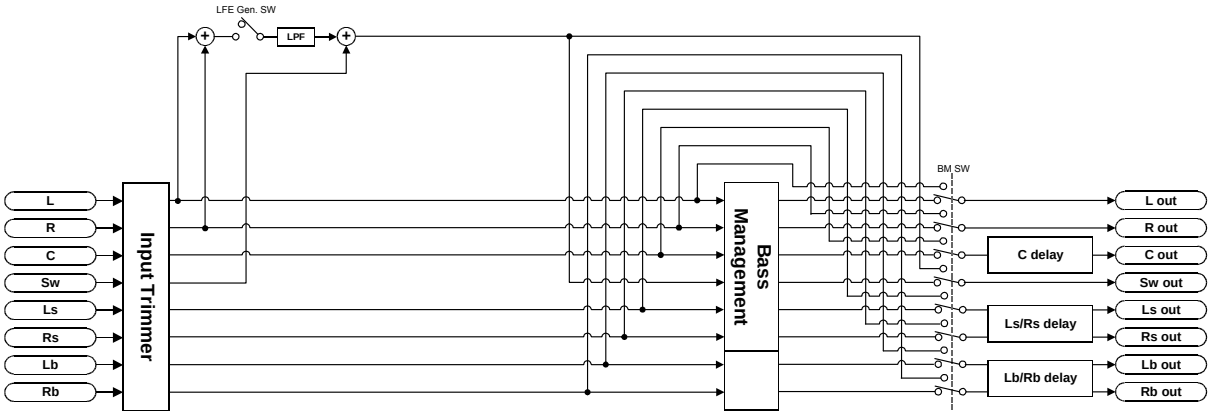
input mode = 2.1ch
Dolby Headphone / Dolby Virtual Speaker disable

Fig. 2.6 NJU26226 Block Diagram (detail)



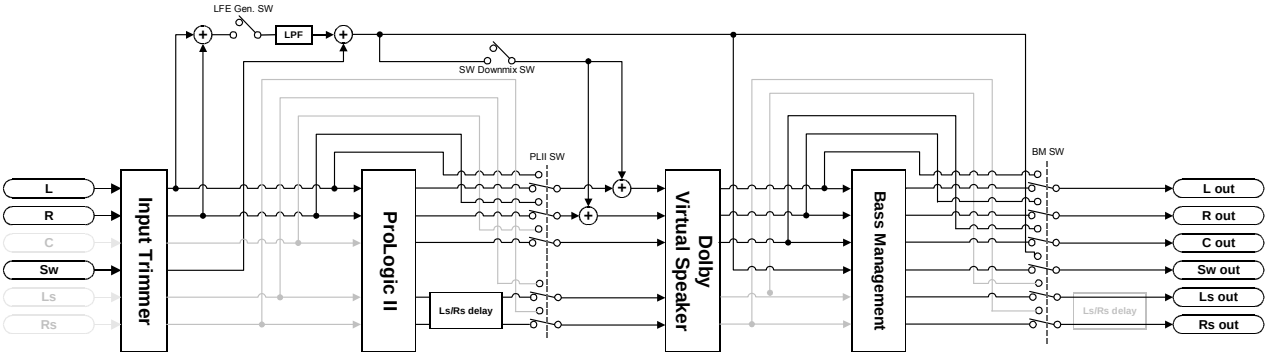
input mode = 5.1ch
Dolby Headphone / Dolby Virtual Speaker disable

Fig. 2.7 NJU26226 Block Diagram (detail)



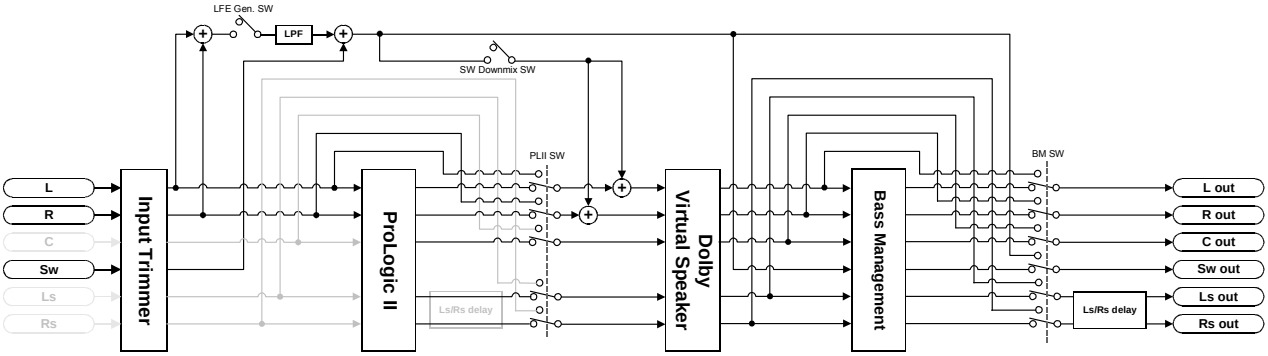
input mode = 7.1ch
Dolby Headphone / Dolby Virtual Speaker disable

Fig. 2.8 NJU26226 Block Diagram (detail)



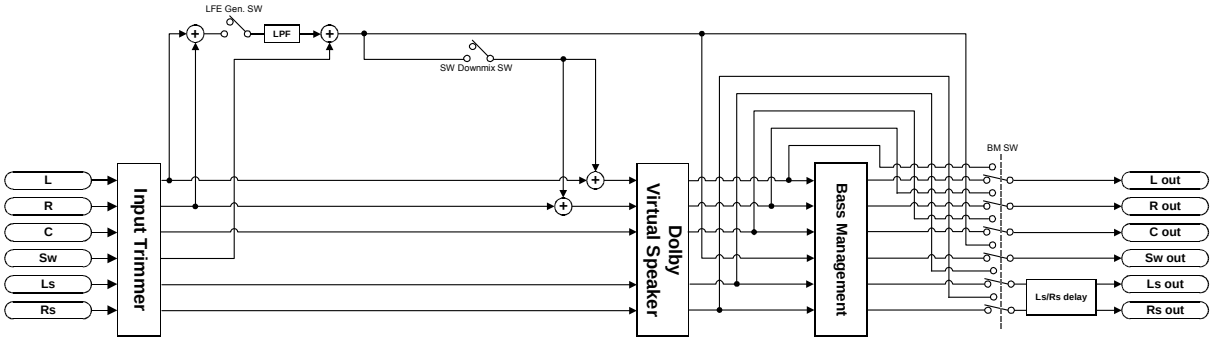
input mode = 2.1ch
Dolby Virtual Speaker enable, 2speaker layout / 3speaker layout

Fig. 2.9 NJU26226 Block Diagram (detail)



input mode = 2.1ch
Dolby Virtual Speaker enable, 4speaker layout / 5speaker layout

Fig. 2.10 NJU26226 Block Diagram (detail)



input mode = 5.1ch
Dolby Virtual Speaker enable

Fig. 2.11 NJU26226 Block Diagram (detail)

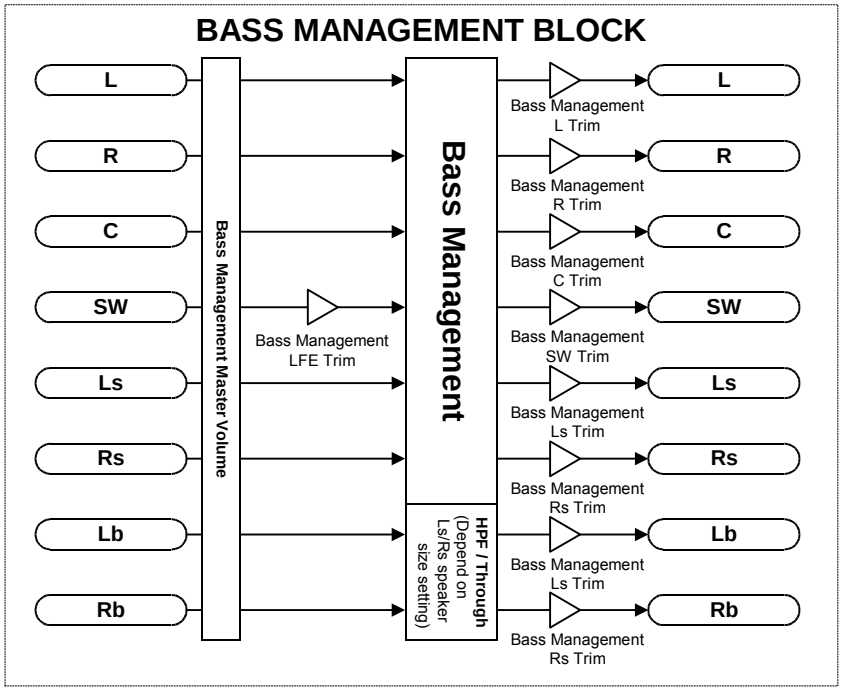


Fig. 2.12 NJU26226 Block Diagram (Bass Management block)

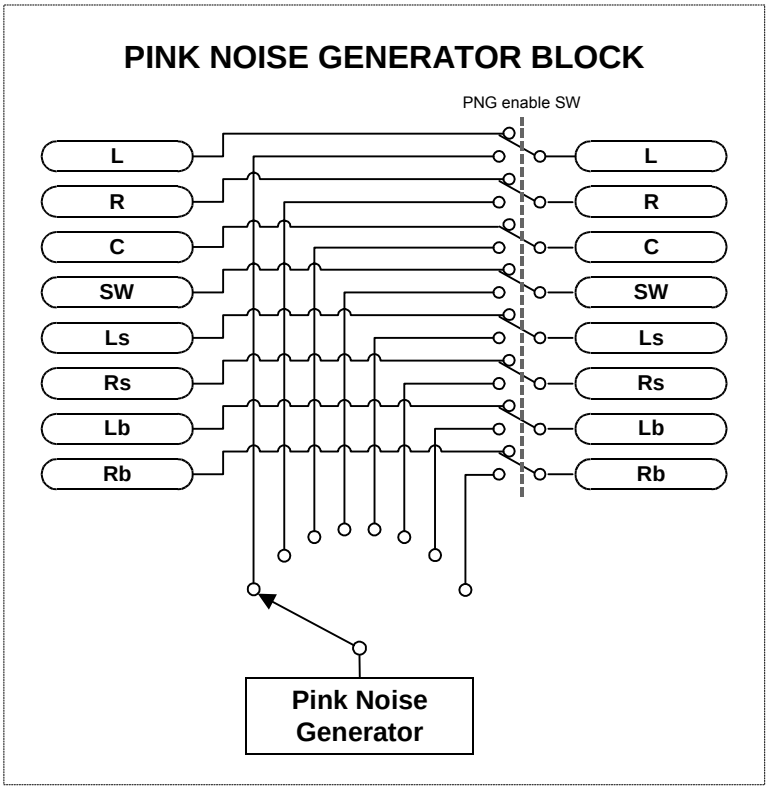


Fig. 2.13 NJU26226 Block Diagram (Pink Noise Generator block)

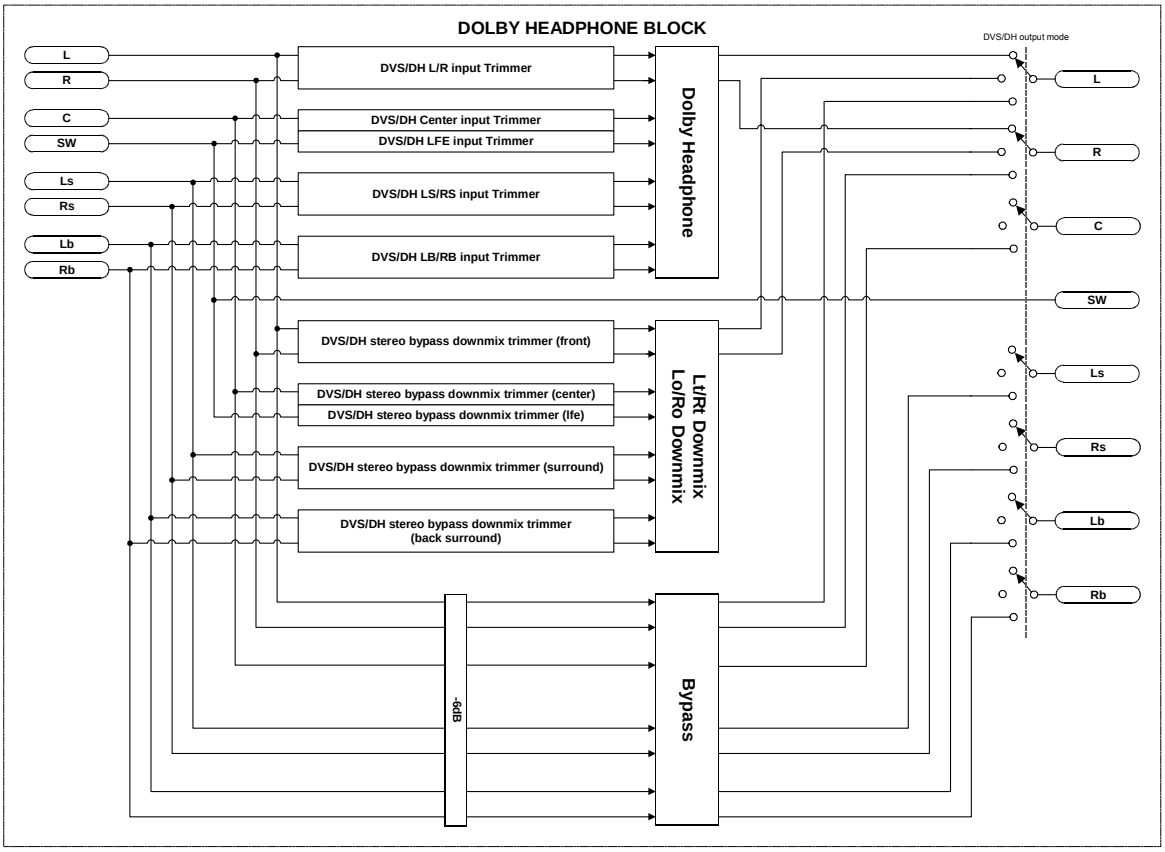


Fig. 2.14 NJU26226 Block Diagram (Dolby Headphone block)

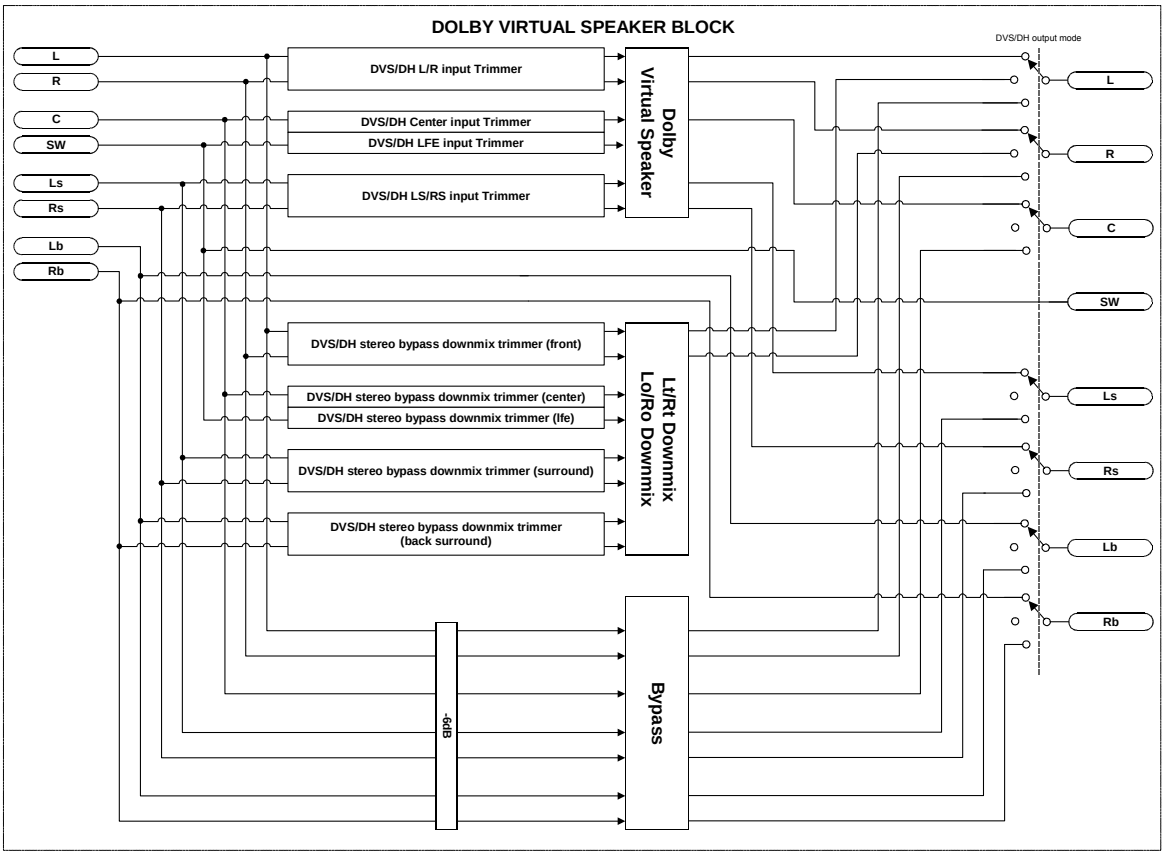


Fig. 2.15 NJU26226 Block Diagram Block Diagram (Dolby Virtual Speaker block)

■ Pin Configuration

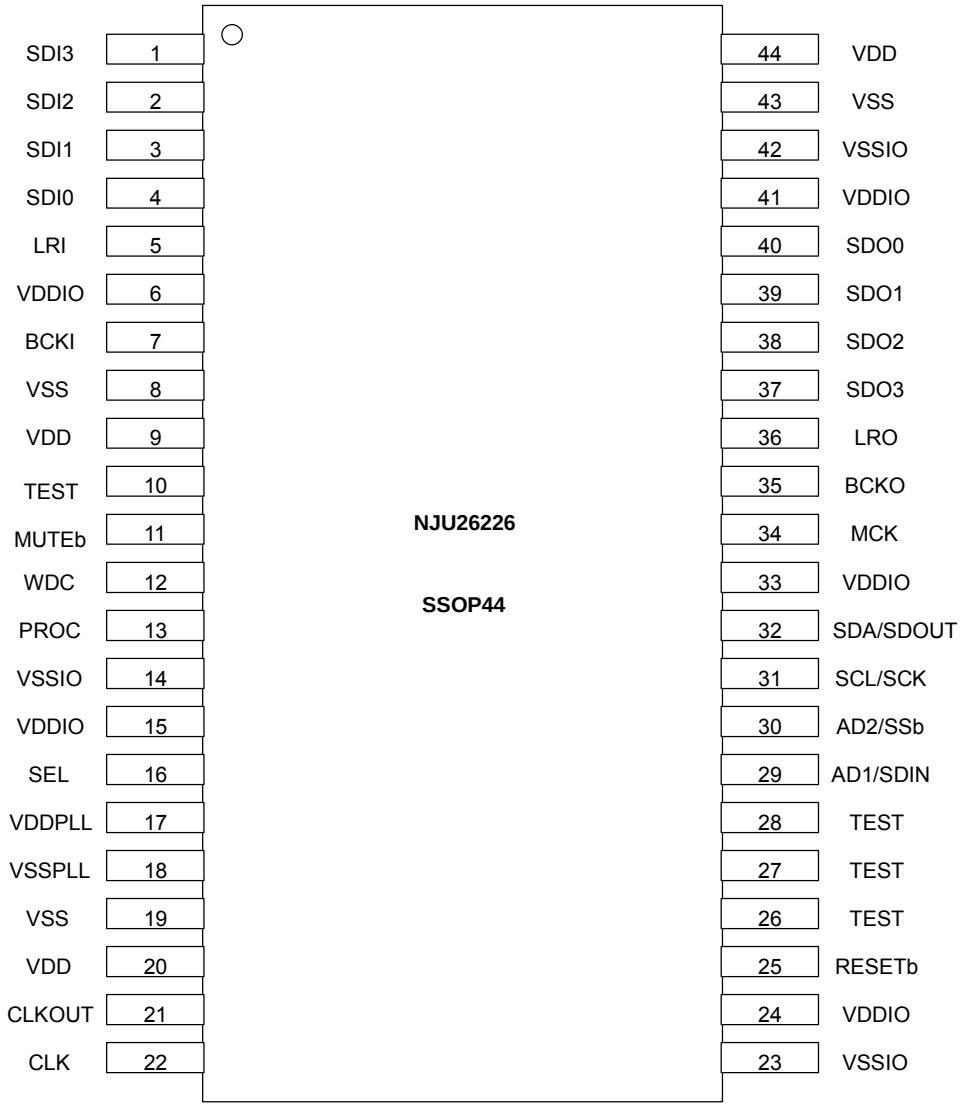


Fig. 3 NJU26226 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Function
1	SDI3	I	Audio Data Input ch.3
2	SDI2	I	Audio Data Input ch.2
3	SDI1	I	Audio Data Input ch.1
4	SDI0	I	Audio Data Input ch.0
5	LRI	I	LR Clock Input
6	VDDIO	-	I/O Power Supply +3.3V
7	BCKI	I	Bit Clock Input
8	VSS	-	DSP Core Power Supply GND
9	VDD	-	DSP Core Power Supply +1.8V
10	TEST *	I	for test connect with VSSIO through 3.3kohm resistance.
11	MUTEb *	I	Master Volume Status after reset '1': 0dB, '0': Mute
12	WDC *	OD	Watchdog Clock output pin (Open drain output)
13	PROC *	I	Signal Processing after reset '1': Normal Processing, '0': Waiting for a Command without Processing
14	VSSIO	-	I/O Power Supply GND
15	VDDIO	-	I/O Power Supply +3.3V
16	SEL	I	Host Interface Selection '1': Serial Interface, '0': I^2C bus
17	VDDPLL	-	PLL Power Supply +1.8V
18	VSSPLL	-	PLL Power Supply GND
19	VSS	-	DSP Core Power Supply GND
20	VDD	-	DSP Core Power Supply +1.8V
21	CLKOUT	O	OSC Clock Output
22	CLK	I	OSC Clock Input (12.288MHz)
23	VSSIO	-	I/O Power Supply GND
24	VDDIO	-	I/O Power Supply +3.3V
25	RESETb	I	Reset (RESETb='0': DSP Reset)
26	TEST	I	for test (connect to VDDIO)
27	TEST	I	for test (connect to VSSIO)
28	TEST	I	for test (connect to VSSIO)
29	AD1/SDIN	I	I^2C Address (I^2C mode) / Serial In (4-wire serial mode)
30	AD2/SSb	I	I^2C Address (I^2C mode) / Serial enable (4-wire serial mode)
31	SCL/SCK	I	I^2C SCL (I^2C mode) / Serial clock (4-wire serial mode)
32	SDA/SDOUT	I/O	I^2C SDA (I^2C mode) / Serial Out (4-wire serial mode)
33	VDDIO	-	I/O Power Supply +3.3V
34	MCK	O	A/D, D/A clock output (buffer output of a CLK pin)
35	BCKO	O	Bit Clock Output
36	LRO	O	LR Clock Output
37	SDO3	O	Audio Data Output ch.3
38	SDO2	O	Audio Data Output ch.2
39	SDO1	O	Audio Data Output ch.1
40	SDO0	O	Audio Data Output ch.0
41	VDDIO	-	I/O Power Supply +3.3V
42	VSSIO	-	I/O Power Supply GND
43	VSS	-	DSP Core Power Supply GND
44	VDD	-	DSP Core Power Supply +1.8V

I : Input

O : Output

OD : Open Drain Output

I/O : Bi-directional

Note: Pins symbol with * : Connect with VDDIO or VSSIO through 3.3kΩ resistance

■ Audio Interface

The NJU26226 audio interface provides industry serial data formats of I^2S, MSB-first Left-justified or MSB-first Right-justified. The NJU26226 audio interface provides four data inputs, SDI0, SDI1, SDI2 and SDI3, and four data outputs, SDO0, SDO1, SDO2 and SDO3, as shown in table 2 and 3.

Table 2 Serial Audio Input Pin

Pin No.	Symbol	Description
4	SDI0	The input signal to L/R, C/Sw, Ls/Rs and Lb/Rb can be selected from SDI0, SDI1, SDI2, and SDI3 (refer to Fig 2.2).
3	SDI1	
4	SDI2	
1	SDI3	

Table 3 Serial Audio Output Pin

Pin No.	Symbol	Description
40	SDO0	L/R, C/Sw, Ls/Rs Lb/Rb, or Mute can be selected (refer to Fig 2.2).
39	SDO1	L/R, C/Sw, Ls/Rs Lb/Rb, or Mute can be selected (refer to Fig 2.2).
38	SDO2	L/R, C/Sw, Ls/Rs Lb/Rb, or Mute can be selected (refer to Fig 2.2).
37	SDO3	L/R, C/Sw, Ls/Rs Lb/Rb, or Mute can be selected (refer to Fig 2.2).

Note: L/R : Front channel
C/Sw : Center channel and Sub woofer
Ls/Rs: Surround channel
Lb/Rb: Surround back channel

■ Host Interface

The NJU26226 can be controlled via Serial Host Interface (SHI) using either of two serial bus formats : I^2C bus or 4-Wire serial bus. Data transfers are in 8 bits packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.
The detail I^2C bus and 4-Wire Serial bus information are described in the 'NJU26200 Series Hardware Data Sheet'.

Table 4 Serial Host Interface Pin Descriptions

Pin No.	Symbol	Setting	Host Interface
16	SEL	Low	I^2C Bus Interface
		High	4-Wire Serial Interface

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C /Serial)	I^2C bus Interface	4-Wire Serial Interface
29	AD1/SDIN	I^2C Address Select Bit1	Serial data input
30	AD2/SSb	I^2C Address Select Bit2	Slave select
31	SCL/SCK	Serial Clock	Serial Clock
32	SDA/SDOUT	Serial Data Input/Output (Open Drain output)	Serial data output (CMOS Output)

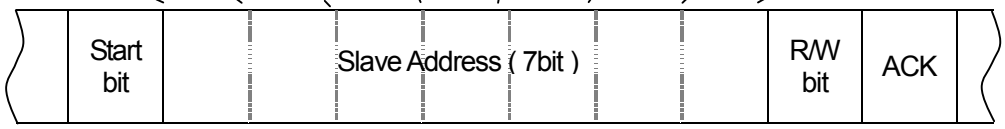
Note: When 4-Wire Serial bus is selected, The SDA/SDOUT pin is CMOS output. The SDOUT pin does not require a pull-up resistance.
When I^2C Bus is selected, this pin is a bi-directional Open Drain output. This pin, which is assigned for I^2C Bus, requires a pull-up resistance.
The SDA/SDOUT pin isn't 5.0V Input tolerant. Please note the voltage level (Max voltage is V_{DDIO}).

■ I²C Bus

When the NJU26226 is configured for I²C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6)

Table 6 I²C-Bus Interface Slave address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

Note: The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer. Moreover, after sending S ("START" condition), Sr (repeated "START" condition) is not received but it becomes the waiting for the P ("STOP" condition). Therefore, please be sure to send P ("STOP" condition).

■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. The SDOUT pin is always CMOS output. This pin does not require a pull-up resistance.

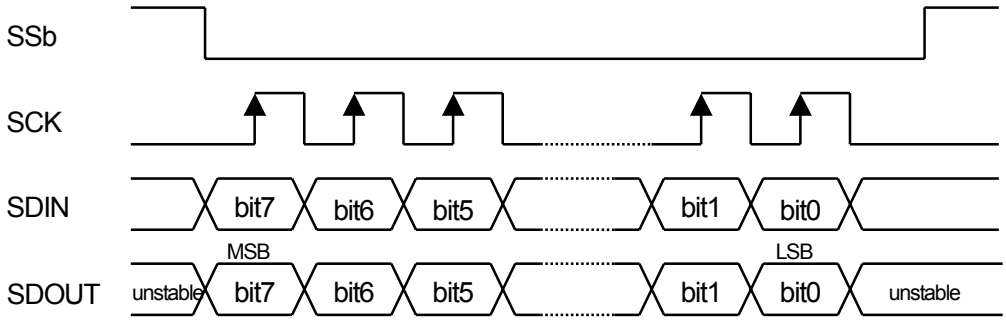


Fig. 4 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High".

When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.

After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High".

■ Pin setting

The NJU26226 operates default command setting after resetting the NJU26226. In addition, the NJU26226 restricts operation at power on by setting PROC pin and MUTEb pin (Table 7). These pins are input pin. However, these pins operate as bi-directional pins. Connect with V_{DDIO} or V_{SSIO} through 3.3kΩ resistance.

Table 7 Pin setting

Pin No.	Symbol	Setting	Function
13	PROC	"High"	The NJU26226 operates default setting after reset.
		"Low"	The NJU26226 does not operate after reset. Sending start command is required for starting operation.
11	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26226 outputs clock pulse through WDC (Pin No.8) during normal operation. The WDC clock is useful to check the status of the NJU26226 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26226. When the WDC clock pulse is lost or not normal clock cycle, the NJU26226 does not operate correctly. Then reset the NJU26226 and set up the NJU26226 again. The WDC clock is able to be variable for 10ms to 640ms by command. Default setting of WDC clock is 200ms.

The WDC pin is open drain output. The WDC pin setting (Table 8)

Table 8 WDC pin setting

Pin No.	Symbol	Setting	
12	WDC	WDC pin is used.	Connect with V_{DDIO} through 3.3kΩ resistance
		WDC pin is not used.	Connect with V_{SSIO} through 3.3kΩ resistance. Do not open WDC pin.

Note: The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing.
In slave mode, when there is no input of BCKI/LRI, the WDC pin can't output.
It is required to set up a sampling rate correctly.

■ Firmware Command Table

Table 9 NJU26226 Command

No.	Command
1	SET_TASK_CMD
2	PRO2MODE_CMD
3	PRO2CDCFG_CMD
4	PRO2FLAGS_CMD
5	DVS_DH_CMD
6	BM_CONFIG_CMD
7	SAMPLERATE_CMD
8	PNG_MODE_CMD
9	DELAY_CMD
10	GAIN_CMD
11	SYSTEM_STATE_CMD
12	WATCHDOG_CMD
13	SMOOTH_CMD
14	INPUT_SEL_CMD
15	OUTPUT_SEL_CMD
16	REINIT_CMD
17	SOFTWARE_RESET_CMD
18	START_CMD
19	NOP_CMD

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (Dolby) is required.

■ License Information

The Word “DOLBY”, “Pro Logic” and the double D mark are trademarks of Dolby Laboratories.
The NJU26226 can only be delivered to licensees of Dolby Laboratories.
Please refer to the licensing application manual issued by Dolby Laboratories.

[CAUTION]
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