



SRS WOW HD Processor

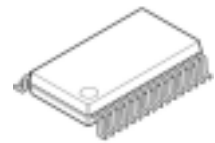
■ General Description

The NJU26040-09B is a digital audio signal processor that provides the function WOW HD (function limited edition of NJU29040-09A).

The NJU26040-09B processes a lot of sound sources, such as DVD, CD, AM/FM radio, and TV sound into spacious sound of natural virtual surround by WOW HD.

The applications of NJU26040-09B are suitable for stereo outputs products such as DVD Receivers, AV Amplifiers, TV, radio-cassettes player or ordinary audio products such as small speakers system.

Package



NJU26040V

■ FEATURES

- Software

- WOW HD technology is offered to the stereo I/O product.
- LFE by SRS TruBass-II technology
- SRS FOCUS technology
- SRS Definition technology improves the perception of clarity and acoustic space

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max.
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Power Supply : 3.3V (Input : 5V tolerant)
- Package : SSOP32-R1 (Pb-Free)
- Micro computer interface : I²C bus (standard-mode/100kbps, fast-mode/400kbps),
4-Wire Serial Bus (4-Wire: clock, enable, input data, output data)

The detail hardware specification is described in the “ NJU26040 Hardware Data Sheet”.

NJU26040-09B

■ DSP Block Diagram

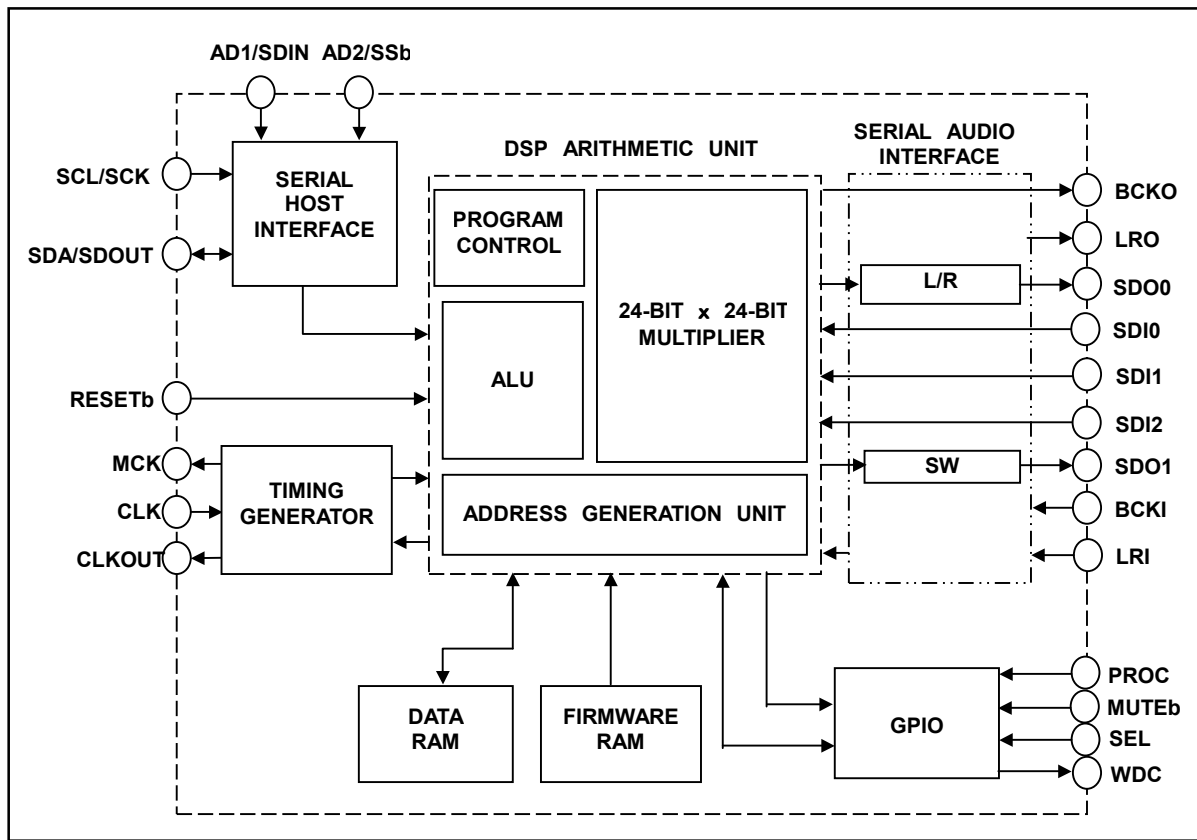


Fig.1 NJU26040-09B Block Diagram

■ WOW HD Decoder

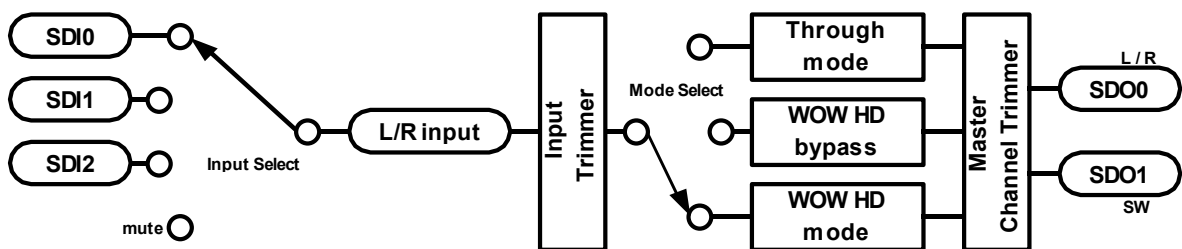
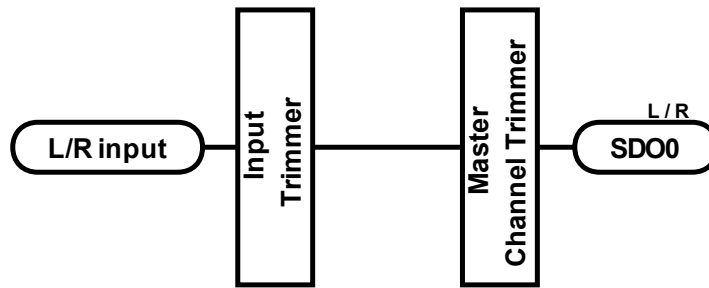
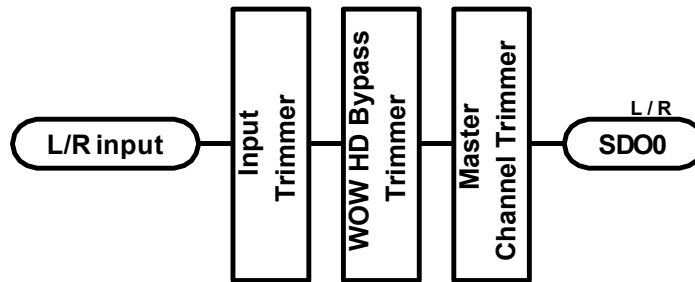


Fig.2-1 NJU26040-09B Top Level Function Diagram



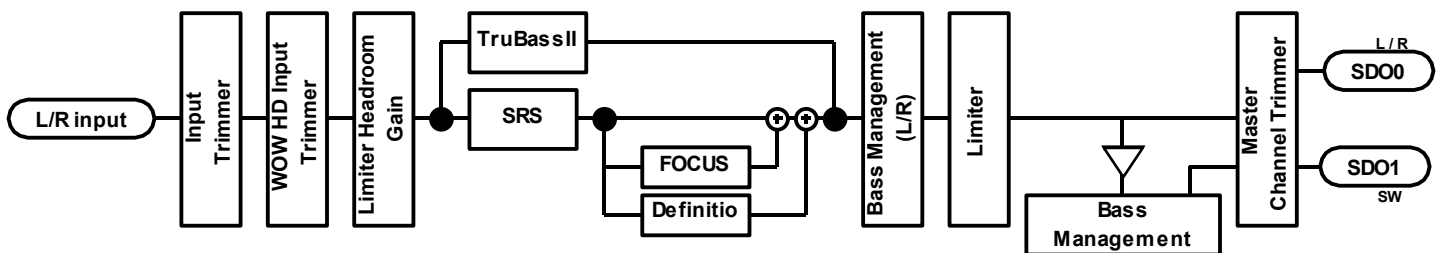
Through mode Block Diagram

Fig.2-2 NJU26040-09B Function Diagram



WOW HD Bypass mode Block Diagram

Fig.2-3 NJU26040-09B Function Diagram



WOW HD Mode Block Diagram

Fig.2-4 NJU26040-09B Function Diagram

NJU26040-09B

■ Pin Configuration

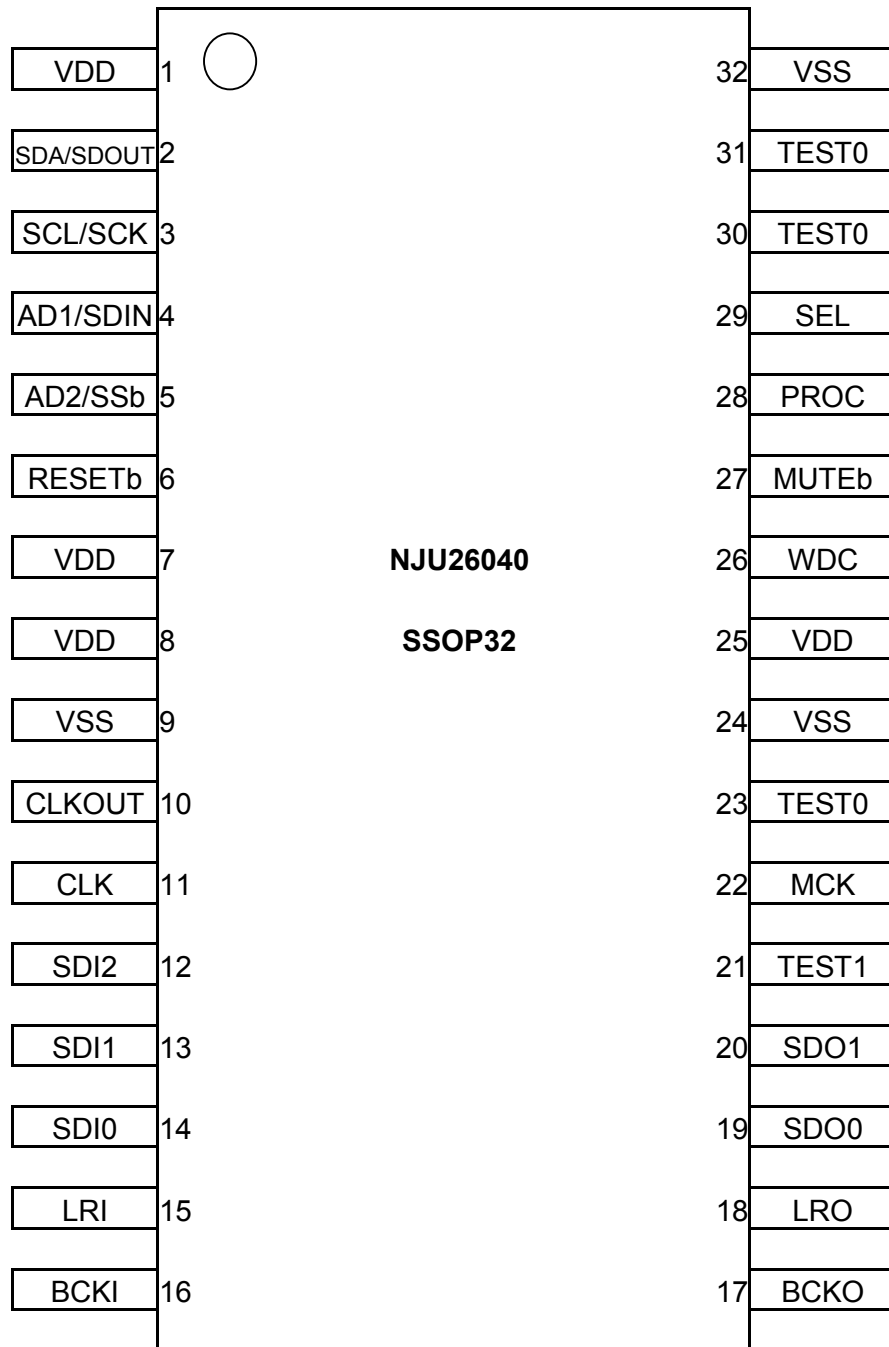


Fig.3 NJU26040 Pin Configuration

■ Pin Description

Table 1. Pin Description

Pin No.	Symbol	I/O	Description
1, 7, 8, 25	VDD	-	Power Supply +3.3V
2	SDA/SDOUT	OD	I ² C I/O / 4-Wire Serial Output This pin requires a pull-up resistance in both I ² C bus and 4-Wire serial mode.
3	SCL/SCK	I	I ² C clock / Serial clock
4	AD1/SDIN	I	I ² C Address / Serial In
5	AD2/SSb	I	I ² C Address / Serial Enable
6	RESETb	I	Reset (RESETb='Low' : DSP Reset)
9, 24, 32	VSS	-	GND
10	CLKOUT	O	OSC Output
11	CLK	I	OSC Clock Input
12	SDI2	I	Audio Data Input 2 (L/R)
13	SDI1	I	Audio Data Input 1 (L/R)
14	SDI0	I	Audio Data Input 0 (L/R)
15	LRI	I	LR Clock Input
16	BCKI	I	Bit Clock Input
17	BCKO	O	Bit clock Output
18	LRO	O	LR clock Output
19	SDO0	O	Audio Data Output 0 (L/R)
20	SDO1	O	Audio Data Output 1 (SW)
21	TEST1	O	for Test (Non connect)
22	MCK	O	Master Clock Output for A/D, D/A
23, 30, 31	TEST0	I-	for Test (connected to VSS)
26	WDC	OD	Watchdog clock output (open drain output)
27	MUTEb	I	Master Volume level, After Reset DSP ("1" : 0dB "0" : Mute)
28	PROC	I	After Reset DSP. ("1" : Normal "0" : Wait from Command)
29	SEL	I	Select I ² C or Serial bus ('1' : Serial / '0' : I ² C-Bus)

Note : I : Input
 I - : Input (Pull-down)
 O : Output
 OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.
 I/O+ : Bi-directional (with Pull-up resistance)
 I/O - : Bi-directional (with Pull-down resistance)

NJU26040-09B

■ Digital Audio Interface

The NJU26040-09B audio interface provides industry standard serial data formats of I²S, MSB-first left-justified or MSB-first right-justified. The NJU26040-09B audio interface provides three data input, SDI0, SDI1, SDI2 and three data outputs, SDO0, SDO1 as shown in table 2, table 3 and Fig.1. An audio interface input and output data format become the same data format.

Table 2. Serial Audio Input Pin

Pin No.	Symbol	Description
14	SDI0	Audio Data Input 0 L / R
13	SDI1	Audio Data Input 1 L / R
12	SDI2	Audio Data Input 2 L / R

Table 3. Serial Audio Output Pin

Pin No.	Symbol	Description
19	SDO0	Audio Data Output 0 L / R
20	SDO1	Audio Data Output 1 C / SW

■ Host Interface

The NJU26040-09B can be controlled via Serial Host Interface (SHI) using either of two serial bus formats: I²C bus or 4-Wire serial bus.(Table 4) Data transfers are in 8 bit packets (1 byte) when using either format.

Serial Host Interface Pin Description.(Table 5)

Table 4. Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
29	SEL	"Low"	I ² C bus
		"High"	4-Wire serial bus

Table 5. Serial Host Interface Pin Description

Pin No.	Symbol (I ² C bus / Serial)	I ² C bus Format	4-Wire Serial bus Format
2	SDA / SDOUT *	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (Open-Drain Output)
3	SCL / SCK *	Serial Clock	Serial Clock
4	AD1 / SDIN *	I ² C bus address Bit1	Serial Data Input
5	AD2 / SSb *	I ² C bus address Bit2	Serial enable

Note : SDA /SDOUT pin is a bi-directional open drain.

This pin requires a pull-up resistance in both I²C bus and 4-Wire serial mode.

* When the power supply (V_{DD}= +3.3V) is supplied to NJU26040, these pins become +5.0V Input tolerant.

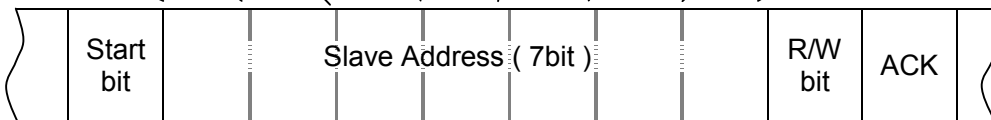
■ I²C bus

When the NJU26040-09B is configured for I²C bus communication during the Reset initialization sequence. I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26040-09B. An address can be arbitrarily set up by the AD1 and AD2 pins. The I²C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

Table 6. I²C bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is “Low”. SLAVE address is 1 when AD1/2 is “High”.

Note : In case of the NJU26040-09B only single-byte transmission is available. The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” I²C bus data transfer.

■ 4-Wire Serial Interface

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb=0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = “High”. SDOUT is Open-drain output in case of SSb = “Low”. SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

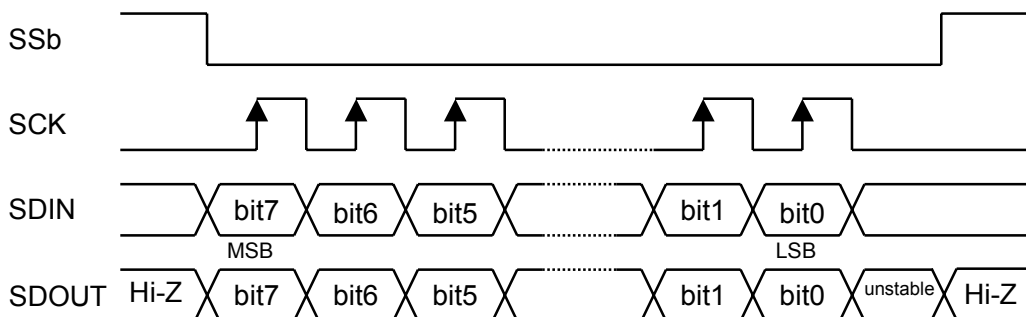


Fig. 4 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb=“High”. When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes “High”.

■ Pin setting

The NJU26040-09B operates default command setting after resetting the NJU26040-09B. In addition, the NJU26040-09B restricts operation at power on by setting PROC pin and MUTEb pin (Table 7). These pins are input pin. However, these pins operate as bi-directional pins. Connect with VDD or VSS through 3.3kΩ resistance.

Table 7. Pin setting

Pin No.	Symbol	Setting	Function
28	PROC	“High”	The NJU26040-09A operates default setting after reset.
		“Low”	The NJU26040-09A does not operate after reset. Sending start command is required for starting operation.
27	MUTEb	“High”	Master volume is set 0dB after reset.
		“Low”	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26040-09B outputs clock pulse through WDC (No.26) pin during normal operation. (Table 8)

Table 8. WatchDog Clock Output Cycle

WDC Output Cycle (Low/High) Time
85ms

The NJU26040-09B generates a clock pulse through the WDC terminal after resetting the NJU26040-09B. The WDC clock is useful to check the status of the NJU26040-09B operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26040-09B. When the WDC clock pulse is lost or not normal clock cycle, the NJU26040-09B does not operate correctly. Then reset the NJU26040-09B and set up the NJU26040-09B again.

Note : If input and output of an audio signal stop and an audio interface stops, WDC can't output. That is because it has controlled based on the signal of an audio interface.

■ NJU26040-09A Command Table


Table 9. NJU26040-09A Command

No.	Command
1	SET_TASK_CMD
2	AUDIO_FORMAT_CMD
3	SYSTEM_STATE_CMD
4	SAMPRATE_CMD
5	INPUT_SELECT_CMD
6	WOWHD_OUTPUT_MODE_CMD
7	DF_SELECT_CMD
8	TB2_SETUP_CMD
9	SW_CROSSOVER_FREQ_CMD
10	SRS3D_SETUP_CMD
11	INPUT_TRIM_CMD
12	MASTER_TRIM_CMD
13	LEFT_TRIM_CMD
14	RIGHT_TRIM_CMD

No.	Command
15	SUBWOOFER_TRIM_CMD
16	WOWHD_INPUT_TRIM_CMD
17	WOWHD_BYPASS_TRIM_CMD
18	FC_CNTRL_CMD
19	TB2_FRONT_CNTRL_CMD
20	TB2_LFE_CNTRL_CMD
21	DF_FRONT_CNTRL_CMD
22	SRS3D_SPACE_CNTRL_CMD
23	SRS3D_CENTER_CNTRL_CMD
24	LIMITER_CMD
25	SOFT_RESET_CMD
26	WDC_TEST_CMD
27	START_CMD

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (SRS Labs. Inc.) is required.

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