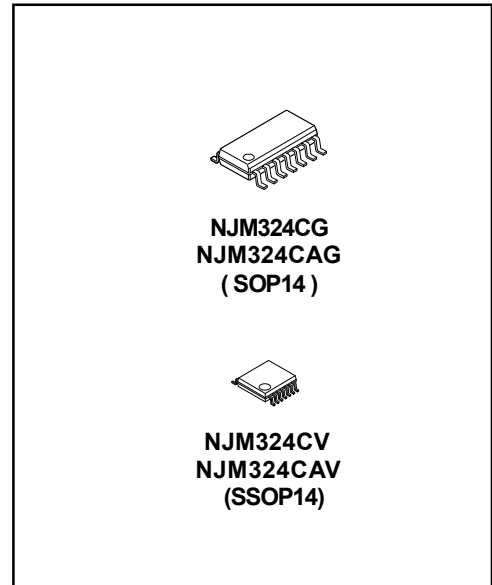


## Low power quad operational amplifiers

### Features

- Wide gain bandwidth: 1.3MHz typ.
- Input common-mode voltage range includes ground
- Large voltage gain: 100dB typ.
- Very low supply current per amplifier: 300uA typ.
- Low input bias current: 20nA typ.
- Low input offset current: 2nA typ.
- Wide power supply range:
  - Single supply: +3V to +30V
  - Dual supplies:  $\pm 1.5V$  to  $\pm 15V$
- Internal ESD protection: Human body model (HBM)  $\pm 2000V$  typ.
- Input Offset Voltage Grade

NJM324C ( Normal-Grade )	NJM324CA ( A Grade )
7mV max. at Ta=25°C	2.5mV max. at Ta=25°C
9mV max. at Ta=0 to 70°C	4mV max. at Ta=0 to 70°C

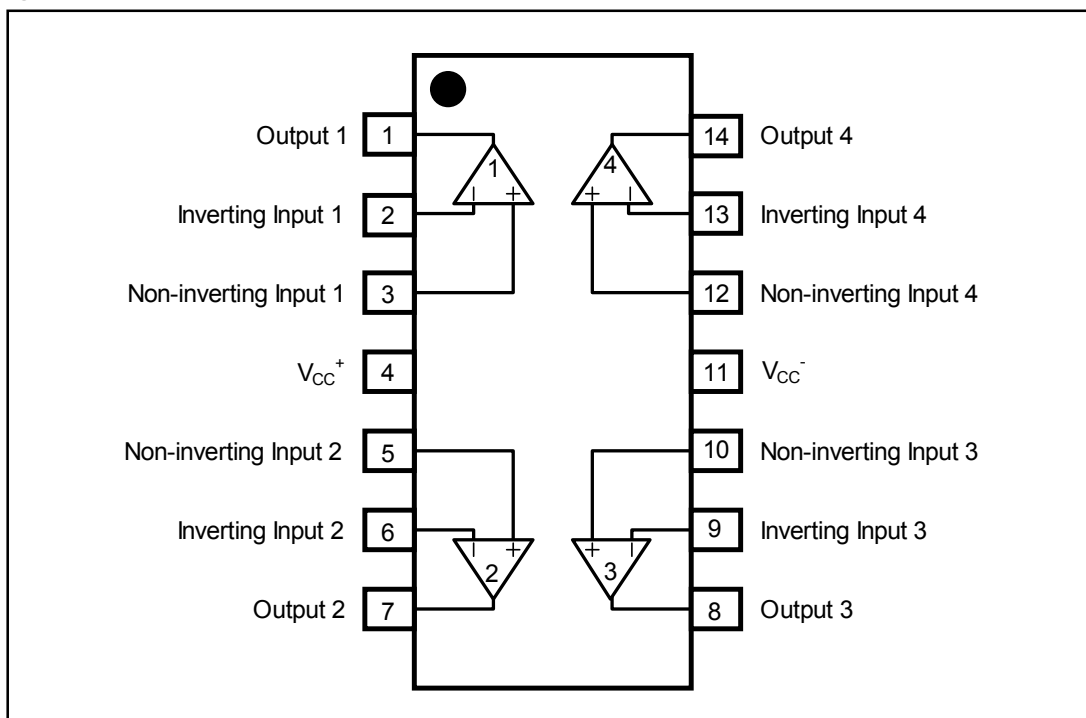


### Description

The NJM324C / NJM324CA consist of four independent, high gain, internally frequency-compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

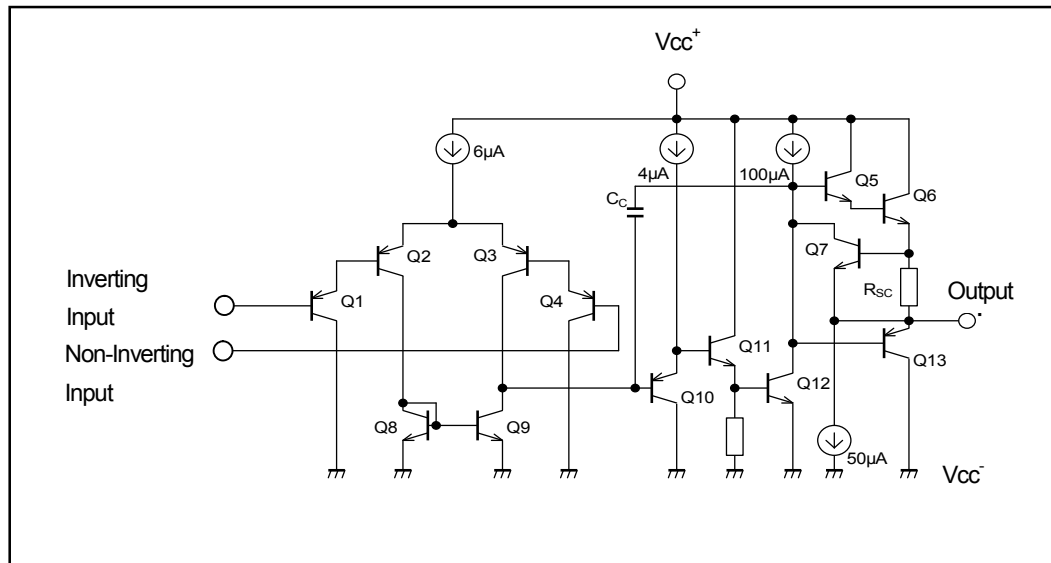
### 1. Pin and schematic diagram

Figure 1. Pin connections (top view)



# NJM324C/NJM324CA

Figure 2. Schematic diagram (1/4 NJM324C / NJM324CA)



## 2 Absolute maximum ratings

Table1. Absolute maximum ratings

(Tamb=25°C)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage (V <sub>CC</sub> <sup>+</sup> - V <sub>CC</sub> <sup>-</sup> )	32	V
V <sub>IN</sub>	Input voltage <sup>(1)</sup>	V <sub>CC</sub> <sup>-</sup> - 0.3 to V <sub>CC</sub> <sup>+</sup> + 32	V
V <sub>O</sub>	Output Terminal Input Voltage	V <sub>CC</sub> <sup>-</sup> - 0.3 to V <sub>CC</sub> <sup>+</sup> + 0.3	V
V <sub>ID</sub>	Differential input voltage	±32	V
I <sub>IN</sub>	Input current <sup>(2)</sup> : Vin driven negative Input current <sup>(3)</sup> : Vin driven positive above AMR value	5mA in DC or 50mA in AC (duty cycle = 10%, T=1s) 0.4	mA
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C
T <sub>j</sub>	Maximum junction temperature	150	°C
P <sub>D</sub>	Power Dissipation	SOP14 : 880 <sup>(5)</sup> 1200 <sup>(6)</sup> SSOP14 : 510 <sup>(5)</sup> 640 <sup>(6)</sup>	mW
θ <sub>ja</sub>	Thermal resistance junction to ambient <sup>(4)</sup>	SOP14 : 140 <sup>(5)</sup> 100 <sup>(6)</sup> SSOP14 : 245 <sup>(5)</sup> 195 <sup>(6)</sup>	°C/W
ψ <sub>jt</sub>	Thermal resistance junction to top surface of IC package <sup>(4)</sup>	SOP14 : 40 <sup>(5)</sup> 35 <sup>(6)</sup> SSOP14 : 49 <sup>(5)</sup> 47 <sup>(6)</sup>	°C/W

1. Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V<sub>CC</sub><sup>+</sup>

2. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V<sub>CC</sub> voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.

3. The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400µA max (R= (Vin-32V)/400µA).

4. Short-circuit can cause excessive heating and destructive dissipation. Values are typical.

5. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting

6. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4) mounting

### 3. Operating conditions

Table2. Operating conditions

(T<sub>amb</sub>=25°C)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage (V <sub>CC</sub> <sup>+</sup> - V <sub>CC</sub> <sup>-</sup> )	3 to 30	V
T <sub>oper</sub>	Operating free-air temperature range	-40 to +85	°C

### Electrical characteristics

Table3. V<sub>CC</sub><sup>+</sup> = +5V, V<sub>CC</sub><sup>-</sup> = 0V, T<sub>amb</sub> = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>io</sub>	Input offset voltage <sup>(1)</sup> T <sub>amb</sub> = 25°C	-	0.5	7	mV
	NJM324CA	-	0.5	2.5	
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	-	-	9	
	NJM324CA	-	-	4	
I <sub>io</sub>	Input offset current T <sub>amb</sub> = 25°C	-	2	30	nA
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	-	-	100	
I <sub>ib</sub>	Input bias current <sup>(2)</sup> T <sub>amb</sub> = 25°C	-	20	150	nA
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	-	-	300	
A <sub>vd</sub>	Large signal voltage gain (V <sub>CC</sub> <sup>+</sup> = +15V, R <sub>L</sub> =2kΩ, V <sub>o</sub> =1.4V to 11.4V) T <sub>amb</sub> = 25°C	50	100	-	V/mV
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	25	-	-	
SVR	Supply voltage rejection ratio (R <sub>s</sub> <10kΩ, V <sub>CC</sub> <sup>+</sup> = 5V to 30V) T <sub>amb</sub> = 25°C	65	110	-	dB
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	65	-	-	
I <sub>CC</sub>	Supply current, all amp, no load T <sub>amb</sub> = 25°C	-	1.2	2	mA
	V <sub>CC</sub> <sup>+</sup> = 5V	-	1.7	3	
	V <sub>CC</sub> <sup>+</sup> = 30V	-	-	2	
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	-	-	3	
V <sub>icm</sub>	Input common mode voltage range <sup>(3)</sup> (V <sub>CC</sub> <sup>+</sup> = +30V) T <sub>amb</sub> = 25°C	0	-	V <sub>CC</sub> <sup>+</sup> - 1.5	V
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	0	-	V <sub>CC</sub> <sup>+</sup> - 2	
CMR	Common mode rejection ratio (R <sub>S</sub> < 10kΩ) T <sub>amb</sub> = 25°C	70	100	-	dB
	0°C < T <sub>amb</sub> < 70°C <sup>(5)</sup>	60	-	-	
I <sub>source</sub>	Output current source V <sub>CC</sub> <sup>+</sup> = 15V, V <sub>O</sub> = +2V, V <sub>id</sub> = +1V	20	40	-	mA

# NJM324C/NJM324CA

**Table4.  $V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25^\circ C$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{sink}$	Output sink current $V_{CC}^+ = 15V, V_o = +2V, V_{id} = -1V$	10	20	-	mA
	$V_{CC}^+ = 15V, V_o = +0.2V, V_{id} = -1V$	12	50	-	$\mu A$
$V_{OH}$	High level output voltage $T_{amb} = 25^\circ C$ $V_{CC}^+ = 30V, R_L = 2k\Omega$	26	27	-	V
	$V_{CC}^+ = 30V, R_L = 10k\Omega$	27	28	-	
	$V_{CC}^+ = 5V, R_L = 2k\Omega$ $0^\circ C < T_{amb} < 70^\circ C$ <sup>(5)</sup>	3.5	-	-	
	$V_{CC}^+ = 30V, R_L = 2k\Omega$	26	-	-	
	$V_{CC}^+ = 30V, R_L = 10k\Omega$ $V_{CC}^+ = 5V, R_L = 2k\Omega$	27 3	- -	- -	
$V_{OL}$	Low level output voltage ( $R_L = 10k\Omega$ ) $T_{amb} = 25^\circ C$	-	5	20	mV
	$0^\circ C < T_{amb} < 70^\circ C$ <sup>(5)</sup>	-	-	20	
SR	Slew rate $V_{CC}^+ = 15V, V_i = 0.5$ to $3V, R_L = 2k\Omega,$ $C_L = 100pF$ , unity gain	-	0.6	-	V/ $\mu s$
GBP	Gain bandwidth product $V_{CC}^+ = 30V, f = 100kHz, V_{in} = 10mV,$ $R_L = 2k\Omega, C_L = 100pF$	-	1.3	-	MHz
THD	Total harmonic distortion $f = 1kHz, A_v = 20dB, R_L = 2k\Omega, V_o = 2V_{pp},$ $C_L = 100pF, V_{CC}^+ = 30V$	-	0.015	-	%
$e_n$	Equivalent input noise voltage $f = 1kHz, R_s = 100\Omega, V_{CC}^+ = 30V$	-	30	-	nV/ $\sqrt{Hz}$
$DV_{io}$	Input offset voltage drift $0^\circ C < T_{amb} < 70^\circ C$ <sup>(5)</sup>	-	7	30	$\mu V/^\circ C$
$DI_{io}$	Input offset current drift $0^\circ C < T_{amb} < 70^\circ C$ <sup>(5)</sup>	-	10	200	pA/ $^\circ C$
$V_{O1}/V_{O2}$	Channel separation <sup>(4)</sup> $1kHz < f < 20kHz$	-	120	-	dB

1.  $V_o = 1.4V, R_s = 0\Omega, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V.$

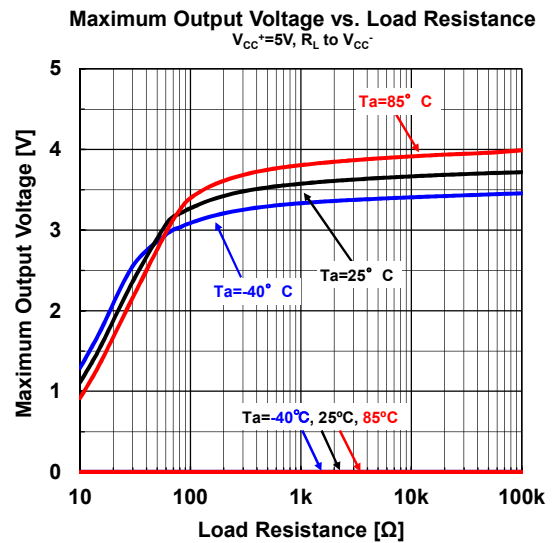
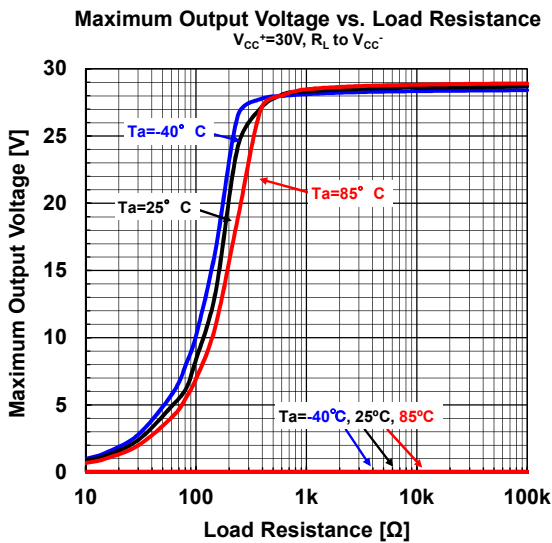
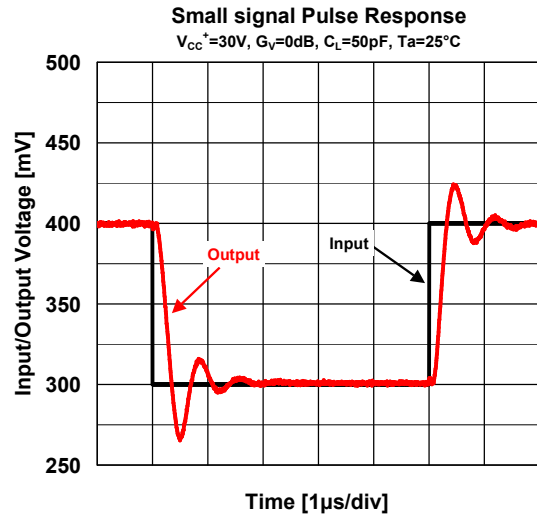
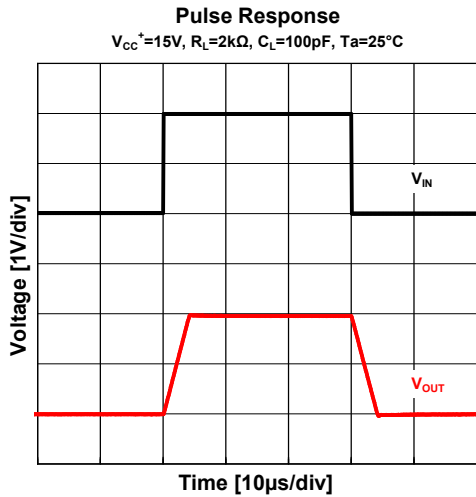
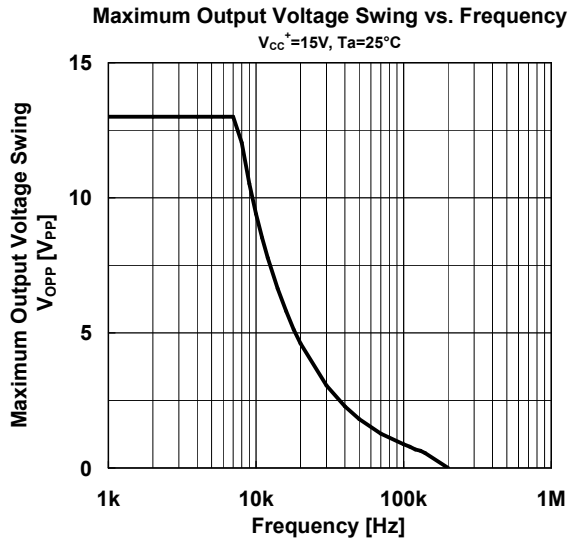
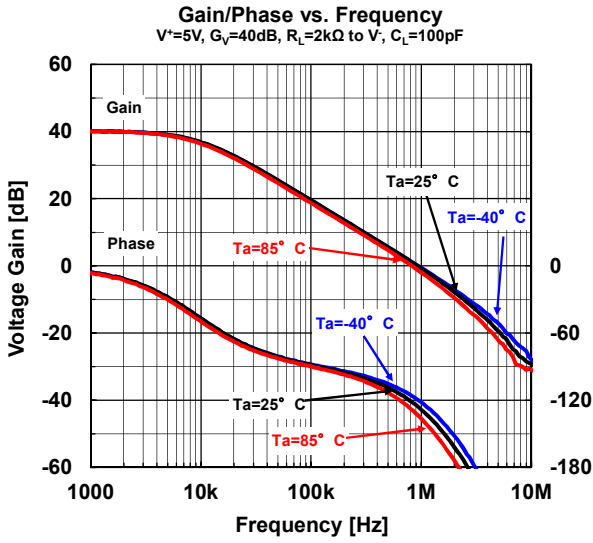
2. The direction of the input current is out of the IC.

3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is  $V_{CC}^+ - 1.5V$ , but either or both inputs can go to +32V without damage.

4. Due to the proximity of the external components, ensure that stray capacitance between these external parts does not cause coupling. Coupling can be detected because this type of capacitance increases at higher frequencies.

5. This parameter is not 100% test.

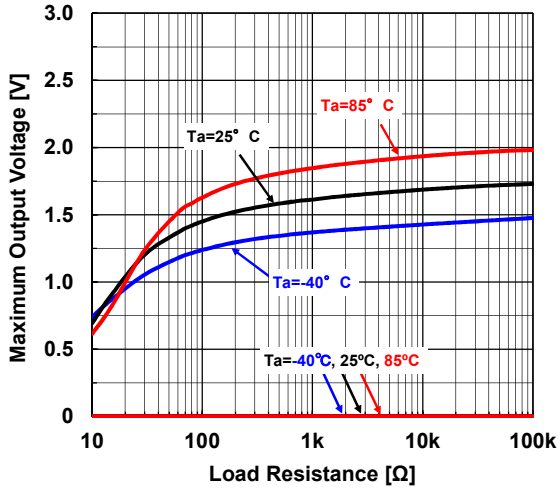
## TYPICAL CHARACTERISTICS



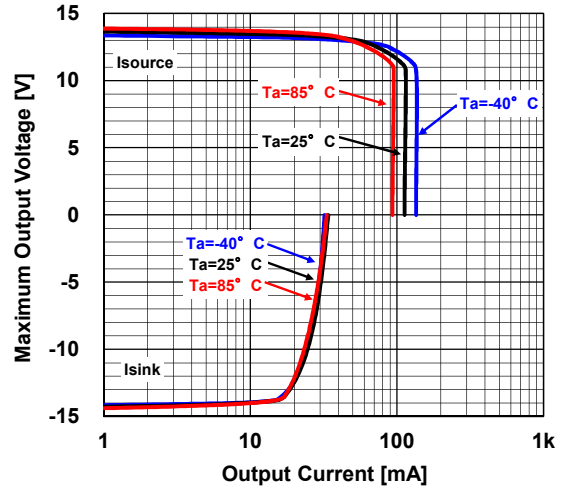
# NJM324C/NJM324CA

## ■ TYPICAL CHARACTERISTICS

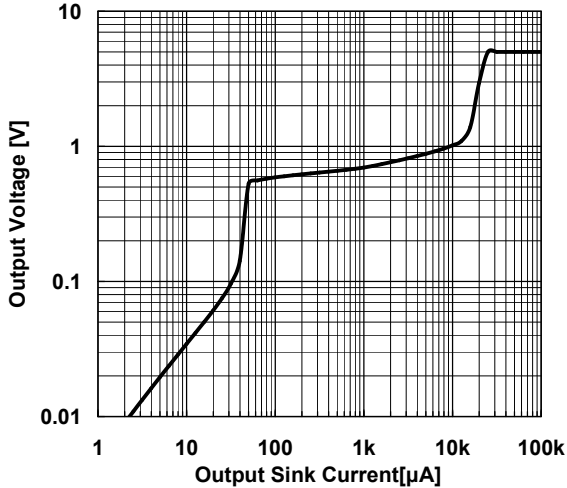
Maximum Output Voltage vs. Load Resistance  
 $V_{CC}^+ = 3V, R_L \text{ to } V_{CC}^-$



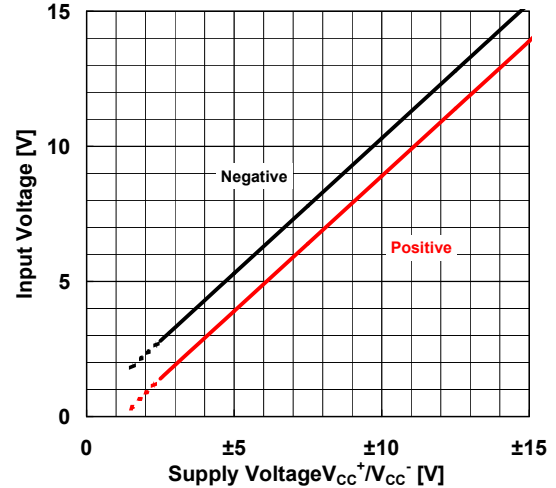
Maximum Output Voltage vs. Output Current  
 $V_{CC}^+/V_{CC}^- = \pm 15V$



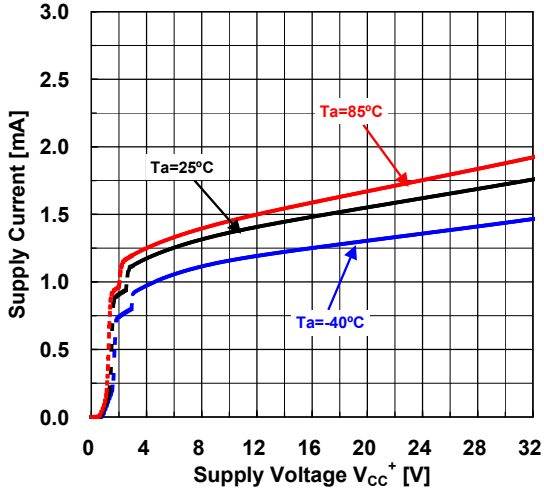
Output Voltage vs. Output Sink Current  
 $V_{CC}^+ = 5V, T_a = 25^\circ C$



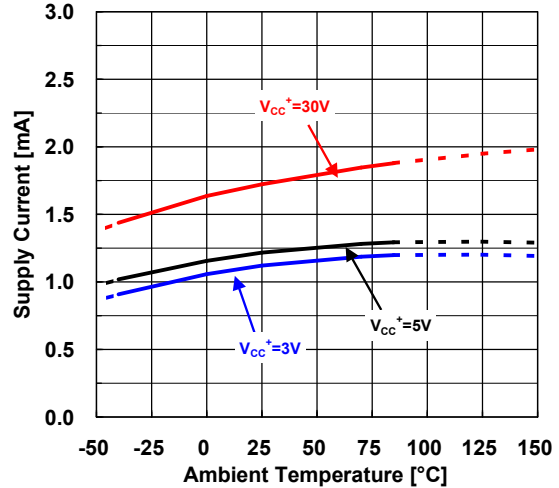
Input Voltage Range vs. Supply Voltage  
 $T_a = 25^\circ C$



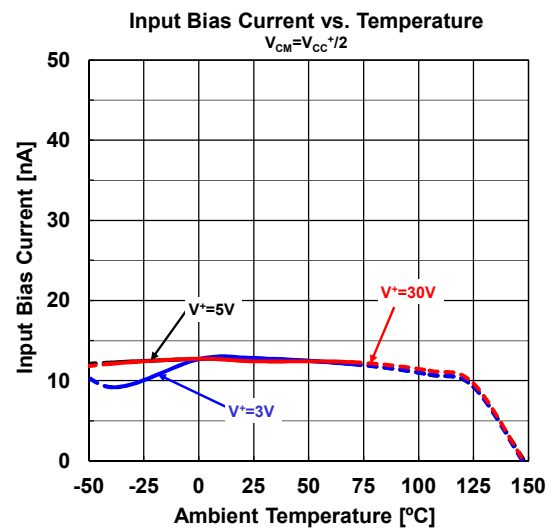
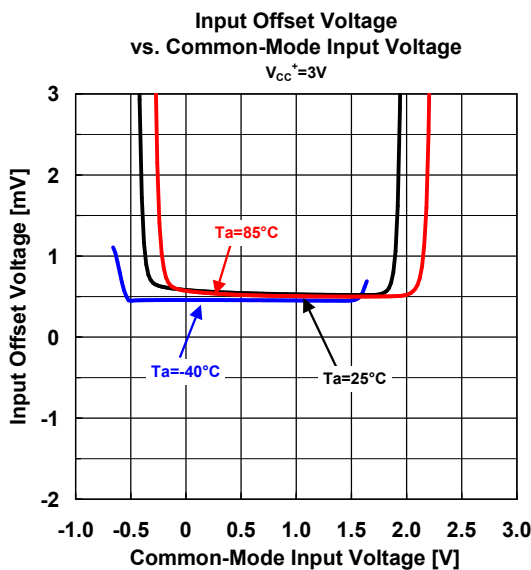
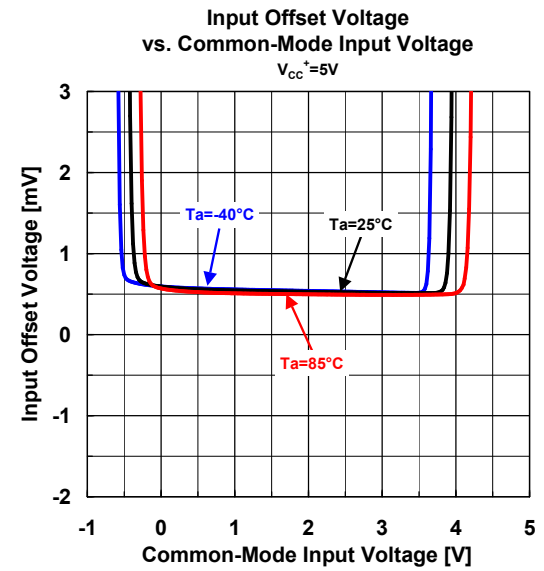
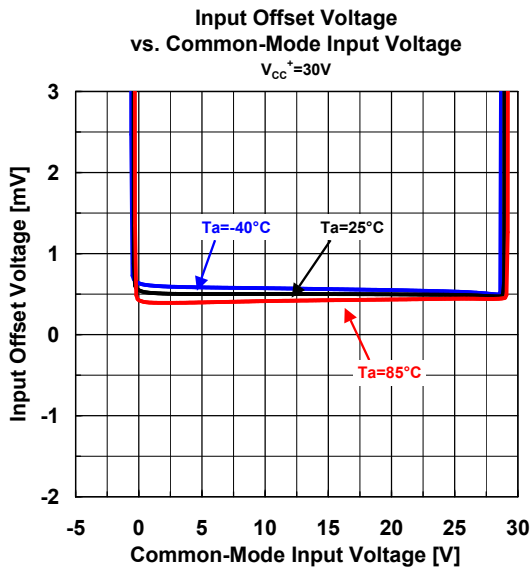
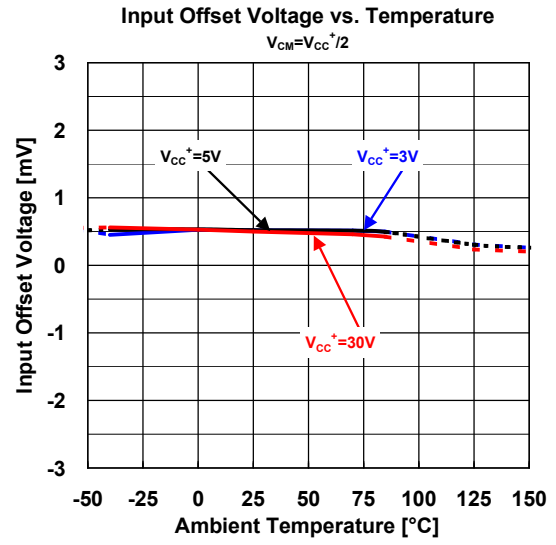
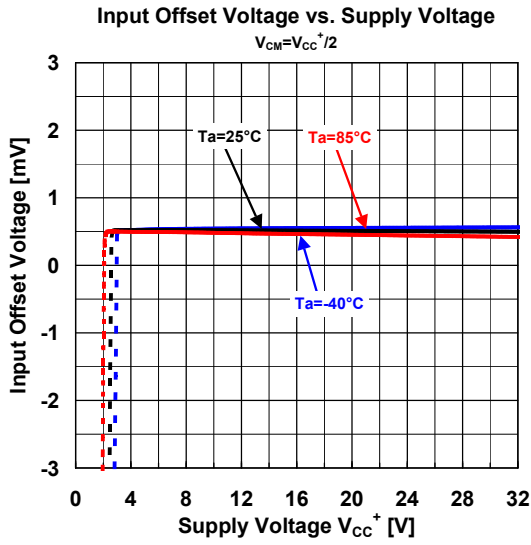
Supply Current vs. Supply Voltage  
 $G_v = 0dB$



Supply Current vs. Temperature  
 $G_v = 0dB$

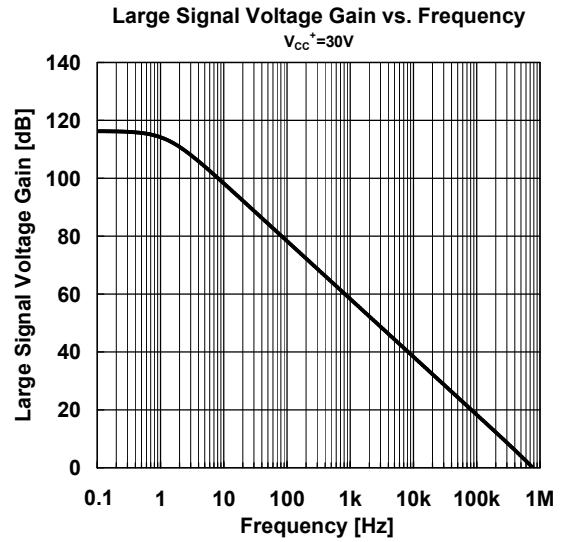
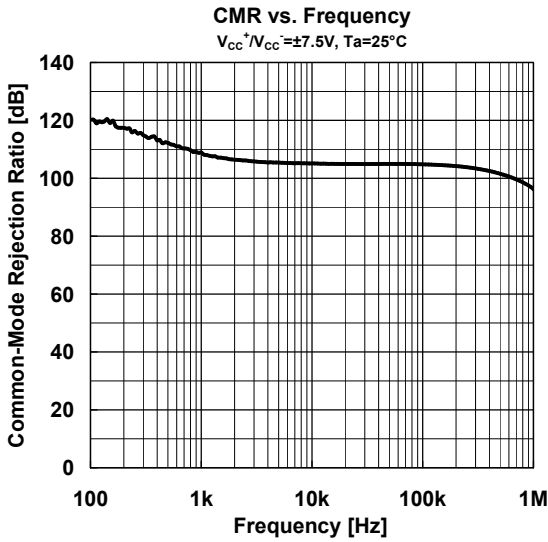
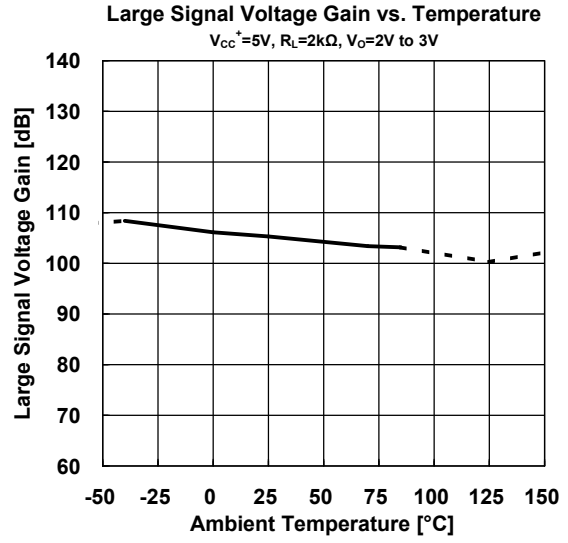
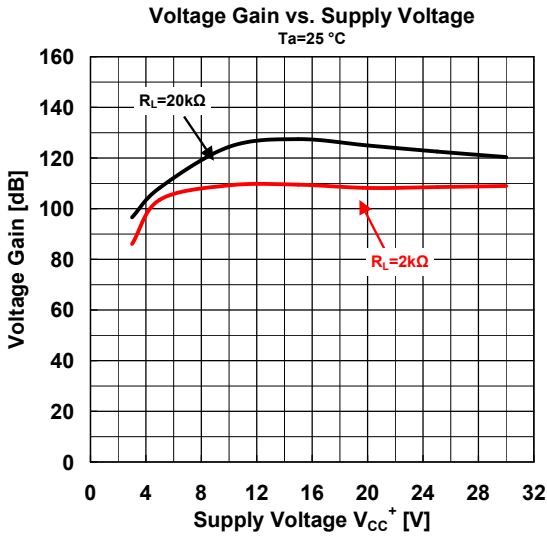


## ■ TYPICAL CHARACTERISTICS



# NJM324C/NJM324CA

## ■ TYPICAL CHARACTERISTICS

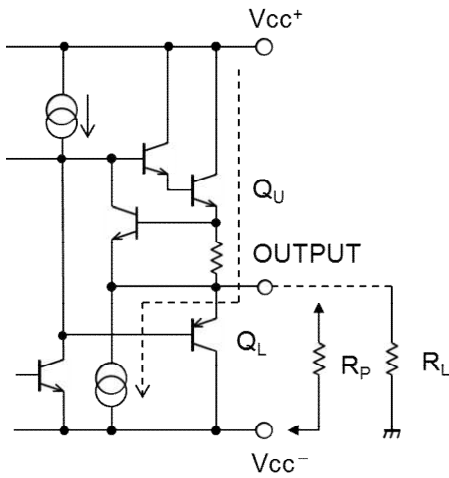




## APPLICATION

### Improvement of Cross-over Distortion

Equivalent circuit at the output stage

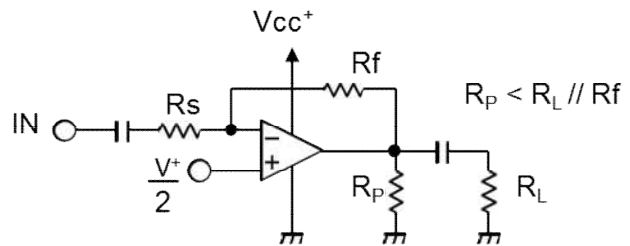
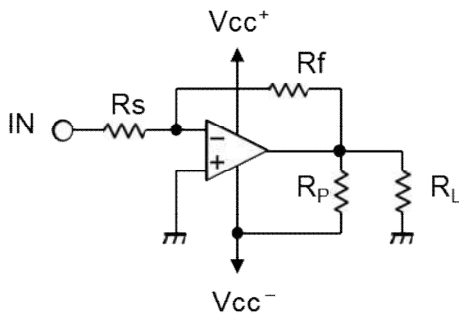


NJM324C / NJM324CA, in its static state ( No in and output condition ) when design,  $Q_U$  being biased by constant current ( break down beam ) yet,  $Q_L$  stays OFF.

While using with both power source mode, the cross-over distortion might occur instantly when  $Q_L$  ON.

There might be cases when application for amplifier of audio signals, not only distortion but also the apparent frequency bandwidth being narrowed remarkably.

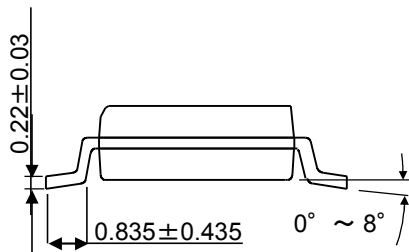
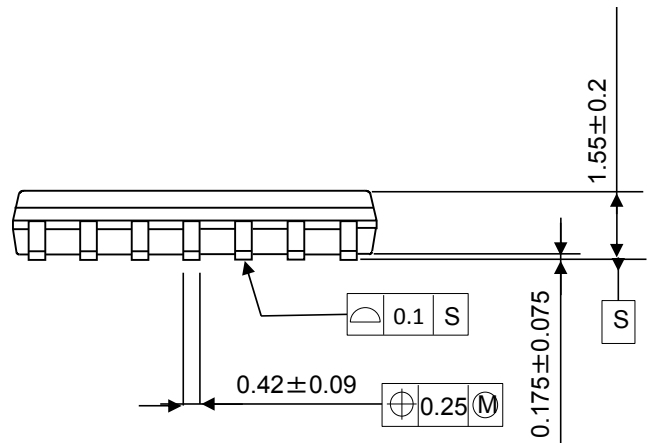
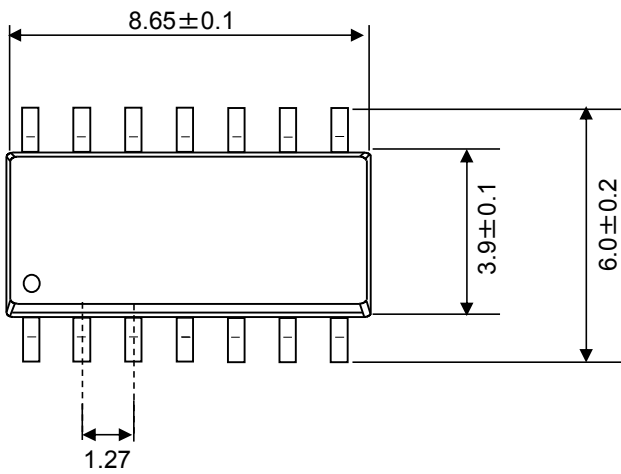
It is adjustable especially when using both power source mode, constantly to use with higher current on  $Q_U$  than the load current ( including feedback current ), and then connect the pull-down resistor  $R_P$  at the part between output and  $V_{cc-}$  pins.



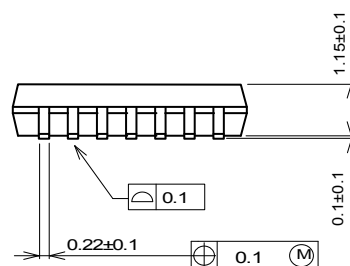
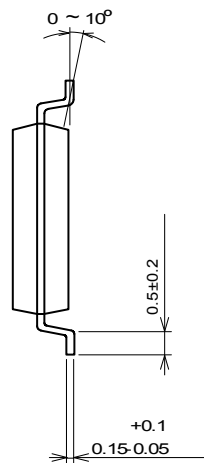
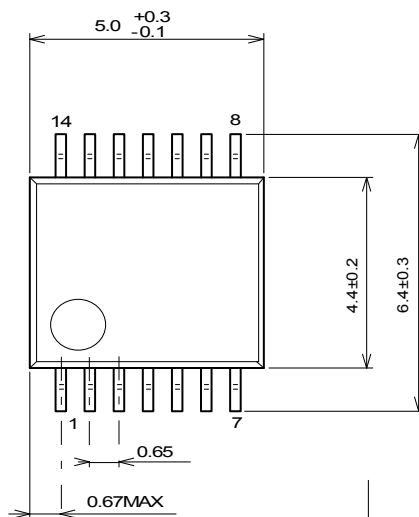
# NJM324C/NJM324CA

## ■PACKAGE OUTLINE UNIT : mm

SOP14



SSOP14



### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions.  
The application circuits in this databook are described only to show representative usages of the product and not intended for the