

Low power single channel OP-Amp

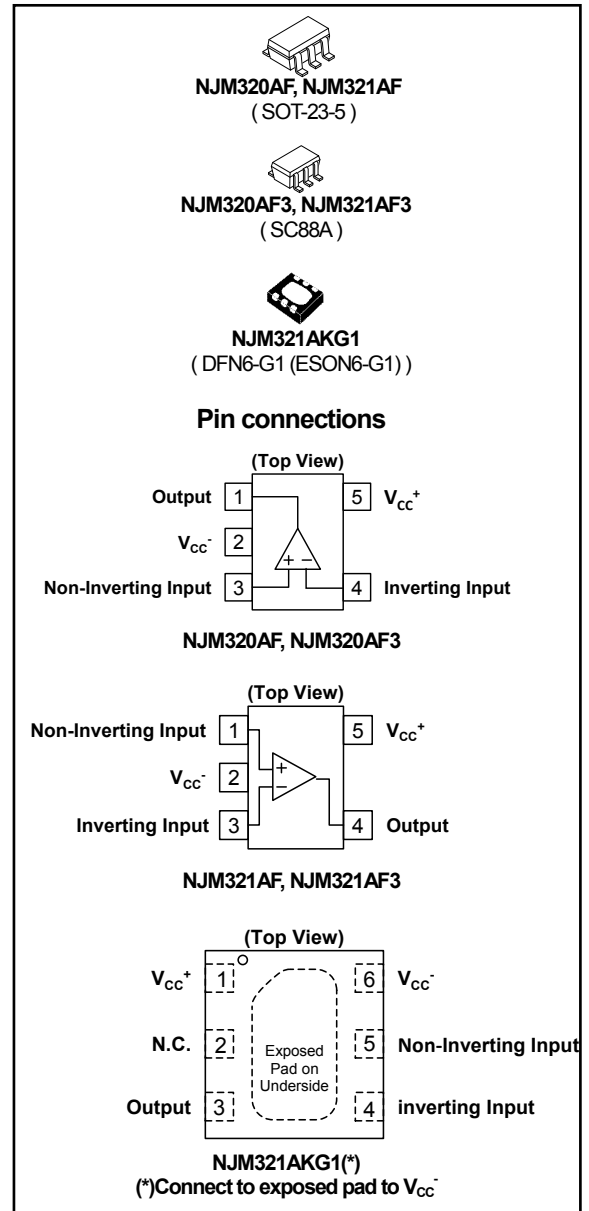
Features

- Input offset voltage : 2.5mV max.
- Input offset voltage drift : $5\mu V/^{\circ}C$ typ.
- Supply current : 0.45mA typ. at $V_{CC}^{+}=5V$
- Input bias current : 20nA typ.
- Input common-mode voltage range includes ground
- Internal ESD protection :
Human body model (HBM) $\pm 2000V$ typ.
- Integrated EMI filter : EMIRR=84dB typ. @ $f=1.8GHz$
- Wide single supply voltage range or dual supplies
+3V to +32V or $\pm 1.5V$ to $\pm 16V$

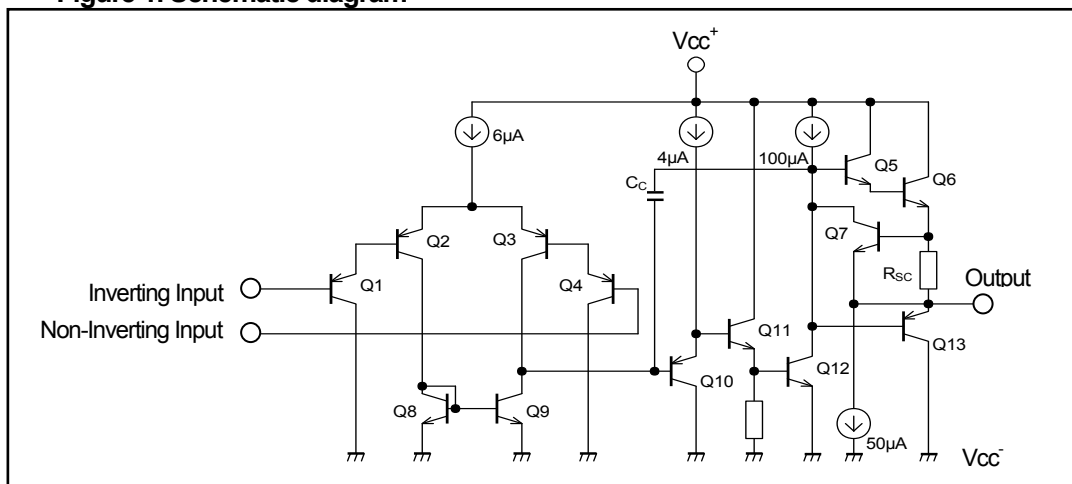
Description

The NJM320A / NJM321A consist of two independent, high gain, internally frequency compensated operation amplifiers, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks, and all the conventional OP-Amp circuits, which now can be more easily implemented in single power supply systems. For example, the NJM320A / NJM321A can be directly operated off of the standard +5V power supply voltage, which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15V$ power supplies.



1 **Schematic diagram**
Figure 1. Schematic diagram



NJM320A/NJM321A

2 Absolute maximum ratings and operating conditions

Table1. Absolute maximum ratings (T_{amb}=25°C)

Symbol	Parameter	RATINGS	Unit
V _{CC}	Supply voltage (V _{CC} ⁺ - V _{CC} ⁻)	32	V
V _{IN}	Input voltage ⁽¹⁾	V _{CC} ⁻ -0.3 to V _{CC} ⁻ +32	V
V _O	Output Terminal Input Voltage	V _{CC} ⁻ -0.3 to V _{CC} ⁺ +0.3	V
V _{ID}	Differential input voltage	±32	V
I _{IN}	Input current ⁽²⁾	5mA in DC or 50mA in AC (duty cycle = 10%, T=1s)	mA
T _{stg}	Storage temperature range	-65 to +150	°C
T _j	Maximum junction temperature	150	°C
P _D	Power Dissipation	SOT-23-5 : 480 ⁽⁴⁾ , 650 ⁽⁵⁾ SC88A : 360 ⁽⁴⁾ , 490 ⁽⁵⁾ DFN6-G1 : 330 ⁽⁶⁾ , 1200 ⁽⁷⁾	mW
θ _{ja}	Thermal resistance junction to ambient ⁽³⁾	SOT-23-5 : 260 ⁽⁴⁾ , 195 ⁽⁵⁾ SC88A : 355 ⁽⁴⁾ , 260 ⁽⁵⁾ DFN6-G1 : 385 ⁽⁶⁾ , 110 ⁽⁷⁾	°C/W
ψ _{jt}	Thermal resistance junction to top surface of IC package ⁽³⁾	SOT-23-5 : 68 ⁽⁴⁾ , 58 ⁽⁵⁾ SC88A : 91 ⁽⁴⁾ , 74 ⁽⁵⁾ DFN6-G1 : 65 ⁽⁶⁾ , 26 ⁽⁷⁾	°C/W

- Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V_{CC}⁺. The normal amplifier operation input voltage is within "Common Mode Input Voltage Range" specified in the Electrical characteristics.
 - This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
 - Short-circuit can cause excessive heating and destructive dissipation. Values are typical.
 - Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers FR4)
 - Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers FR4), internal Cu area: 74.2 x 74.2mm
 - Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)
 - Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
- *For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

Table2. Operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage (V _{CC} ⁺ - V _{CC} ⁻)	3 to 32	V
T _{oper}	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

Table3. $V_{CC^+} = +5V, V_{CC^-} = 0V, T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾ $T_{amb} = 25^{\circ}C$	-	0.5	2.5	mV
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	-	4	
DV_{io}	Input offset voltage drift $0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	5	30	$\mu V/^{\circ}C$
I_{io}	Input offset current $T_{amb} = 25^{\circ}C$	-	2	30	nA
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	-	40	
DI_{io}	Input offset current drift $0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	-	300	$pA/^{\circ}C$
I_{ib}	Input bias current ⁽²⁾ $T_{amb} = 25^{\circ}C$	-	20	150	nA
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	-	200	
A_{vd}	Large signal voltage gain ($V_{CC^+} = +15V, R_L = 2k\Omega, V_o = 1.4V$ to $11.4V$) $T_{amb} = 25^{\circ}C$	50	100	-	V/mV
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	25	-	-	
SVR	Supply voltage rejection ratio($V_{CC^+} = 5V$ to $30V, R_s < 10k\Omega$) $T_{amb} = 25^{\circ}C$	65	100	-	dB
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	65	-	-	
I_{CC}	Supply current, all amp, no load $V_{CC^+} = 5V$ $0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	0.45	0.7	mA
	$V_{CC^+} = 30V$ $0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	-	-	1	
V_{icm}	Input common mode voltage range($V_{CC^+} = +30V$ ⁽³⁾) $T_{amb} = 25^{\circ}C$	0	-	$V_{CC^+} - 1.5$	V
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	0	-	$V_{CC^+} - 2$	
CMR	Common mode rejection ratio($R_s < 10k\Omega$) $T_{amb} = 25^{\circ}C$	70	100	-	dB
	$0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$ ⁽⁵⁾	60	-	-	

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Table3. $V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25^\circ C$, (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{source}	Output source current $V_{CC}^+ = 15V, V_O = +2V, V_{id} = +1V$	20	40	-	mA
I_{sink}	Output sink current $V_{CC}^+ = 15V, V_O = +2V, V_{id} = -1V$ $V_{CC}^+ = 15V, V_O = +0.2V, V_{id} = -1V$	10 12	20 50	- -	mA μA
V_{OH}	High level output voltage($V_{CC}^+ = 30V$) $T_{amb} = 25^\circ C, R_L = 2k\Omega$ $0^\circ C \leq T_{amb} \leq 70^\circ C^{(5)}, R_L = 2k\Omega$ $T_{amb} = 25^\circ C, R_L = 10k\Omega$ $0^\circ C \leq T_{amb} \leq 70^\circ C^{(5)}, R_L = 10k\Omega$	26 26 27 27	27 - 28 -	- - - -	V
V_{OL}	Low level output voltage $T_{amb} = 25^\circ C, R_L = 10k\Omega$ $0^\circ C \leq T_{amb} \leq 70^\circ C^{(5)}, R_L = 10k\Omega$	- -	5 -	20 20	mV
SR	Slew rate $V_{CC}^+ = 15V, V_f = 0.5$ to $3V, R_L = 2k\Omega,$ $C_L = 100pF$, unity gain	-	0.6	-	V/ μs
GBP	Gain bandwidth product $V_{CC}^+ = 30V, f = 100kHz, V_{in} = 10mV,$ $R_L = 2k\Omega, C_L = 100pF$	-	1.1	-	MHz
THD	Total harmonic distortion $f = 1kHz, A_v = 20dB, R_L = 2k\Omega, V_O = 2V_{pp},$ $C_L = 100pF$	-	0.02	-	%
e_n	Equivalent input noise voltage $f = 1kHz, R_S = 100\Omega, V_{CC}^+ = 30V$	-	30	-	nV/ \sqrt{Hz}

1. $V_O = 1.4V, R_S = 0\Omega, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V$.

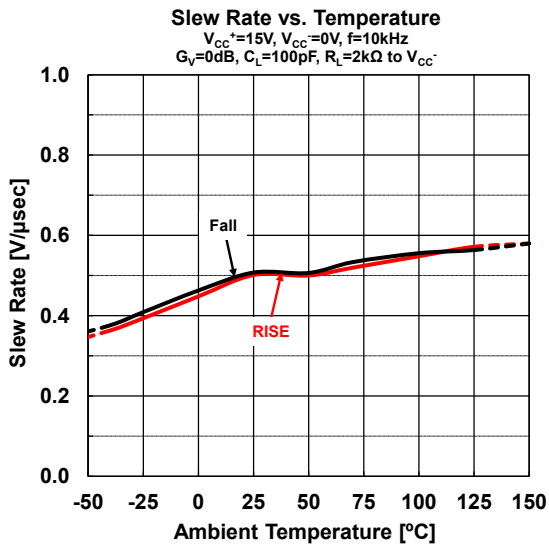
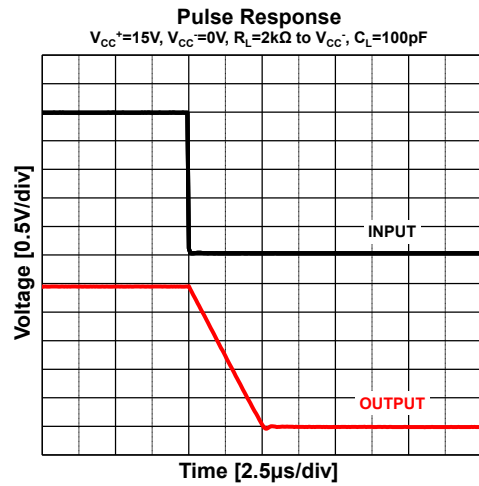
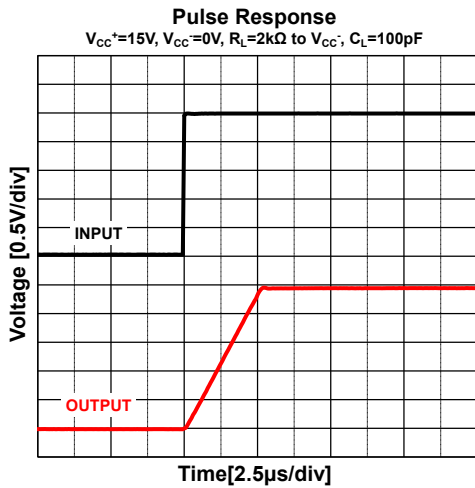
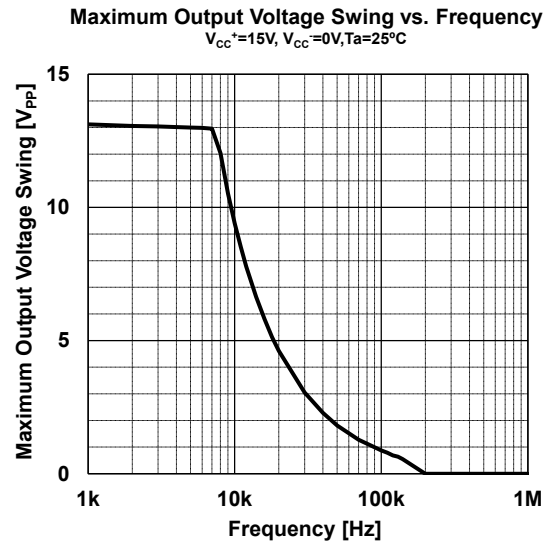
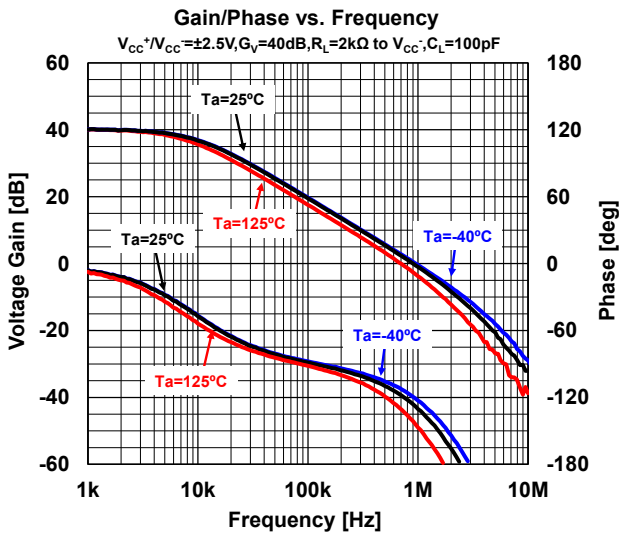
2. The direction of the input current is out of the IC.

3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$, but either or both inputs can go to +32V without damage.

4. Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling.

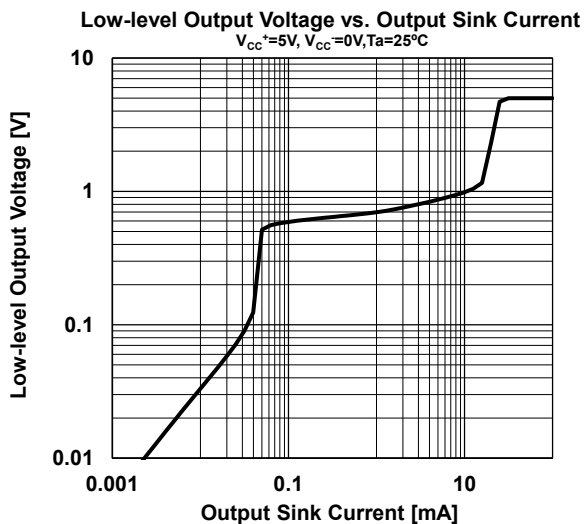
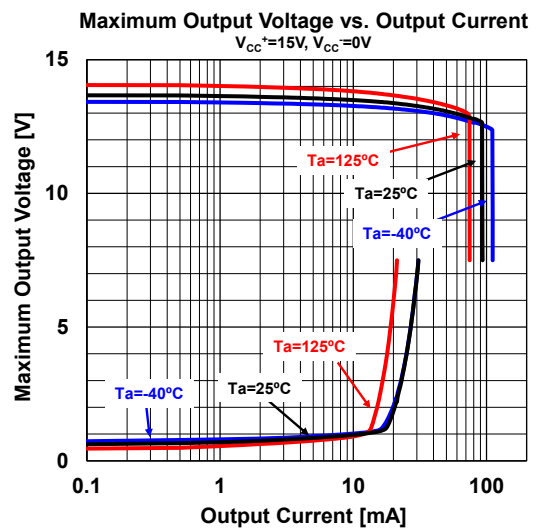
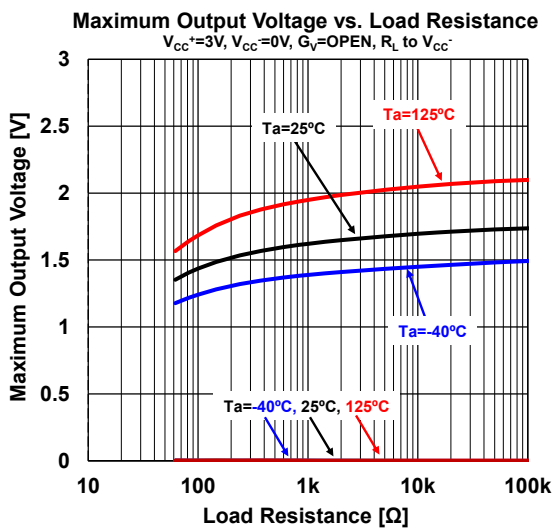
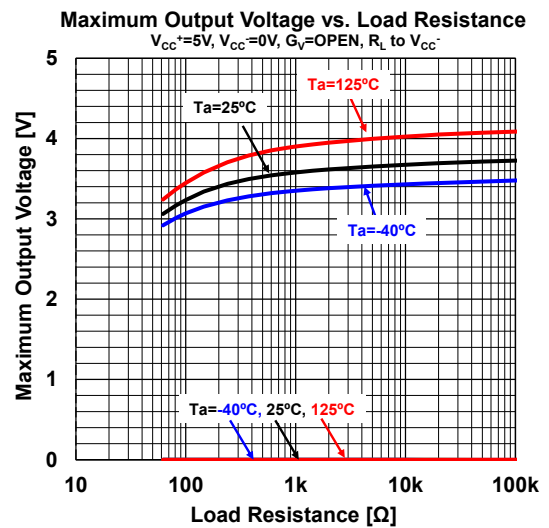
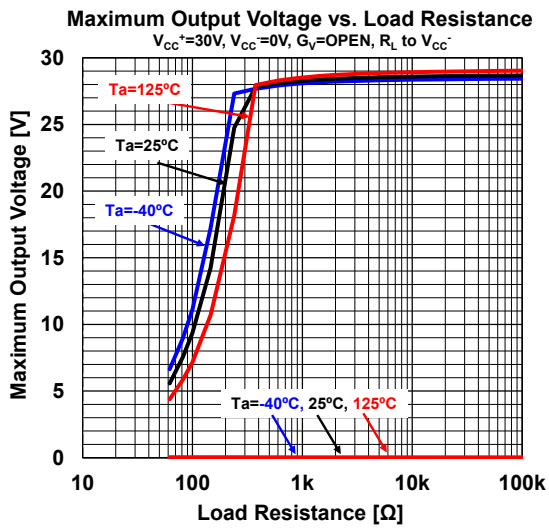
5. This parameter is not 100% test.

TYPICAL CHARACTERISTICS



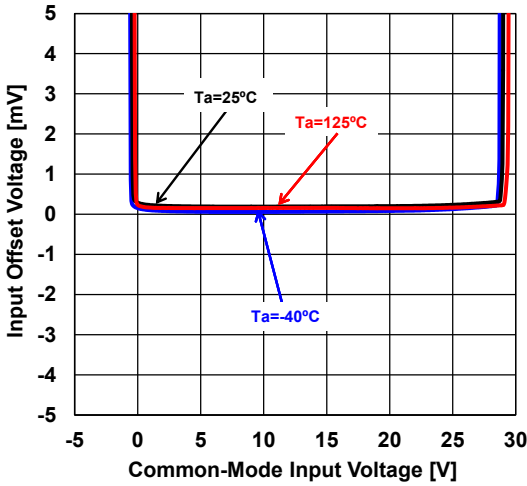
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TYPICAL CHARACTERISTICS

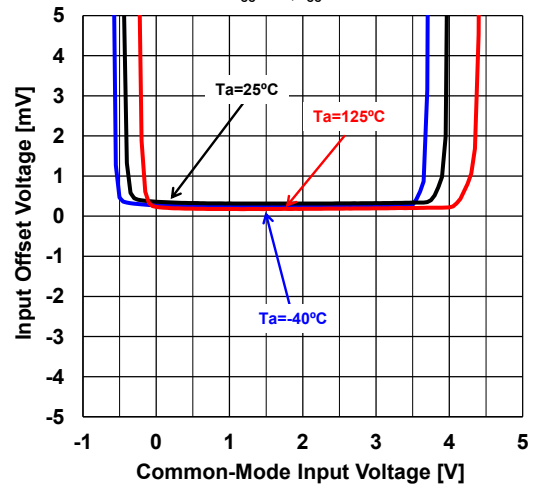


TYPICAL CHARACTERISTICS

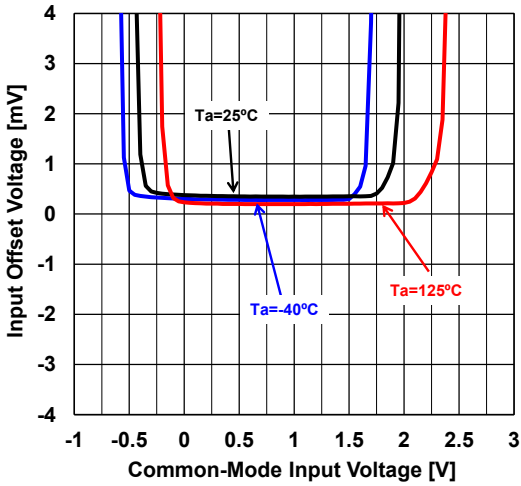
Input Offset Voltage vs.
Common-Mode Input Voltage
 $V_{CC^+}=30V, V_{CC^-}=0V$



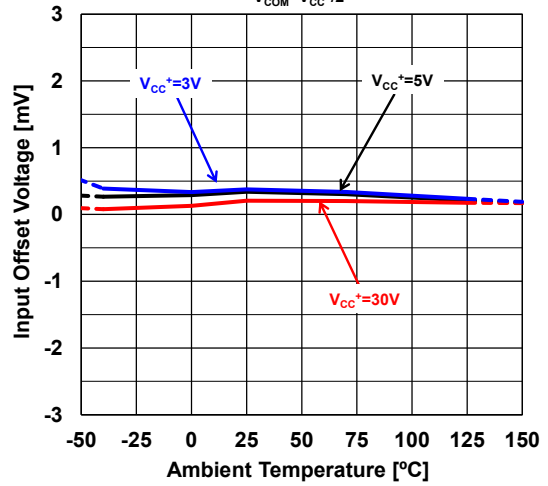
Input Offset Voltage vs.
Common-Mode Input Voltage
 $V_{CC^+}=5V, V_{CC^-}=0V$



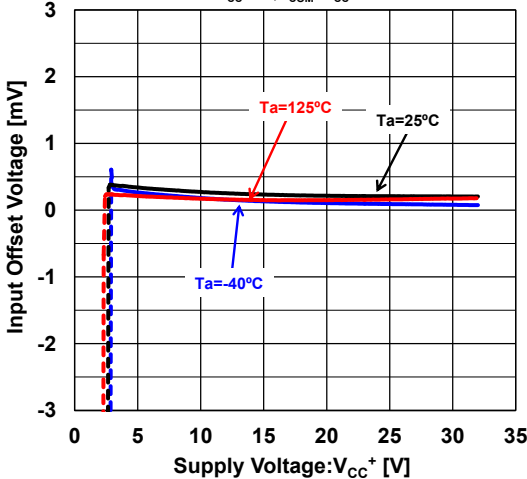
Input Offset Voltage vs.
Common-Mode Input Voltage
 $V_{CC^+}=3V, V_{CC^-}=0V$



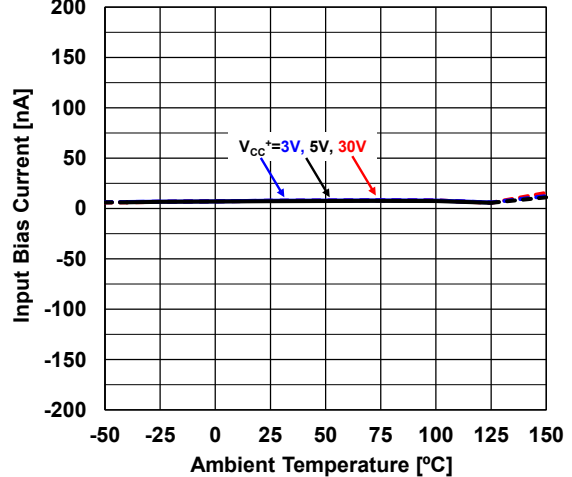
Input Offset Voltage vs. Temperature
 $V_{COM}=V_{CC^+}/2$



Input Offset Voltage vs. Supply Voltage
 $V_{CC^-}=0V, V_{COM}=V_{CC^+}/2$

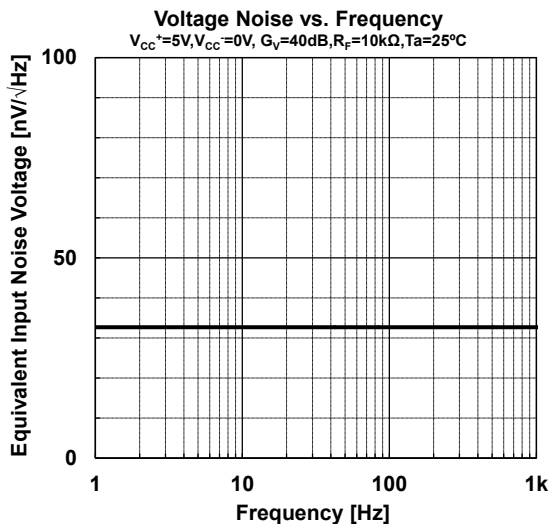
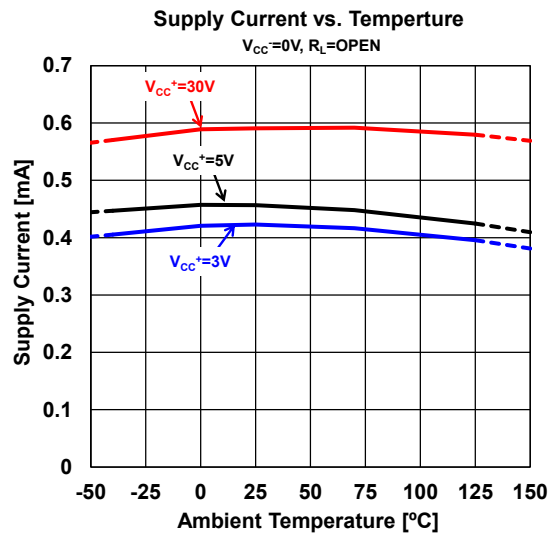
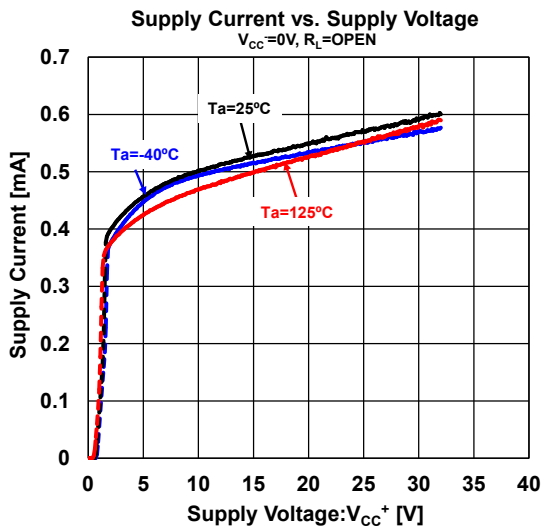
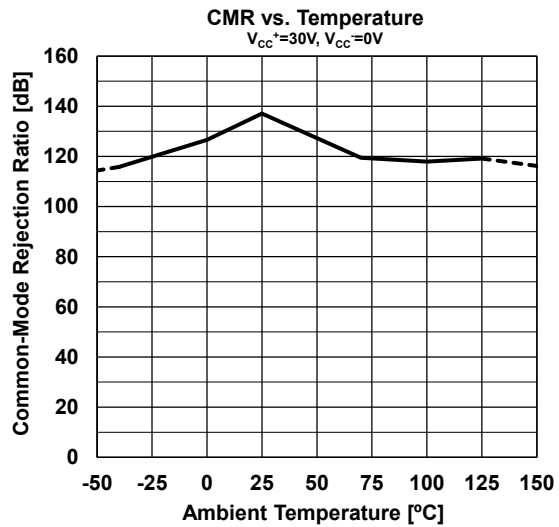
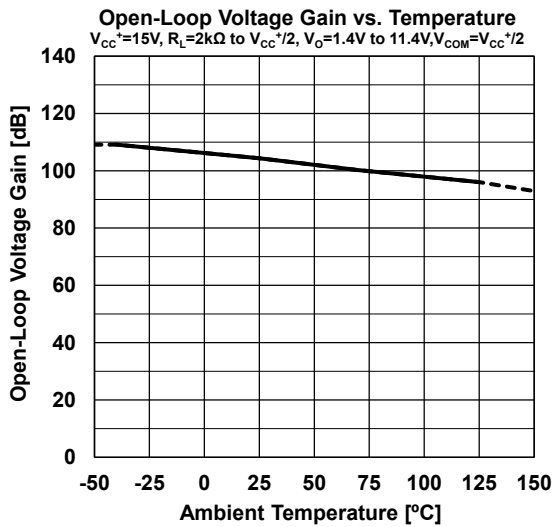


Input Bias Current vs. Temperature
 $V_{CC^-}=0V, V_{COM}=0V$



NJM320A/NJM321A

TYPICAL CHARACTERISTICS



APPLICATION NOTE

EMIRR(EMI Rejection Ratio) Definition

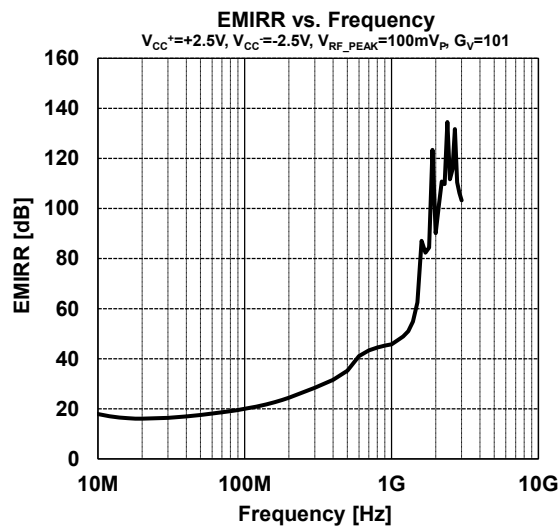
EMIRR is a parameter indicating the EMI robustness of an OP-Amp. The definition of EMIRR is given by the following a formula (1). We can grasp the tolerance of the RF signal by measuring an RF signal and offset voltage shift quantity.

Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

$$EMIRR = 20 \cdot \log \left(\frac{V_{RF_PEAK}}{|\Delta V_{IO}|} \right) \quad \dots(1)$$

V_{RF_PEAK} : RF Signal Amplitude [V_P]

ΔV_{IO} : Input offset voltage shift quantity [V]

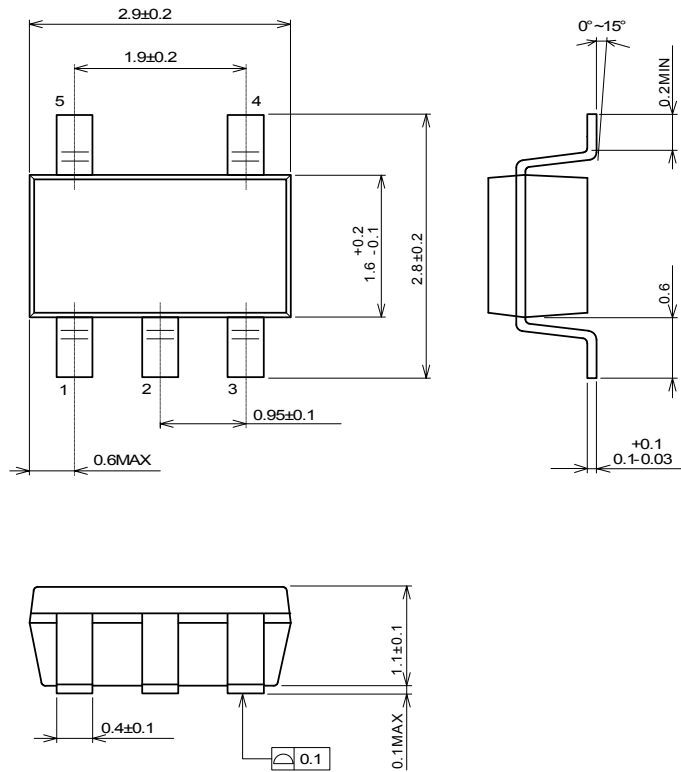


*For details, refer to " Application Note for EMI Immunity" in our HP: <http://www.njr.com/>

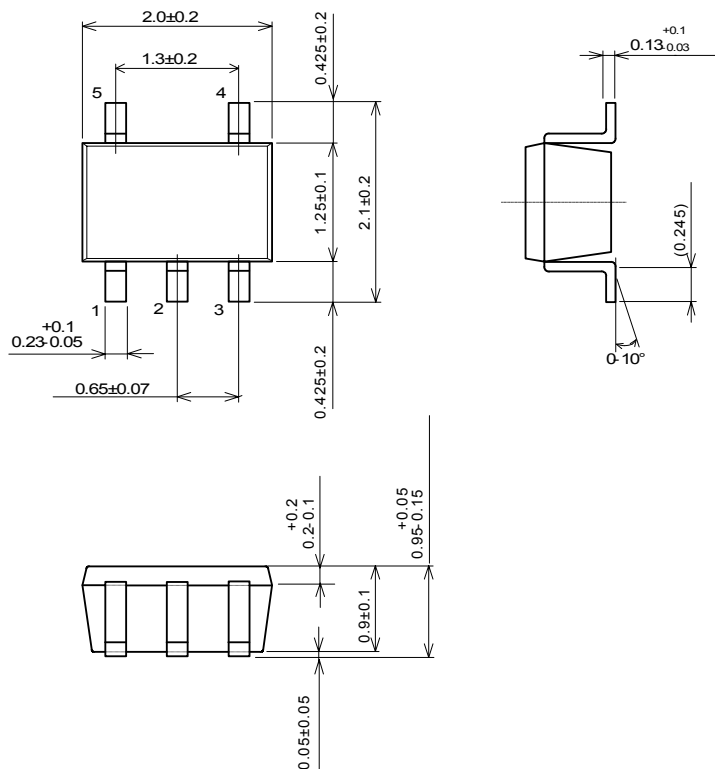
NJM320A/NJM321A

■PACKAGE OUTLINE UNIT : mm

SOT-23-5

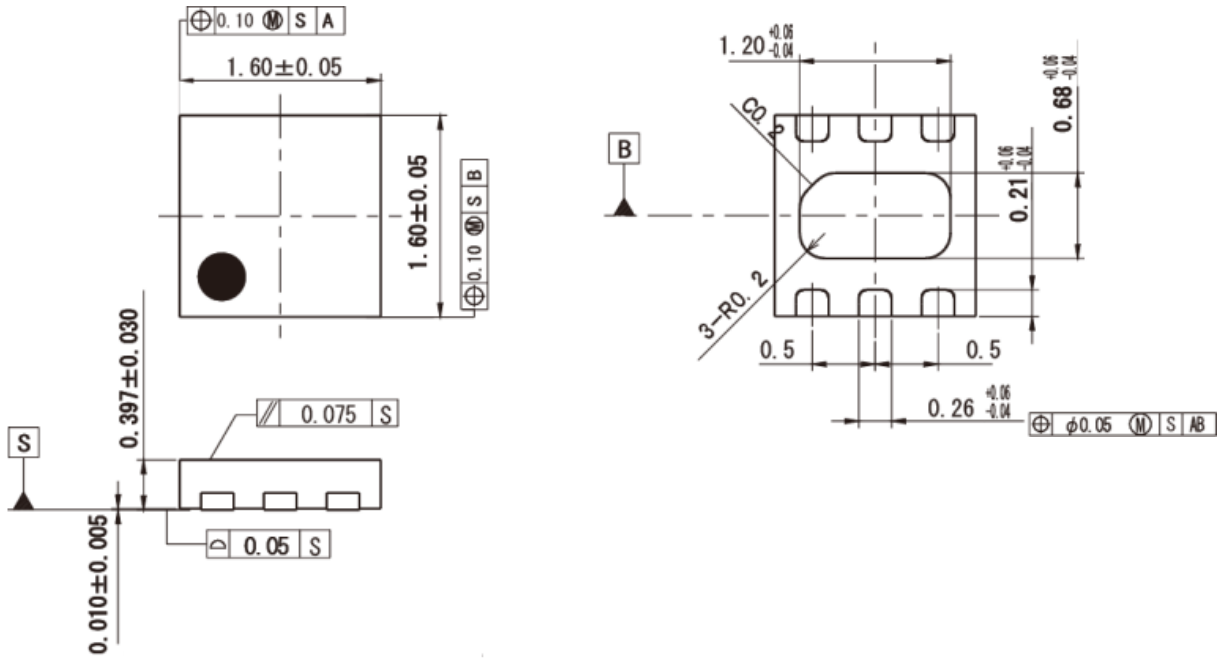


SC-88A



■PACKAGE OUTLINE UNIT : mm

DFN6-G1 (ESON6-G1)



[CAUTION]
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