Very Low Output Low Dropout Regulator

**GENERAL DESCRIPTION**

The NJM2842 is a very low output voltage, low drop out regulators.

It delivers up to 1A output current with the output voltage from 0.8V to 1.8V.

The use of an external bias voltage can improve the transient response and the ripple rejection characteristics while maintaining minimum input to output voltage.

The NJM2842 suitable for constant-voltage source such as CPU, DSP and ASIC.

**FEATURES**

- **Output Voltage Range** 0.8V to 1.8V
- **High Ripple Rejection** 91 dB typ. @ $V_O=1.2V$
- **Output Noise Voltage** $V_{NO}=44\,\mu V_{rms}\,\text{typ.}\,\@ V_O=1.2V$
- **Output Current** $I_O(\text{min})=1.0A$
- **High Precision Output** $V_O=1.0\%
- **Dual input Voltage Type** $V_{IN}, V_{BIAS}$ (sequence free)
- **High Stability for Load** 0.002%/mA (max)
- **Output Capacitor with 4.7µF ceramic capacitor**
- **Low Dropout Voltage** 0.1V typ. @ $I_O=600mA$
- **ON/OFF Control**
- **Built-in Thermal Overload Protection and Current Limit Protection**
- **Bipolar Technology**
- **Package Outline** SOT-89-5, DFN6-H1 (ESON6-H1), TO-252-5

**PIN CONFIGURATION**

![Pin Configuration Diagram]

The NJM2842U2 and NJM2842DL3 have the following pin configurations:

- **CONTROL**, **GND**, **VOUT**, **VIN**, **VBIAS**
- **Exposed PAD on backside connected to GND.**

New Japan Radio Co., Ltd.
**NJM2842**

### BLOCK DIAGRAM

![Block Diagram](image)

### OUTPUT VOLTAGE RANK LIST

<table>
<thead>
<tr>
<th>Device Name</th>
<th>$V_O$</th>
<th>Device Name</th>
<th>$V_O$</th>
<th>Device Name</th>
<th>$V_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT-89-5</td>
<td>0.8V</td>
<td>NJM2842KH1-008</td>
<td>0.8V</td>
<td>NJM2842DL3-011</td>
<td>1.1V</td>
</tr>
<tr>
<td>NJM2842U2-008</td>
<td>1.0V</td>
<td>NJM2842KH1-010</td>
<td>1.0V</td>
<td>NJM2842DL3-012</td>
<td>1.2V</td>
</tr>
<tr>
<td>NJM2842U2-010</td>
<td>1.1V</td>
<td>NJM2842KH1-012</td>
<td>1.2V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NJM2842U2-011</td>
<td>1.2V</td>
<td>NJM2842KH1-015</td>
<td>1.5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NJM2842U2-012</td>
<td>1.45V</td>
<td>NJM2842KH1-018</td>
<td>1.8V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NJM2842U2-0145</td>
<td>1.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NJM2842U2-015</td>
<td>1.8V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NJM2842U2-018</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

### ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>RATINGS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_{IN}$</td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>Bias Voltage</td>
<td>$V_{BIAS}$</td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>Control Voltage</td>
<td>$V_{CONT}$</td>
<td>+7</td>
<td>V</td>
</tr>
</tbody>
</table>

| Power Dissipation | $P_D$ | SOT-89-5 | 625 (*1) | 2400 (*2) |
|                  |       | TO-252-5 | 1190(*1) | 3125(*2)  |
|                  |       | DFN6-H1 (ESON6-H1) | 440 (*3) | 1200 (*4) |

| Operating Temperature | Topr | -40 ~ +125 | °C |
| Storage Temperature   | Tstg | -40 ~ +150  | °C |

(*1): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)  
(*2): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: based on EIA/JDEC standard, 4Layers)  
(4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)  
(*3): Mounted on glass epoxy board based on EIA/JEDEC. (101.5x114.5x1.6mm, 2Layers, Use the Exposed Pad)  
(*4): Mounted on glass epoxy board based on EIA/JEDEC. (101.5x114.5x1.6mm, 4Layers, Use the Exposed Pad)  
(4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

### BIAS VOLTAGE INPUT RANGE

- $V_{BIAS}=+2.5V$ to $+5.5V$  
- $V_{BIAS}=V_O+1V$ to $+5.5V$  
- $V_O<1.5V$  
- $V_O\geq1.5V$
ELECTRICAL CHARACTERISTICS

(V_{BIAS}=2.5V(V_{O}+1V), V_{IN}=V_{O}+1V, C_{BIAS}=0.1\mu F, C_{B}=4.7\mu F, C_{O}=4.7\mu F, Ta=25°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITION</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>V_{O}</td>
<td>I_{O}=30mA</td>
<td>1.0%</td>
<td>-</td>
<td>+0.1%</td>
<td>V</td>
</tr>
<tr>
<td>Unloaded Bias Current</td>
<td>I_{BIAS}</td>
<td>I_{O}=0mA, except I_{CONT}</td>
<td>-</td>
<td>300</td>
<td>500</td>
<td>\mu A</td>
</tr>
<tr>
<td>Unloaded Input Current</td>
<td>I_{IN}</td>
<td>I_{O}=0mA, except I_{CONT}</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>\mu A</td>
</tr>
<tr>
<td>Bias Current at Control OFF</td>
<td>I_{BIAS(OFF)}</td>
<td>V_{CONT}=0V</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>nA</td>
</tr>
<tr>
<td>Input Current at Control OFF</td>
<td>I_{(NOFF)}</td>
<td>V_{CONT}=0V</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>nA</td>
</tr>
<tr>
<td>Output Current</td>
<td>I_{O}</td>
<td>V_{O} x 0.9</td>
<td>1000</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>Line Regulation 1 (V_{BIAS})</td>
<td>ΔV_{O}/ΔV_{BIAS}</td>
<td>V_{BIAS}=2.5V to +5.5V(V_{O}&lt;1.5V)</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>%/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{BIAS}=3.8V(V_{O}≥1.5V)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>%/V</td>
</tr>
<tr>
<td>Line Regulation 2 (V_{IN})</td>
<td>ΔV_{O}/ΔV_{IN}</td>
<td>V_{IN}=V_{O}+1V to +5.5V, I_{O}=30mA</td>
<td>-</td>
<td>-</td>
<td>0.10</td>
<td>%/V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>ΔV_{O}/ΔI_{O}</td>
<td>I_{O}=30mA to 1000mA</td>
<td>-</td>
<td>-</td>
<td>0.002</td>
<td>%/mA</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>V_{O}</td>
<td>I_{O}=600mA</td>
<td>-</td>
<td>0.10</td>
<td>0.18</td>
<td>V</td>
</tr>
<tr>
<td>Ripple Rejection Ratio 1 (V_{BIAS})</td>
<td>RR(V_{BIAS})</td>
<td>V_{BIAS}=3.5V(V_{O}&lt;1.5V)</td>
<td>Refer to Table 1</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{BIAS}=3.8V(V_{O}≥1.5V)</td>
<td>Refer to Table 1</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ripple Rejection Ratio 2 (V_{IN})</td>
<td>RR(V_{IN})</td>
<td>ein=200mVrms, f=1kHz, I_{O}=10mA</td>
<td>Refer to Table 1</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average Temperature Coefficient of Output Voltage</td>
<td>ΔV_{O}/ΔTa</td>
<td>Ta=0 to +85°C, I_{O}=10mA</td>
<td>±50</td>
<td>-</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Output Noise Voltage</td>
<td>V_{NO}</td>
<td>f=10Hz to 80kHz, I_{O}=10mA</td>
<td>Refer to Table 1</td>
<td>\mu Vrms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control Current</td>
<td>I_{CONT}</td>
<td>V_{CONT}=1.6V</td>
<td>1.6</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Control Voltage for ON-state</td>
<td>V_{CONT(ON)}</td>
<td>-</td>
<td>-</td>
<td>0.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Control Voltage for OFF-state</td>
<td>V_{CONT(OFF)}</td>
<td>-</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Bias Voltage</td>
<td>V_{BIAS}</td>
<td>-</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>V_{IN}</td>
<td>-</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Table 1

<table>
<thead>
<tr>
<th>Voltage Rank</th>
<th>Ripple Rejection Ratio 1 (V_{BIAS})</th>
<th>Ripple Rejection Ratio 2 (V_{IN})</th>
<th>Output Noise Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>MIN.</td>
<td>TYP.</td>
<td>MAX.</td>
</tr>
<tr>
<td>0.8V</td>
<td>-</td>
<td>77</td>
<td>-</td>
</tr>
<tr>
<td>1.0V</td>
<td>-</td>
<td>75</td>
<td>-</td>
</tr>
<tr>
<td>1.1V</td>
<td>-</td>
<td>74</td>
<td>-</td>
</tr>
<tr>
<td>1.2V</td>
<td>-</td>
<td>73</td>
<td>-</td>
</tr>
<tr>
<td>1.45V</td>
<td>-</td>
<td>71</td>
<td>-</td>
</tr>
<tr>
<td>1.5V</td>
<td>-</td>
<td>71</td>
<td>-</td>
</tr>
<tr>
<td>1.8V</td>
<td>-</td>
<td>70</td>
<td>-</td>
</tr>
</tbody>
</table>
Power Dissipation vs. Ambient Temperature

**NJM2842U2 (SOT-89-5)**

*Power Dissipation (Topr = -40°C to +125°C, Tj=150°C)*

- On 4 layers board
- On 2 layers board

**NJM2842DL3 (TO-252-5)**

*Power Dissipation (Topr = -40°C to +125°C, Tj=150°C)*

- On 4 layers board
- On 2 layers board

**NJM2842KH1 (DFN6-H1)**

*Power Dissipation (Topr = -40°C to +125°C, Tj=150°C)*

- On 4 layers board
- On 2 layers board
**TEST CIRCUIT**

![Circuit Diagram]

**TYPICAL APPLICATION**

a) In case of where ON/OFF control is not required:

![Diagram a]

b) In use of ON/OFF control:

![Diagram b]

State of control pin:

“H” → output is enabled.

“L” or “open” → output is disabled.
In the case of using a resistance "R" between $V_{\text{BIAS}}$ and control.

If this resistor is inserted, it can reduce the control current when the control voltage is high.

The applied voltage to control pin should set to consider voltage drop through the resistor "R" and the minimum control voltage for ON-state.

The $V_{\text{CONT(ON)}}$ and $I_{\text{CONT}}$ have temperature dependence as shown in the "Control Current vs. Temperature" and "Control Voltage vs. Temperature" characteristics. Therefore, the resistance "R" should be selected to consider the temperature characteristics.

* Bias Capacitance ($C_{\text{BIAS}}$) and an Input Capacitance ($C_{\text{IN}}$)

$C_{\text{BIAS}}$ and $C_{\text{IN}}$ are required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended $C_{\text{BIAS}}$ and $C_{\text{IN}}$ value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between $V_{\text{BIAS}}$-GND and $V_{\text{IN}}$-GND as shortest path as possible to avoid the problem.

*Output Capacitor $C_{\text{O}}$

Output capacitor ($C_{\text{O}}$) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller $C_{\text{O}}$ may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

On the other hand, Use of a larger $C_{\text{O}}$ reduces output noise and ripple output, and also improves output transient response when rapid load change.

Therefore, use the recommended $C_{\text{O}}$ value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and $V_{\text{OUT}}$ as shortest path as possible for stable operation.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting $C_{\text{O}}$, recommend that have withstand voltage margin against output voltage and superior temperature characteristic.
TYPICAL CHARACTERISTICS

**Output Voltage vs. Input Voltage**

- Temperature: 25°C
- Input Voltage: 2.2V
- Bias Voltage: 2.5V
- Capacitors: Cin = Co = 4.7 μF (Ceramic)
- Bias Capacitor: Cbias = 0.1 μF (Ceramic)

**Output Voltage vs. Bias Voltage**

- Temperature: 25°C
- Input Voltage: 2.2V
- Bias Voltage: 2.5V
- Capacitors: Cin = Co = 4.7 μF (Ceramic)
- Bias Capacitor: Cbias = 0.1 μF (Ceramic)

**Output Voltage vs. Output Current**

- Temperature: 25°C
- Bias Voltage: 2.5V
- Capacitors: Cin = Co = 4.7 μF (Ceramic)
- Bias Capacitor: Cbias = 0.1 μF (Ceramic)

**Ground Pin Current vs. Output Current**

- Temperature: 25°C
- Bias Voltage: 2.5V
- Capacitors: Cin = Co = 4.7 μF (Ceramic)
- Bias Capacitor: Cbias = 0.1 μF (Ceramic)

**Control Current vs. Control Voltage**

- Temperature: 25°C
- Bias Voltage: 2.5V
- Capacitors: Cin = Co = 4.7 μF (Ceramic)
- Bias Capacitor: Cbias = 0.1 μF (Ceramic)

**Output Voltage vs. Control Voltage**

- Temperature: 25°C
- Bias Voltage: 2.5V
- Capacitors: Cin = Co = 4.7 μ F (Ceramic)
- Bias Capacitor: Cbias = 0.1 μ F (Ceramic)

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New Japan Radio Co., Ltd.

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Load Regulation vs. Output Current

![Graph showing load regulation vs. output current for NJM2842_1.2V. The graph includes the following details:

- Temperature: Ta=25°C
- Input Voltage: Vin=2.2V
- Bias Voltage: Vbias=2.5V
- Capacitors: Cin=Co=4.7μF (Ceramic), Cbias=1μF (Ceramic)

Peak Output Current vs. Input Voltage

![Graph showing peak output current vs. input voltage for NJM2842_1.2V. The graph includes the following details:

- Temperature: Ta=25°C
- Bias Voltage: Vbias=2.5V
- Capacitors: Cin=Co=4.7μF (Ceramic), Cbias=1μF (Ceramic)

Unloaded Input Current vs. Input Voltage

![Graph showing unloaded input current vs. input voltage for NJM2842_1.2V. The graph includes the following details:

- Temperature: Ta=25°C
- Bias Voltage: Vbias=2.5V
- Capacitors: Cin=Co=4.7μF (Ceramic), Cbias=0.1μF (Ceramic)

Unloaded Bias Current vs. Bias Voltage

![Graph showing unloaded bias current vs. bias voltage for NJM2842_1.2V. The graph includes the following details:

- Temperature: Ta=25°C
- Input Voltage: Vin=2.2V
- Output Voltage: Vcnt=1.6V
- Capacitors: Cin=Co=4.7μF (Ceramic), Cbias=0.1μF (Ceramic)

Dropout Voltage vs. Output Current

![Graph showing dropout voltage vs. output current for NJM2842_1.2V. The graph includes the following details:

- Temperature: Ta=25°C
- Bias Voltage: Vbias=2.5V
- Capacitors: Cin=Co=4.7μF (Ceramic), Cbias=1μF (Ceramic)

Output Noise Voltage vs. Output Current

![Graph showing output noise voltage vs. output current for NJM2842_1.2V. The graph includes the following details:

- Temperature: Ta=25°C
- Input Voltage: Vin=2.2V
- Bias Voltage: Vbias=2.5V
- Capacitors: Cin=Co=4.7μF, Cbias=0.1μF]
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