

3-INPUT 1-OUTPUT 3-CIRCUIT VIDEO AMPLIFIER WITH LPF

■ GENERAL DESCRIPTION

NJM2515 is the 3-input 1-output 3-circuit video amplifier. Internal LPF is progressive correspondence. Also the High Definition (30MHz) is realized by LPF through mode. It is the best for the video system corresponding to a component video signal or a RGB signal.

■ PACKAGE OUTLINE

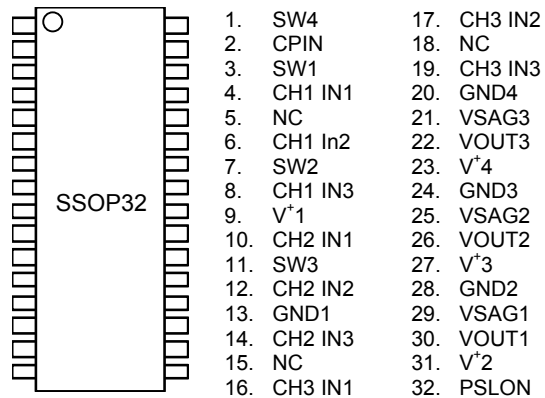


NJM2515V

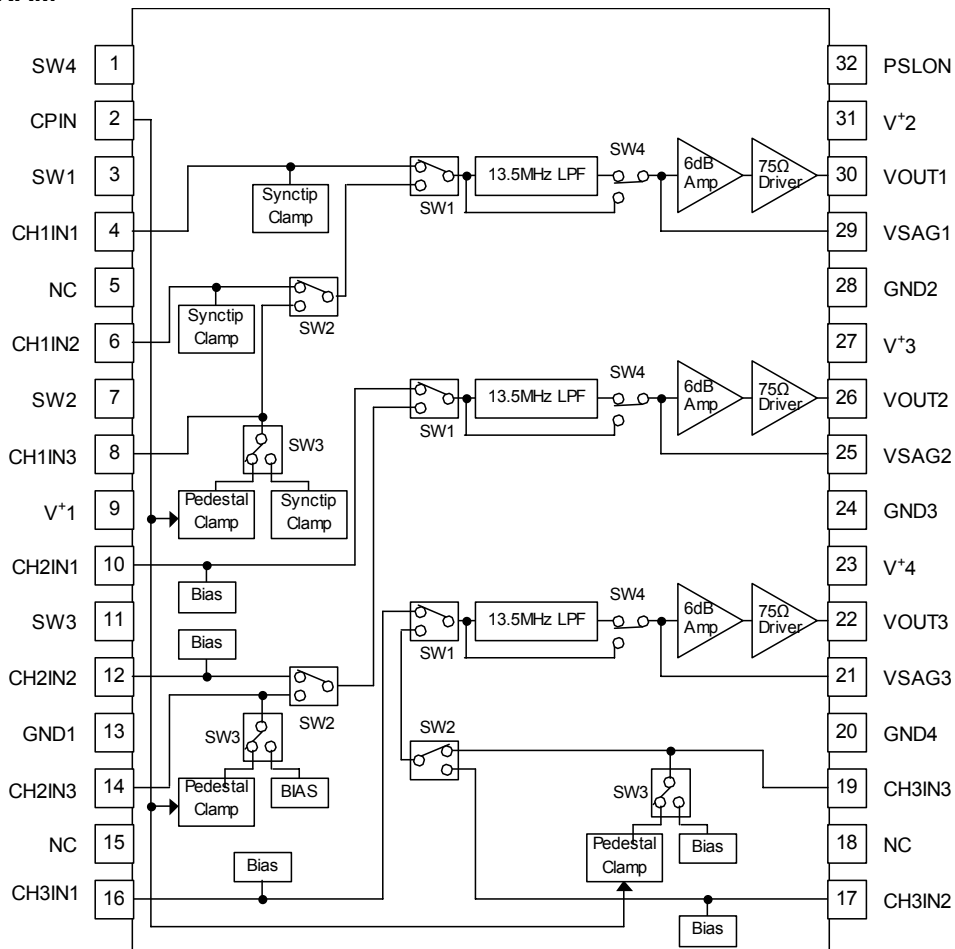
■ FEATURES

- Operating voltage 4.5 to 5.5V
- Internal 3-input 1-output 3-circuit video switch
- Internal LPF 0dBtyp.at 13.5MHz
- Internal LPF through switch 0dBtyp.at 34MHz
- Internal 6dB amplifier
- Internal 75ohm driver
- Internal Power Save circuit
- Bipolar technology
- Package outline SSOP32

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



NJM2515

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	10.0	V
Power Dissipation	P _D	1250*	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstr	-40 to +150	°C

*EIA/JEDEC STANDARD Test Board (76.2x114.3x1.6mm, 4layers,FR-2) mounting

■ RECOMMENDED OPERATING CONDITION (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vopr		4.5	5.0	5.5	V

■ ELECTRICAL CHARACTERISTICS (V⁺1= V⁺2= V⁺3= V⁺4=5V, RL=150ohm, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I _{CC}	V ⁺ 1 to V ⁺ 4, No signal	-	27	40	mA
Supply Current with Power Save Mode	I _{save}	V ⁺ 1 to V ⁺ 4, Power save mode	-	0.6	1.3	mA
Maximum Output Level 1	V _{omy}	Vin=100kHz sin-signal, THD=1% Select to sync-chip clamp	2.4	2.5	-	Vp-p
Maximum Output Level 2	V _{om} PbPr	Vin=100kHz sin-signal, THD=1% Select to bias	2.4	2.5	-	Vp-p
Maximum Output Level 3	V _{om} RGB	Vin=100kHz sin-signal, THD=1% Select to pedestal clamp	1.8	1.9	-	Vp-p
Voltage Gain	G _v	Vin=1MHz, 1.0Vp-p sin-signal	6.0	6.4	6.8	dB
Voltage Gain Difference between Input Terminal	ΔG _{vI}	Vin=1MHz, 1.0Vp-p sin-signal, IN1 to IN2 to IN3 for all channel	-0.2	0	0.2	dB
Voltage Gain Difference between Channel	ΔG _{vB}	Vin=1MHz, 1.0Vp-p sin-signal, CH1 to CH2 to CH3	-0.2	0	0.2	dB
LPF Characteristics 1	G _f 13.5M	13.5MHz/1MHz, 1.0Vp-p, sin-signal	-3.0	0	1.0	dB
LPF Characteristics 2	G _f 54M	54MHz/1MHz, 1.0Vp-p, sin-signal	-	-40	-	dB
Frequency Characteristics	G _f	Vin=34MHz/1MHz, 1.0Vp-p sin-signal, select to LPF through mode	-	0	-	dB
Crosstalk between Input Terminal 1	CT-I1	Vin=4.43MHz, 1.0Vp-p sin-signal, IN1 to IN2 to IN3 for all channel	-	-70	-	dB
Crosstalk between Input Terminal 2	CT-I2	Vin=30MHz, 1.0Vp-p sin-signal, IN1 to IN2 to IN3 for all channel	-	-50	-	dB
Crosstalk between Channel 1	CT-B1	Vin=4.43MHz, 1.0Vp-p sin-signal, CH1 to CH2 to CH3	-	-70	-	dB
Crosstalk between Channel 2	CT-B2	Vin=30MHz, 1.0Vp-p sin-signal, CH1 to CH2 to CH3	-	-50	-	dB
Differential Gain	DG	Vin=1.0Vp-p, 10step video signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p, 10step video signal	-	0.3	-	deg
S/N Ratio	SN	Vin=1.0Vp-p, 100% white video signal, 100KHz to 6MHz	-	70	-	dB

■ ELECTRICAL CHARACTERISTICS ($V^+1 = V^+2 = V^+3 = V^+4 = 5V$, $R_L = 150\Omega$, $T_a = 25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Switch High level for power save	VthPH	PS	2.0	-	V^+	V
Switch Low level for power save	VthPL	PS	0	-	0.6	V
Switch High level for input signal switch	VthSH	SW1, SW2	2.0	-	V^+	V
Switch High level for input signal switch	VthSL	SW1, SW2	0	-	0.6	V
High level for CP IN	Vth CPH		2.0	-	V^+	V
Low level for CP IN	Vth CPL		0	-	0.6	V

■ CONTROL SIGNAL

TERMINAL	CONTROL	NOTE
PS	H	Power save: OFF (Operation)
	L	Power save: ON (Mute)
	OPEN	Power save: ON (Mute)

TERMINAL	CONTROL	NOTE	
SW 1, SW2	SW1	SW2	
	L, OPEN	X	IN1 (X=don't care)
	H	L, OPEN	IN2
	H	H	IN3

TERMINAL	CONTROL	NOTE
SW 3	H	Y,Pb,Pr (CH1IN3: Sync Tip Clamp CH2IN3/CH3IN3: Bias)
	L	RGB (CH1IN3/CH2IN3/CH3IN3: Pedestal Clamp)
	OPEN	RGB (CH1IN3/CH2IN3/CH3IN3: Pedestal Clamp)

TERMINAL	CONTROL	NOTE
SW4	H	LPF
	L	Through
	OPEN	Through

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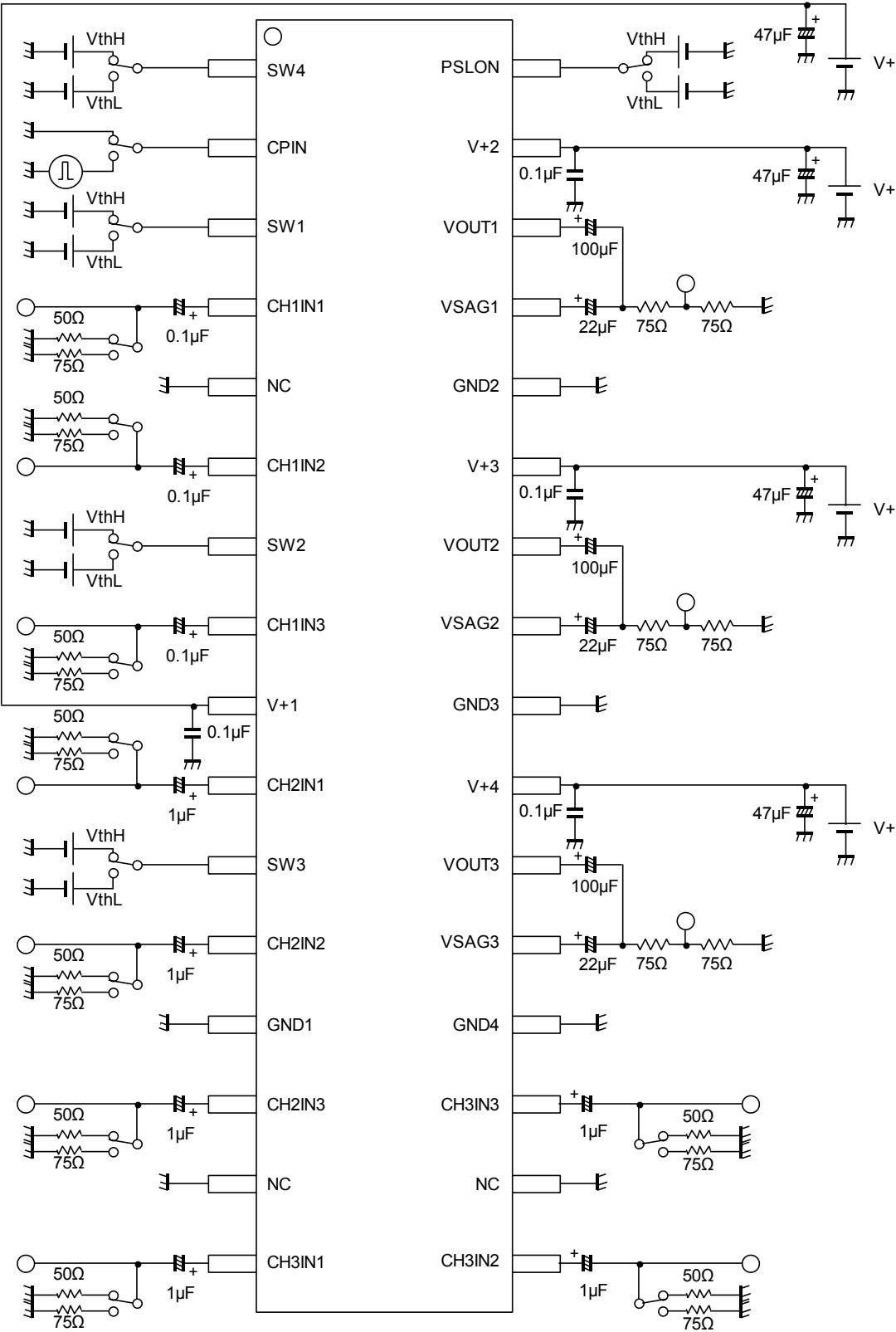
■ TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
1	SW4	LPF/ THROUGH control terminal		-
3	SW1	Input selector control 1 terminal		
7	SW2	Input selector control 2 terminal		
11	SW3	Y,Pb,Pr/ RGB control terminal		
2	CP IN	CLAMP Pulse input terminal		-
32	PSLON	Power Save control terminal		
4	CH1 IN1	Y/G input 1 terminal		Sync-chip clamp 2.0V Pedestal clamp 2.3V
6	CH1 IN2	Y/G input 2 terminal		
8	CH1 IN3	Y/G input 3 terminal		
10	CH2 IN1	Pb/ B input 1 terminal		Bias 2.6V Pedestal clamp 2.3V
12	CH2 IN2	Pb/ B input 2 terminal		
14	CH2 IN3	Pb/ B input 3 terminal		
16	CH3 IN1	Pr/ R input 1 terminal		
17	CH3 IN2	Pr/ R input 2 terminal		
19	CH3 IN3	Pr/ R input 3 terminal		

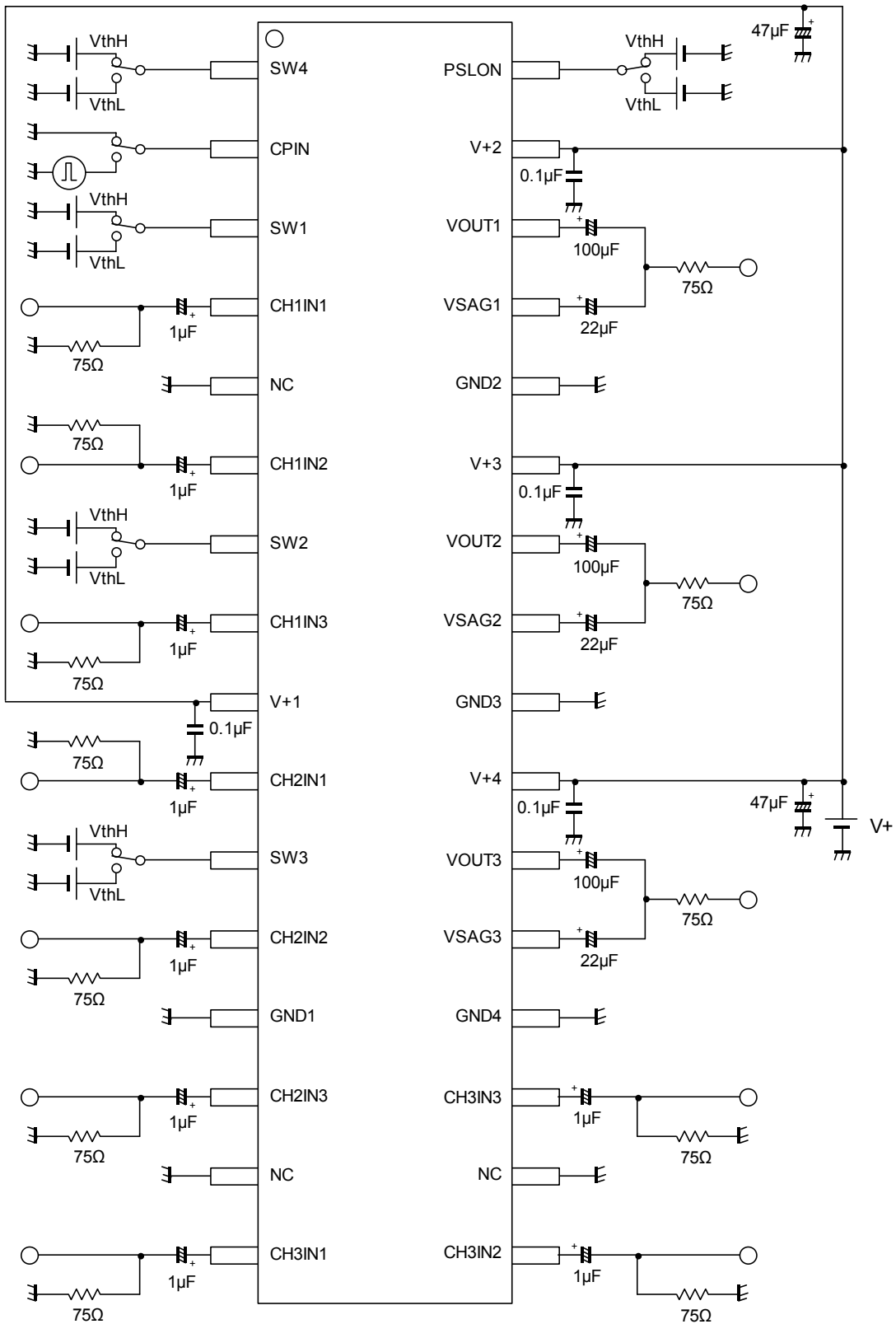
PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
22	VOUT3	Output 3 terminal		Sync-chip clamp 1.2V Pedestal clamp 1.8V Bias 2.5V
26	VOUT2	Output 2 terminal		
30	VOUT1	Output 1 terminal		
21	VSAG3	Sag correction 3 terminal		1.9V
25	VSAG2	Sag correction 2 terminal		
29	VSAG1	Sag correction 1 terminal		
9	V ⁺ 1	Supply voltage 1 terminal		-
23	V ⁺ 4	Supply voltage 4 terminal		
27	V ⁺ 3	Supply voltage 3 terminal		
31	V ⁺ 2	Supply voltage 2 terminal		
13	GND1	GND 1 terminal		-
20	GND4	GND 4 terminal		
24	GND3	GND 3 terminal		
28	GND2	GND 2 terminal		

NJM2515

TEST CIRCUIT



APPLICATION CIRCUIT



APPLICATION

(1) Pedestal - clamp, Clamp - pulse (Terminal name: CH1IN3, CH2IN3, CH3IN3)

1. Select to pedestal - clamp (SW3: Low or OPEN) at RGB signal input.
 - Clamp - pulse input at back-porch period. (Refer Fig.A)
 - Clamp - pulse input in synchronous to input signal.
 - When used clamp-pulse, clamp-pulse keep going input in synchronous to input signal.Clamp-pulse timing is following.

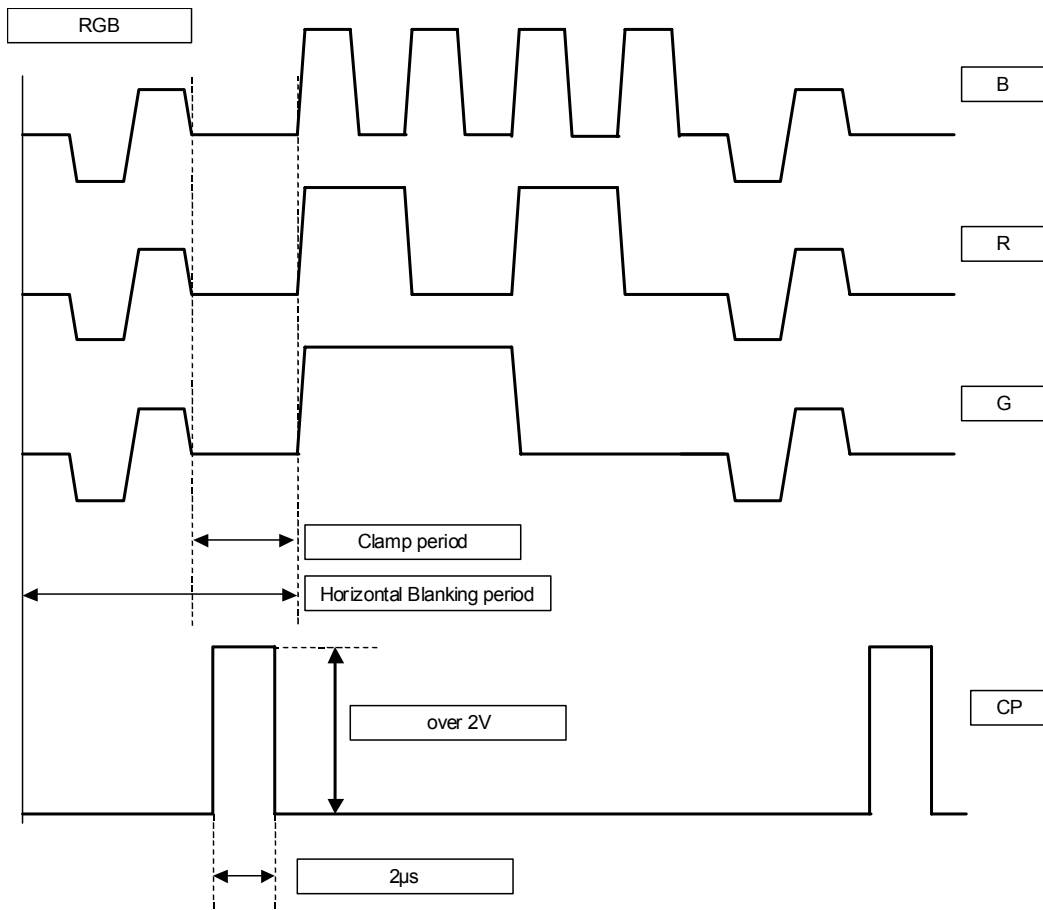


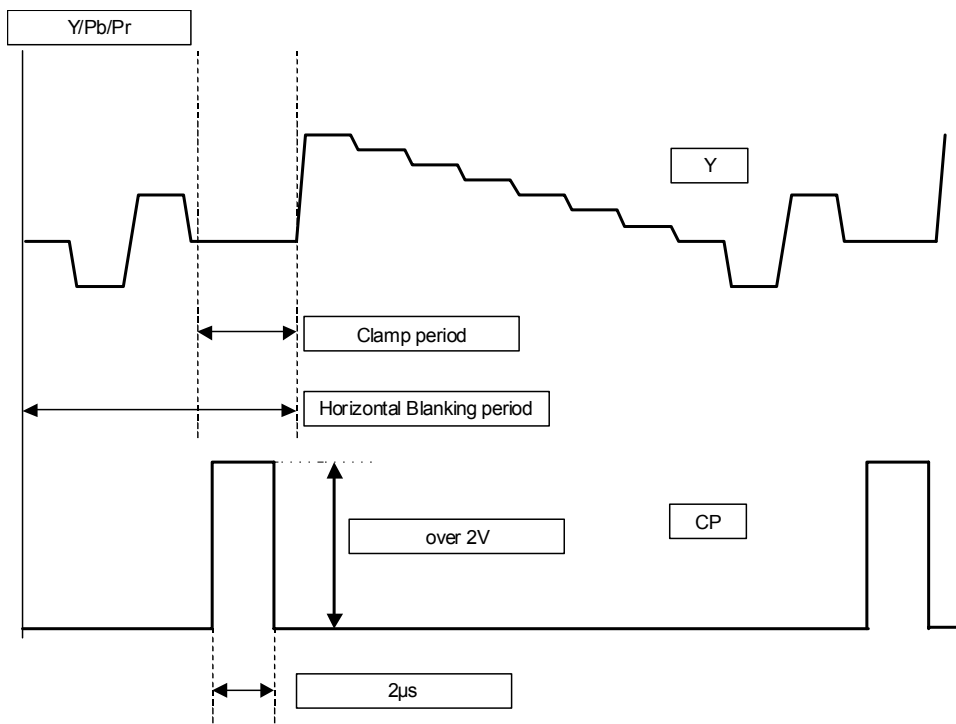
Fig.A: Clamp-pulse timing (RGB)

2. Select to sync- chip –clamp or bias (SW3: High) at component signal input.
 - When not used pedestal-clamp, clamp-pulse don't input.
We recommend CPIN (pin2) connect to GND.

When clamp-pulse can not stopping:

- Clamp - pulse input in synchronous to input signal. (Refer Fig.B)
- Note) When clamp-pulse isn't synchronous, come out possibility of over shoot or under shoot on video signal. (Refer Fig.C)

Clamp-pulse timing is following.



Y/Pb/Pr Fig.B: Clamp-pulse timing (at synchronous)

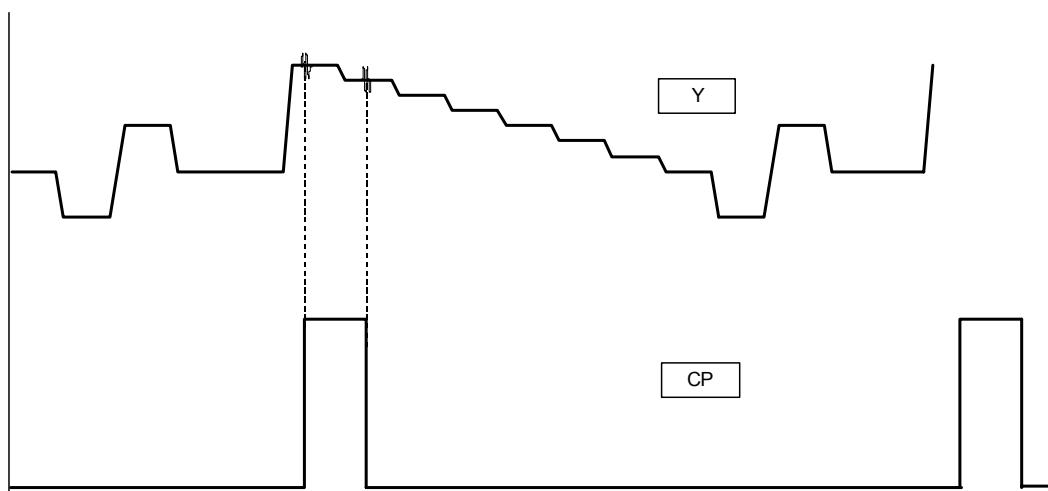


Fig.C: Clamp-pulse timing (at no-synchronous)

(2) Two-system output

We don't recommend driving the two-line load of 75Ω. (75Ω+75Ω // 75Ω+75Ω " Total load resistance = 75Ω ")
 Adjust R_L of figure 2 referring to Figure 1 when two system outputs are necessary.
 Cancel the SAG correction for the two-line drive. Connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 1000μF or more.

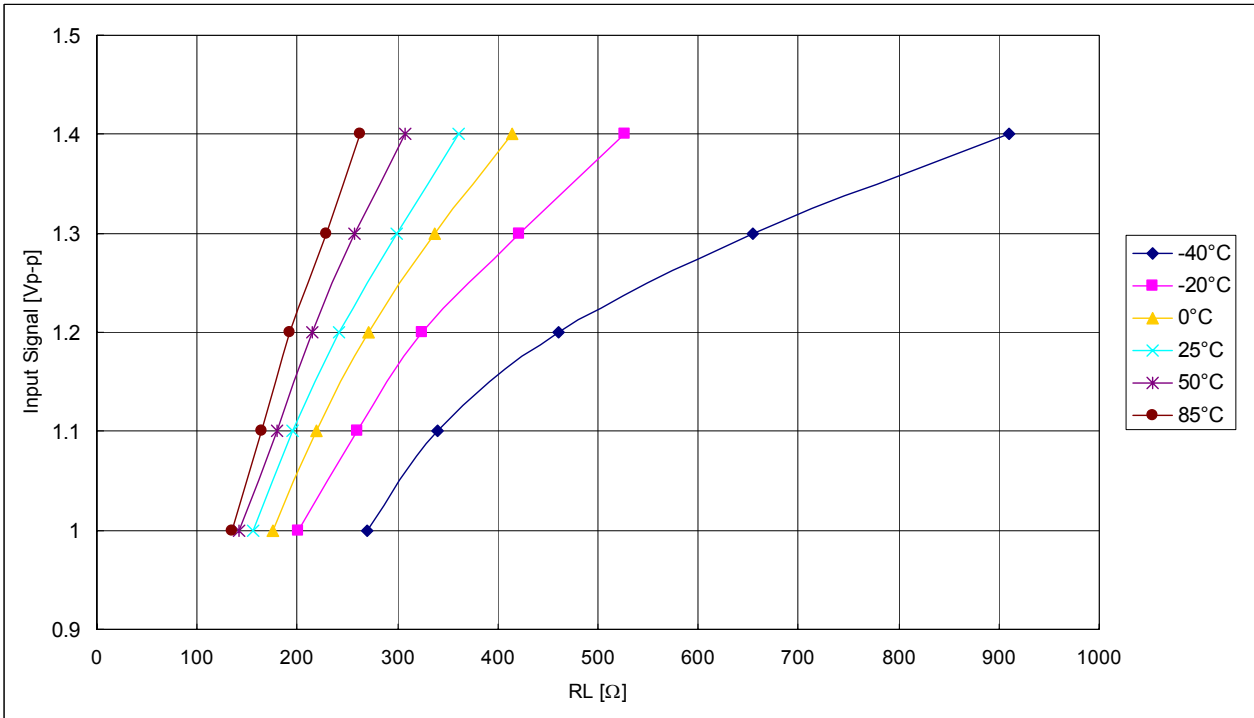


Figure 1 Input Signal vs. Load Resistance (R_L) Characteristic

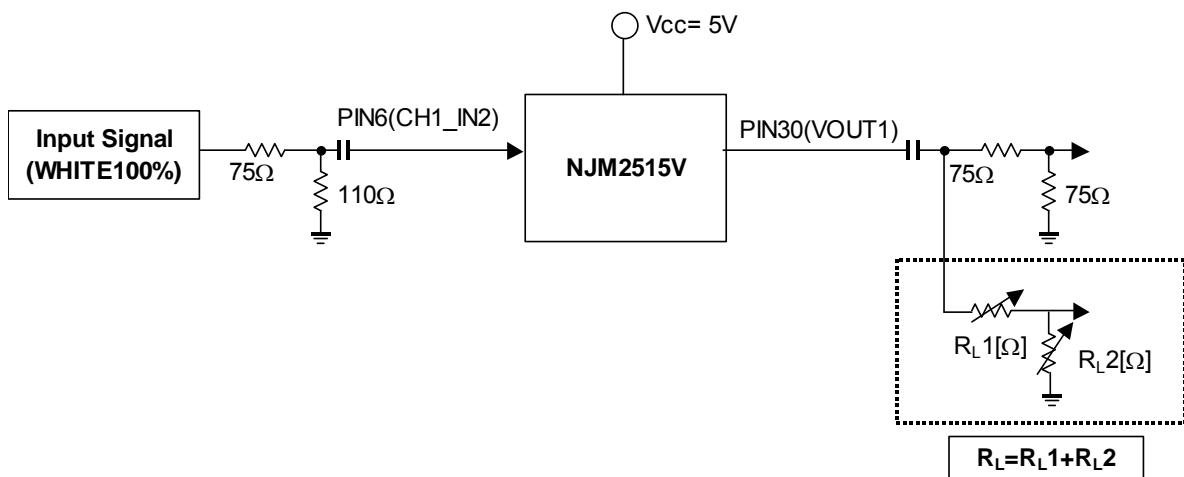
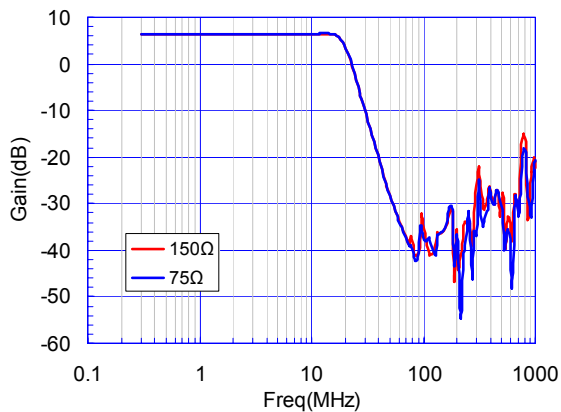


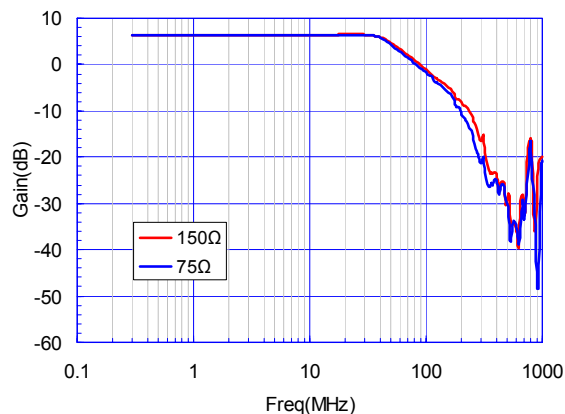
Figure 2 Test Circuit

TYPICAL CHARACTERISTICS

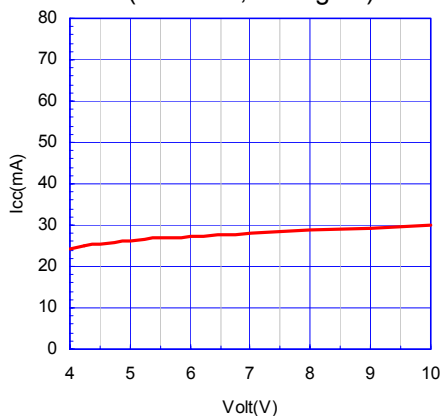
Voltage gain vs. Frequency
($V_{in}=1\text{MHz}, 1.0\text{Vp-p, LPF}$)



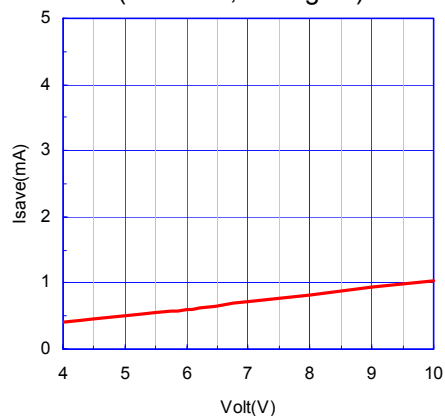
Voltage gain vs. Frequency
($V_{in}=1\text{MHz}, 1.0\text{Vp-p, non-LPF}$)



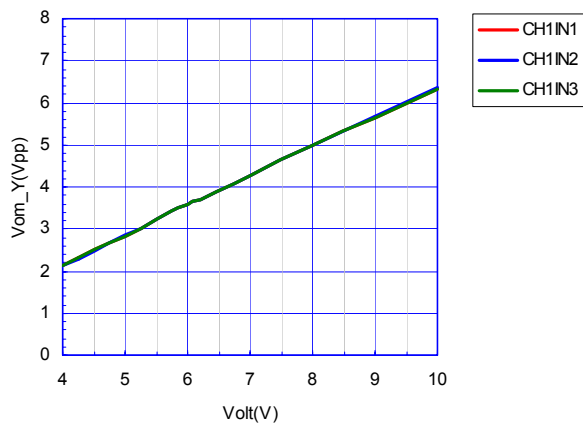
Operating current vs. Supply voltage
($T_a=25^\circ\text{C}$, No signal)



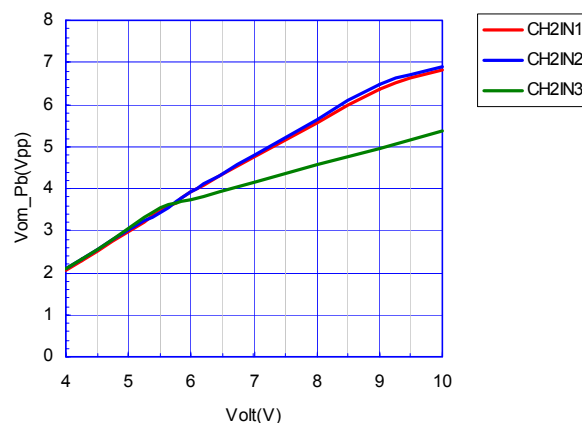
Operating current at Power save mode vs. Supply voltage
($T_a=25^\circ\text{C}$, No signal)



Maximum output level 1 vs. Supply voltage
($T_a=25^\circ\text{C}$, sync-tip clamp)

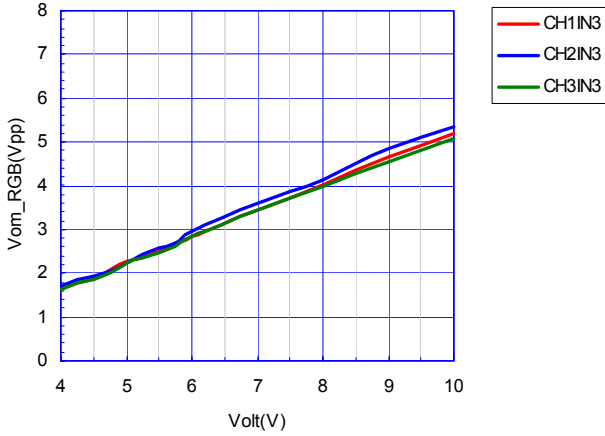


Maximum output level 2 vs. Supply voltage
($T_a=25^\circ\text{C}$, Pbin, bias)

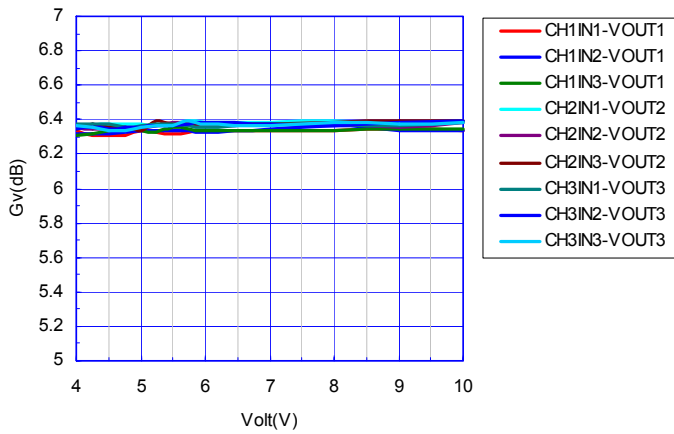


TYPICAL CHARACTERISTICS

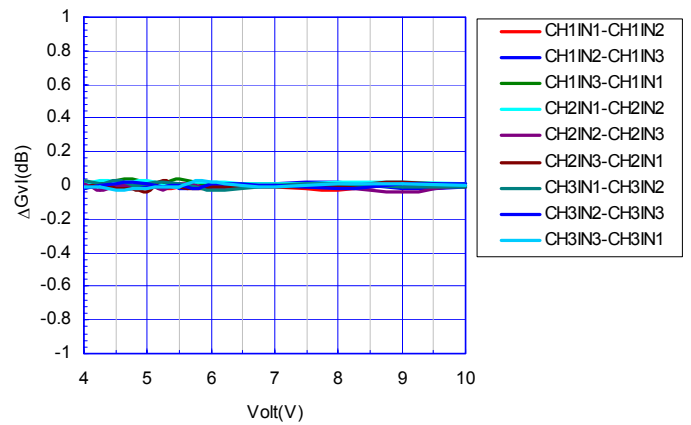
Maximum output level 3 vs. Supply voltage
($T_a=25^\circ\text{C}$, pedestal clamp)



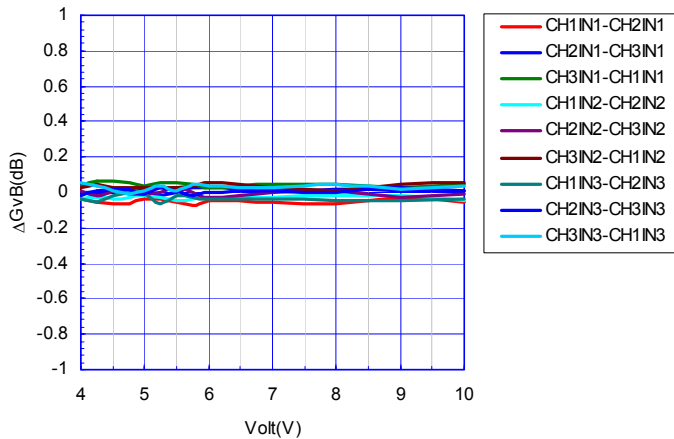
Voltage gain vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=1\text{MHz}$, 1.0Vp-p)



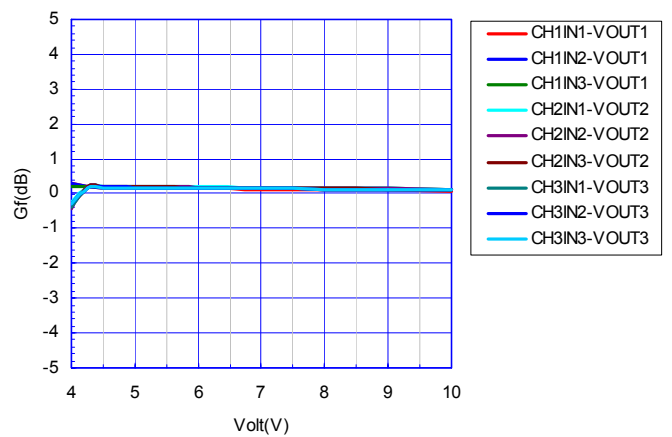
Voltage gain difference between input terminal
vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=1\text{MHz}$, 1.0Vp-p)



Voltage gain difference between channel
vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=1\text{MHz}$, 1.0Vp-p)

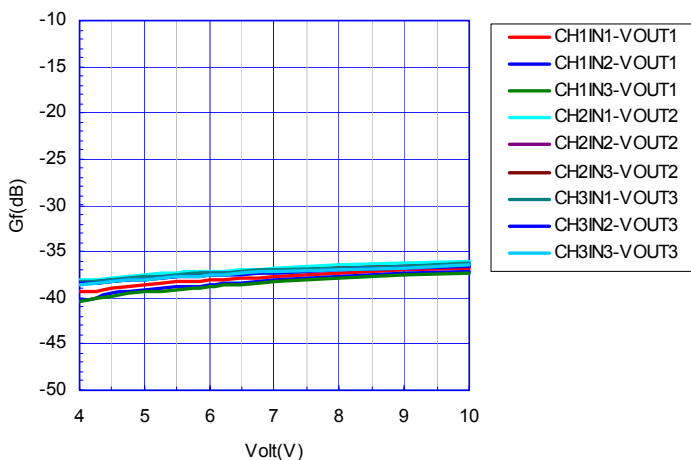


LPF vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=13.5\text{MHz}/1\text{MHz}$, 1.0Vp-p)

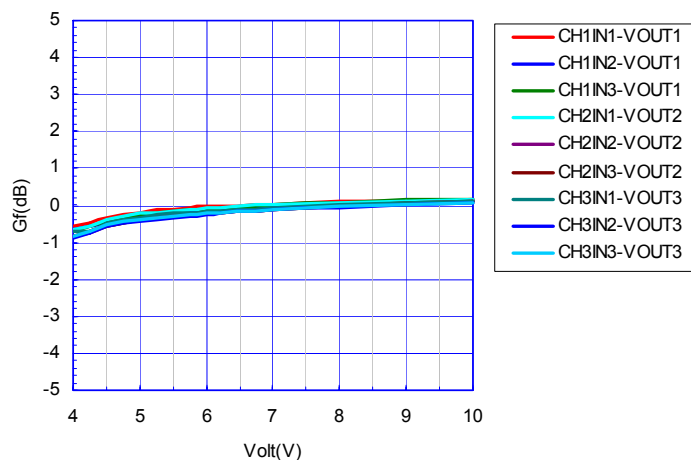


TYPICAL CHARACTERISTICS

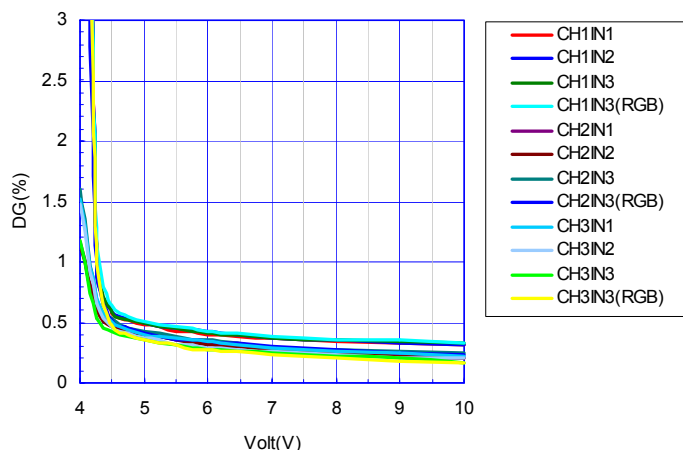
LPF vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=54\text{MHz}/1\text{MHz}$, 1.0Vp-p)



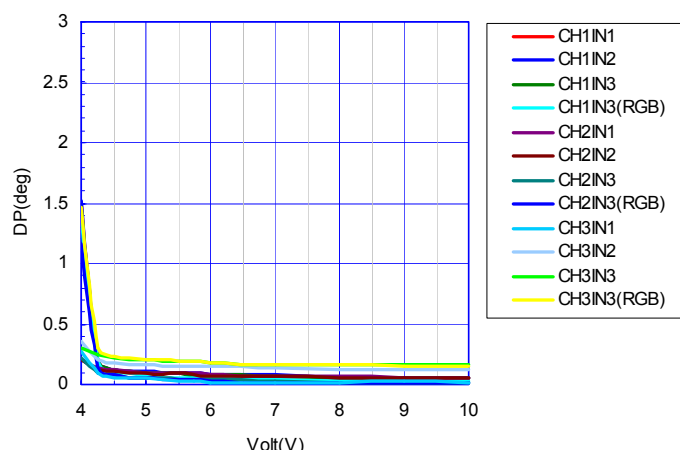
LPF vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=34\text{MHz}/1\text{MHz}$, 1.0Vp-p , non-LPF)



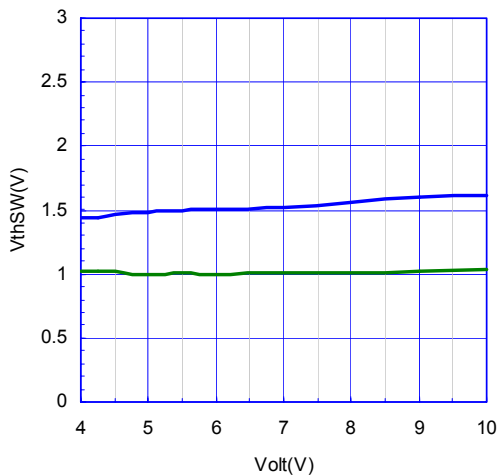
DG vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=1.0\text{Vp-p}$, 10STEP)



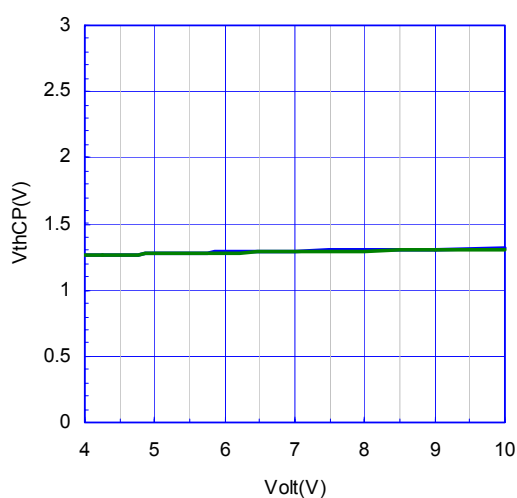
DP vs. Supply voltage
($T_a=25^\circ\text{C}$, $V_{in}=1.0\text{Vp-p}$, 10STEP)



SW voltage vs. Supply voltage
($T_a=25^\circ\text{C}$)

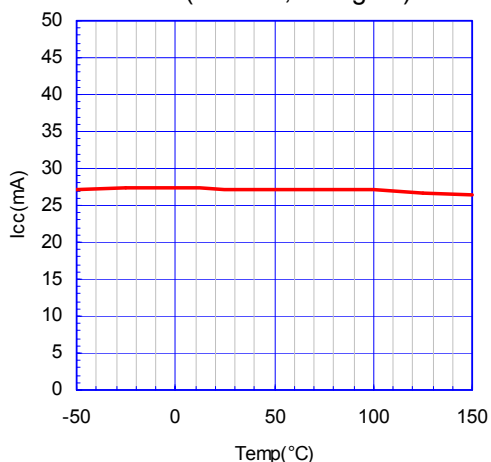


CP input level vs. Supply voltage
($T_a=25^\circ\text{C}$)

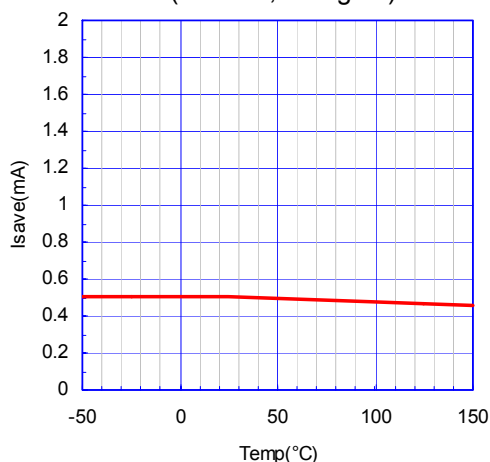


TYPICAL CHARACTERISTICS

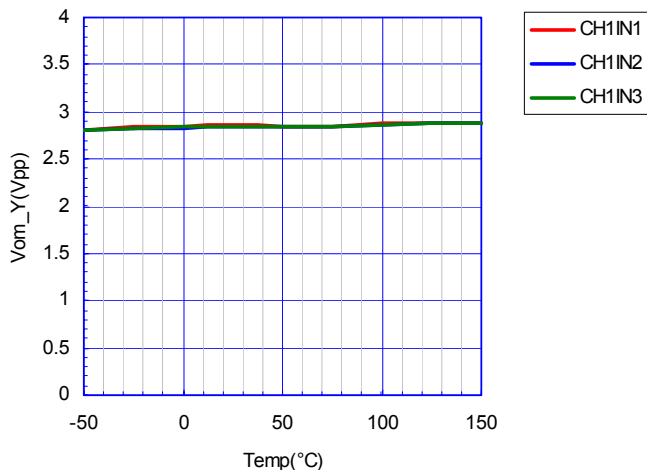
Operating current vs. Temperature
(Vcc=5V, No signal)



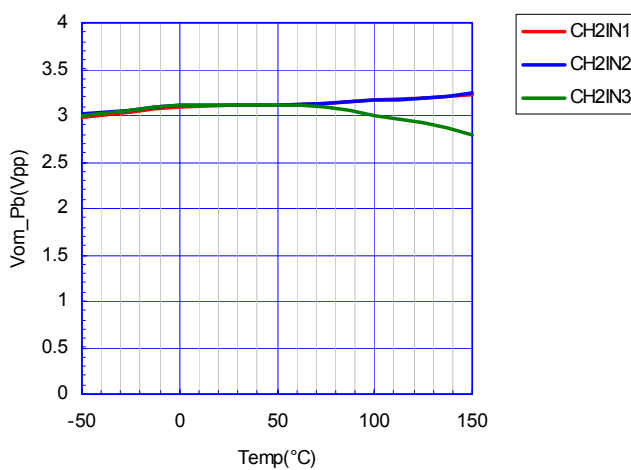
Operating current at Power save mode vs. Temperature
(Vcc=5V, No signal)



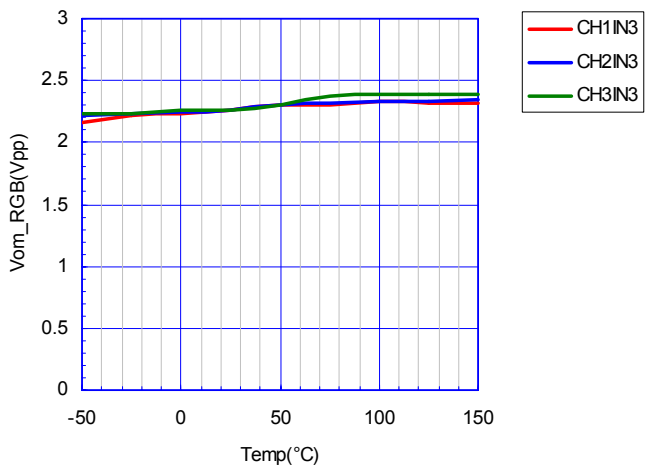
Maximum output level 1 vs. Temperature
(Vcc=5V, sync-tip clamp)



Maximum output level 2 vs. Temperature
(Vcc=5V, Pbin, Bias)

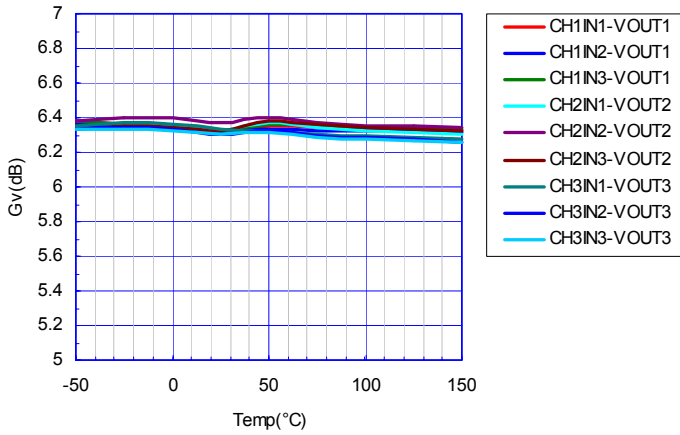


Maximum output level 3 vs. Temperature
(Vcc=5V, pedestal clamp)

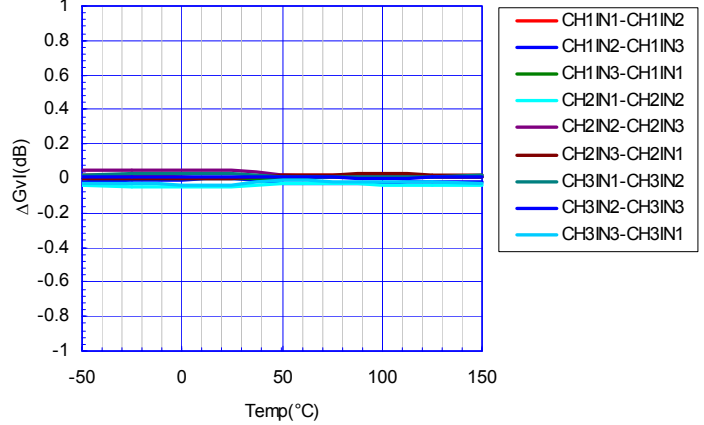


TYPICAL CHARACTERISTICS

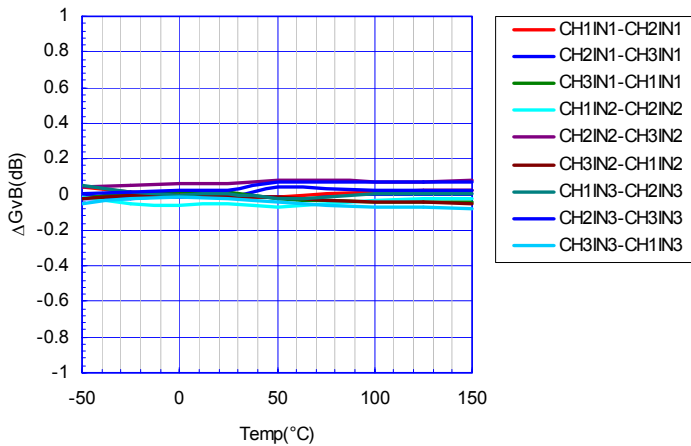
Voltage gain vs. Temperature
(Vcc=5V, Vin=1MHz, 1.0Vp-p)



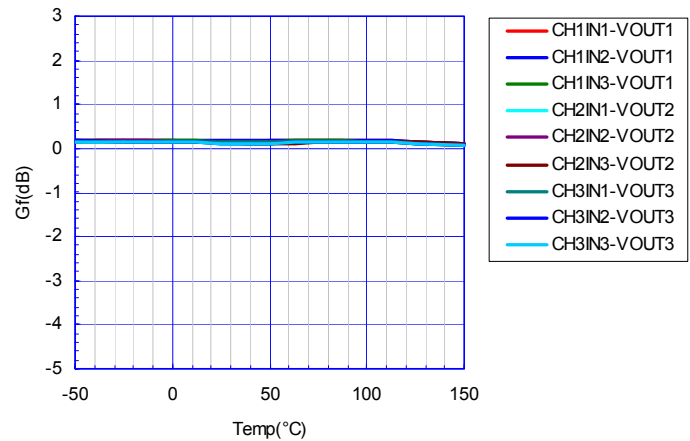
Voltage gain difference between input terminal
vs. Temperature
(Vcc=5V, Vin=1MHz, 1.0Vp-p)



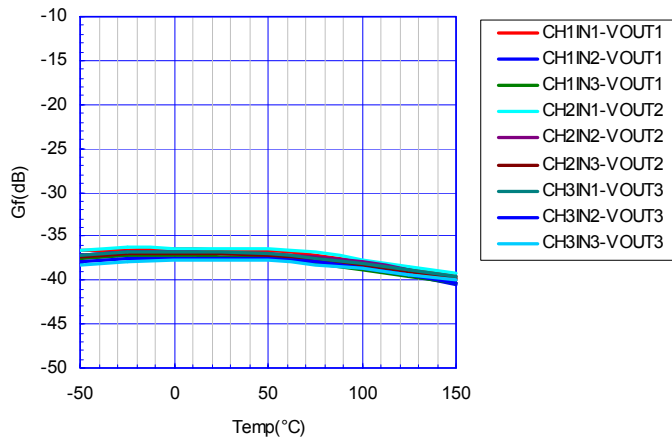
Voltage gain difference between channel
vs. Temperature
(Vcc=5V, Vin=1MHz, 1.0Vp-p)



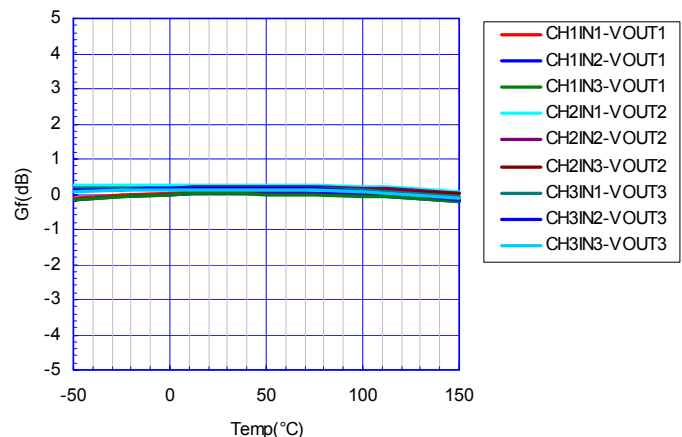
LPF vs. vs. Temperature
(Vcc=5V, Vin=13.5MHz/1MHz, 1.0Vp-p)



LPF vs. Temperature
(Vcc=5V, Vin=54MHz/1MHz, 1.0Vp-p)

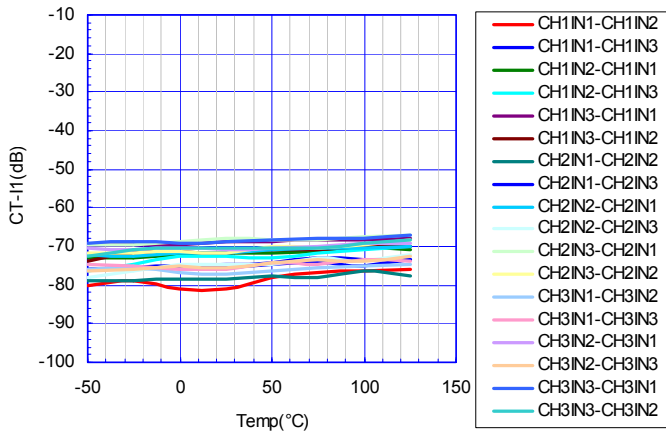


Frequency at LPF through mode vs. Temperature
(Vcc=5V, Vin= 34MHz/1MHz, 1.0Vp-p)

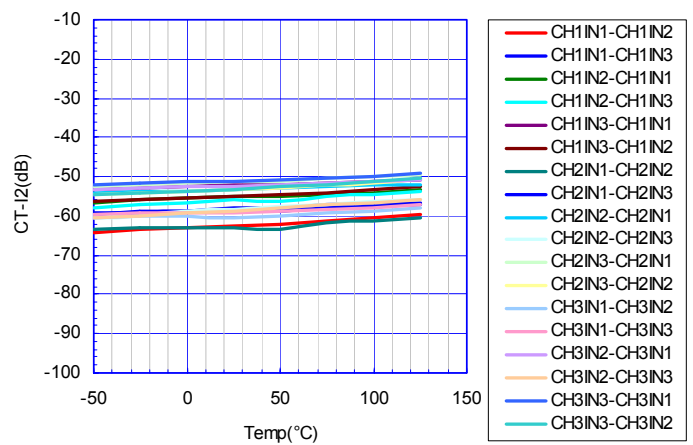


TYPICAL CHARACTERISTICS

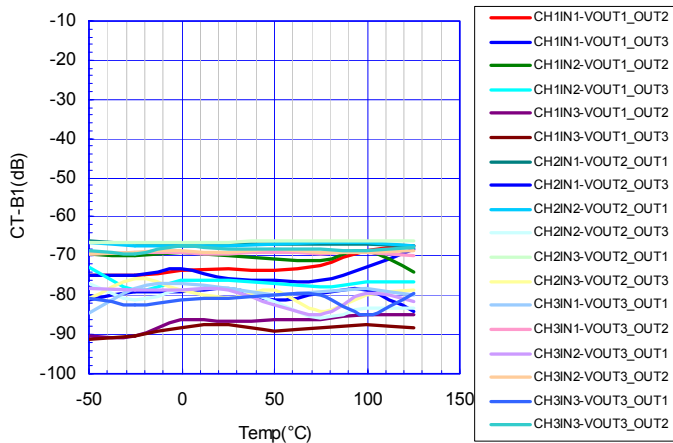
Cross talk vs. Temperature
(Vcc=5V, Vin=4.43MHz, 1.0Vp-p at input terminal)



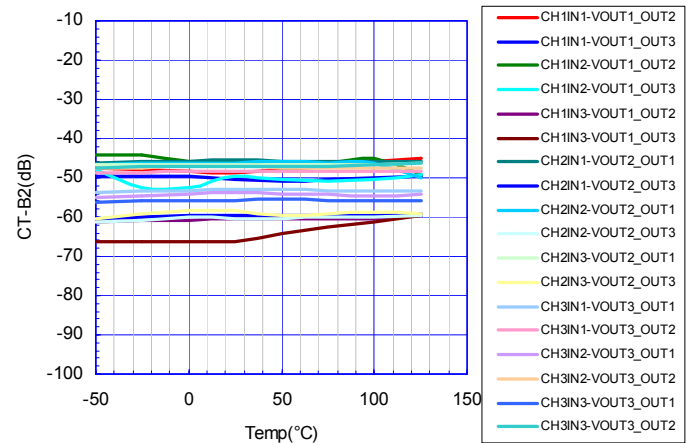
Cross talk vs. Temperature
(Vcc=5V, Vin=30MHz, 1.0Vp-p at input terminal)



Cross talk vs. Temperature
(Vcc=5V, Vin=4.43MHz, 1.0Vp-p at channel)



Cross talk vs. Temperature
(Vcc=5V, Vin=30MHz, 1.0Vp-p at channel)



[CAUTION]

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