

HIGH POWER SPDT SWITCH GaAs MMIC

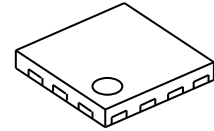
■ GENERAL DESCRIPTION

The NJG1814MD7 is a GaAs SPDT switch MMIC suitable for WLAN, LTE and 4G applications.

The NJG1814MD7 features very high isolation, low insertion loss, and excellent linearity performance at high frequency up to 6GHz. In addition, its high speed switching time is available for WLAN application. Integrated ESD protection device on each port achieves excellent ESD robustness. No DC blocking capacitors are required for all RF ports unless DC is biased externally.

The small and thin EQFN14-D7 package is adopted.

■ PACKAGE OUTLINE



NJG1814MD7

■ APPLICATIONS

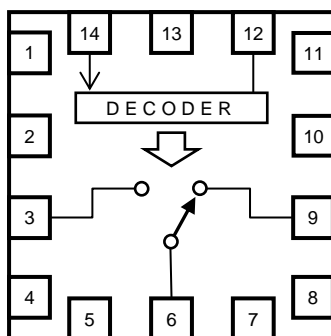
- IEEE 802.11a/b/g/n/ac applications
- LTE and LTE-U applications
- General Purpose Switching applications

■ FEATURES

- Low voltage logic control 1.35V to 5.0V
- High Isolation 42dB typ. @f=0.7GHz, P_{IN}=+27dBm
- 35dB typ. @f=2.0GHz, P_{IN}=+27dBm
- 34dB typ. @f=2.7GHz, P_{IN}=+27dBm
- 33dB typ. @f=5.85GHz, P_{IN}=+27dBm
- Low insertion loss 0.35dB typ. @f=0.7GHz, P_{IN}=+27dBm
- 0.38dB typ. @f=2.0GHz, P_{IN}=+27dBm
- 0.40dB typ. @f=2.7GHz, P_{IN}=+27dBm
- 0.45dB typ. @f=5.85GHz, P_{IN}=+27dBm
- +33dBm min.
- P_{-0.1dB} 200ns typ.
- High speed switching time
- Ultra small & thin package EQFN14-D7 (Package size: 1.6 x 1.6 x 0.397mm)
- RoHS compliant and Halogen Free, MSL1

■ PIN CONFIGURATION

(TOP VIEW)



Pin connection

- | | |
|------------|-------------|
| 1. GND | 8. GND |
| 2. NC(GND) | 9. P1 |
| 3. P2 | 10. GND |
| 4. GND | 11. GND |
| 5. GND | 12. VDD |
| 6. PC | 13. NC(GND) |
| 7. GND | 14. VCTL |

Exposed PAD: GND

■ TRUTH TABLE

“H”=V_{CTL(H)}, “L”=V_{CTL(L)}

| VCTL | Path |
|------|-------|
| H | PC-P1 |
| L | PC-P2 |

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS |
|-------------------|-----------|--|-------------|--------------------|
| RF Input Power | P_{IN} | $V_{DD}=3.3\text{V}$ | +33.5 | dBm |
| Supply Voltage | V_{DD} | | 5.0 | V |
| Control Voltage | V_{CTL} | | 5.0 | V |
| Power Dissipation | P_D | Four-layer FR4 PCB with through-hole (76.2x114.3mm), $T_j=150^{\circ}\text{C}$ | 1300 | mW |
| Operating Temp. | T_{opr} | | -40 to +105 | $^{\circ}\text{C}$ |
| Storage Temp. | T_{stg} | | -55 to +150 | $^{\circ}\text{C}$ |

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|--------------|-----------------------------------|------|-----|------|---------------|
| Supply Voltage | V_{DD} | | 2.5 | 3.3 | 5.0 | V |
| Operating Current | I_{DD} | No RF input, $V_{DD}=3.3\text{V}$ | - | 200 | 400 | μA |
| Control Voltage (LOW) | $V_{CTL(L)}$ | | 0 | - | 0.45 | V |
| Control Voltage (HIGH) | $V_{CTL(H)}$ | | 1.35 | 1.8 | 5.0 | V |
| Control Current | I_{CTL} | $V_{CTL(H)}=1.8\text{V}$ | - | 4 | 10 | μA |

■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_L=50\Omega$, $V_{DD}=3.3\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|---------------------|--|---------|------|------|-------|----|
| Insertion Loss 1 | LOSS1 | $f=0.7\text{GHz}$, $P_{IN}=+27\text{dBm}$ | - | 0.35 | 0.50 | dB | |
| Insertion Loss 2 | LOSS2 | $f=2.0\text{GHz}$, $P_{IN}=+27\text{dBm}$ | - | 0.38 | 0.53 | dB | |
| Insertion Loss 3 | LOSS3 | $f=2.7\text{GHz}$, $P_{IN}=+27\text{dBm}$ | - | 0.40 | 0.60 | dB | |
| Insertion Loss 4 | LOSS4 | $f=3.5\text{GHz}$, $P_{IN}=+27\text{dBm}$ | - | 0.42 | 0.62 | dB | |
| Insertion Loss 5 | LOSS5 | $f=5.85\text{GHz}$, $P_{IN}=+27\text{dBm}$ | - | 0.45 | 0.65 | dB | |
| Isolation 1 | ISL1 | $f=0.7\text{GHz}$, $P_{IN}=+27\text{dBm}$ | 39 | 42 | - | dB | |
| Isolation 2 | ISL2 | $f=2.0\text{GHz}$, $P_{IN}=+27\text{dBm}$ | 32 | 35 | - | dB | |
| Isolation 3 | ISL3 | $f=2.7\text{GHz}$, $P_{IN}=+27\text{dBm}$ | 31 | 34 | - | dB | |
| Isolation 4 | ISL4 | $f=3.5\text{GHz}$, $P_{IN}=+27\text{dBm}$ | 30 | 33 | - | dB | |
| Isolation 5 | ISL5 | $f=5.85\text{GHz}$ $P_{IN}=+27\text{dBm}$ | PC-Pn*1 | 30 | 33 | - | dB |
| | | | Pm-Pn*2 | 25 | 27 | - | dB |
| Input Power at 0.1dB Compression Point | $P_{-0.1\text{dB}}$ | $f=5.85\text{GHz}$ | +33 | - | - | dBm | |
| 2nd Harmonics | 2fo | $f=5.18\text{GHz}$, 5.85GHz , $P_{IN}=+27\text{dBm}$ | - | - | -70 | dBc | |
| 3rd Harmonics | 3fo | $f=5.18\text{GHz}$, 5.85GHz , $P_{IN}=+27\text{dBm}$ | - | - | -70 | dBc | |
| 4th Harmonics | 4fo | $f=5.18\text{GHz}$, 5.85GHz , $P_{IN}=+27\text{dBm}$ | - | - | -70 | dBc | |
| Input 2nd order intercept point | IIP2 | $f=2.48+2.69\text{GHz}$, $f_{\text{meas}}=5.17\text{GHz}$, $P_{IN}=+10\text{dBm}$ each | +100 | - | - | dBm | |
| Input 3rd order intercept point | IIP3 | $f=1.71+2.40\text{GHz}$, $f_{\text{meas}}=5.82\text{GHz}$, $P_{IN}=+10\text{dBm}$ each | +60 | - | - | dBm | |
| VSWR1 | VSWR1 | On-state ports, $f=2.7\text{GHz}$ | - | 1.1 | 1.5 | | |
| VSWR2 | VSWR2 | On-state ports, $f=5.85\text{GHz}$ | - | 1.1 | 1.5 | | |
| Switching time | T_{SW} | 50% V_{CTL} to 10/90% RF | - | 200 | 400 | ns | |

*1: $P_n=P_1, P_2$.

*2: $P_m=P_1, P_2$. $P_n=P_1, P_2$. $m \neq n$

■ TERMINAL INFORMATION

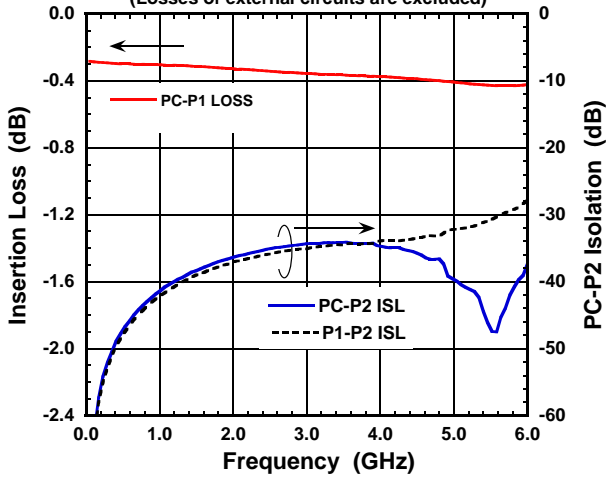
| No. | SYMBOL | DESCRIPTION |
|-------------|---------|---|
| 1 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 2 | NC(GND) | No connected terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 3 | P2 | RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. |
| 4 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 5 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 6 | PC | RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. Please connect an inductor with GND terminal for ESD protection. |
| 7 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 8 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 9 | P1 | RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. |
| 10 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 11 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 12 | VDD | Positive voltage supply terminal. The positive voltage (+2.5 to +5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance. |
| 13 | NC(GND) | No connected terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 14 | VCTL | Control signal input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V). |
| Exposed Pad | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |

■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

Loss, ISL vs. Frequency

(PC-P1 ON, $V_{DD}=3.3V$, $V_{CTL(H)}=1.8V$)

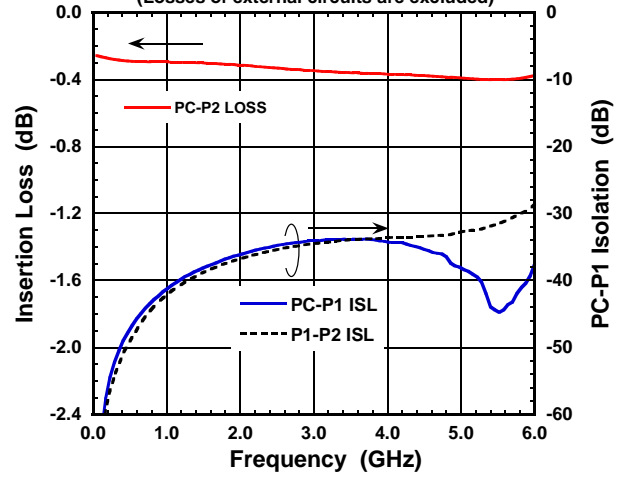
(Losses of external circuits are excluded)



Loss, ISL vs. Frequency

(PC-P2 ON, $V_{DD}=3.3V$, $V_{CTL(L)}=0V$)

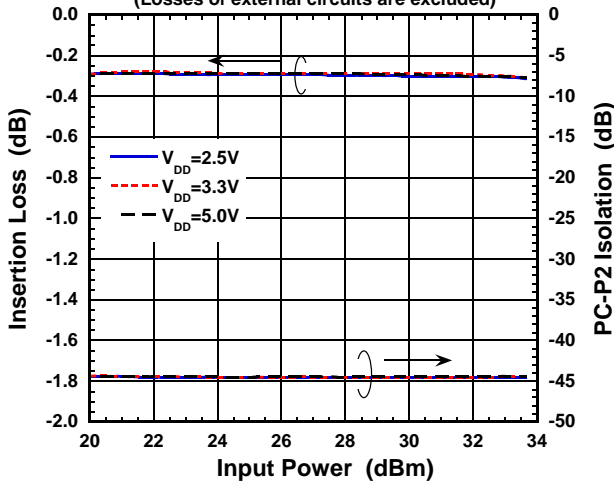
(Losses of external circuits are excluded)



Loss, ISL vs. Input Power

($f=0.7GHz$, PC-P1 ON, $V_{CTL(H)}=1.8V$)

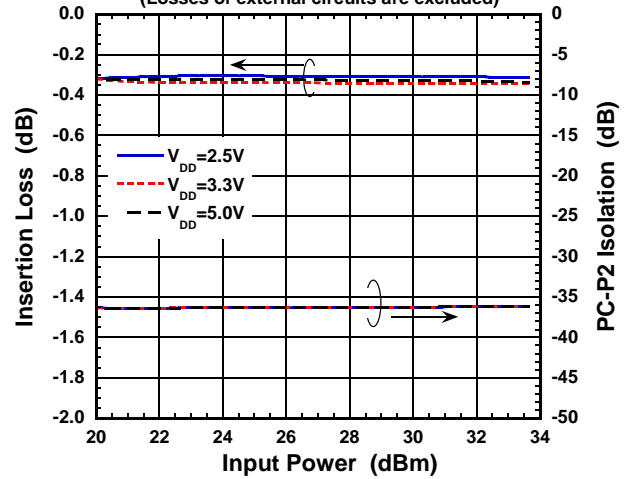
(Losses of external circuits are excluded)



Loss, ISL vs. Input Power

($f=2.0GHz$, PC-P1 ON, $V_{CTL(H)}=1.8V$)

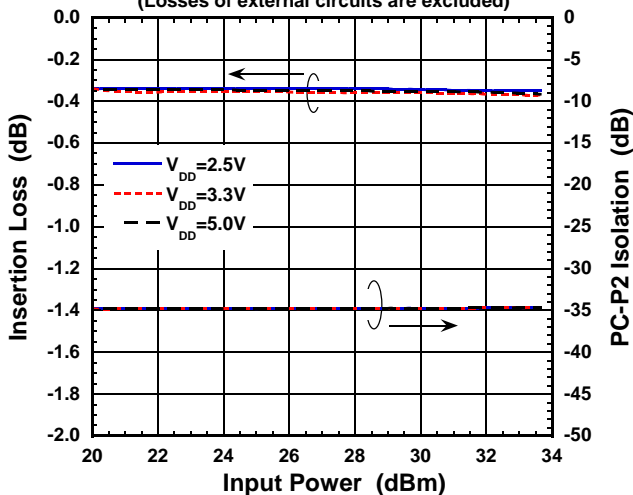
(Losses of external circuits are excluded)



Loss, ISL vs. Input Power

($f=2.7GHz$, PC-P1 ON, $V_{CTL(H)}=1.8V$)

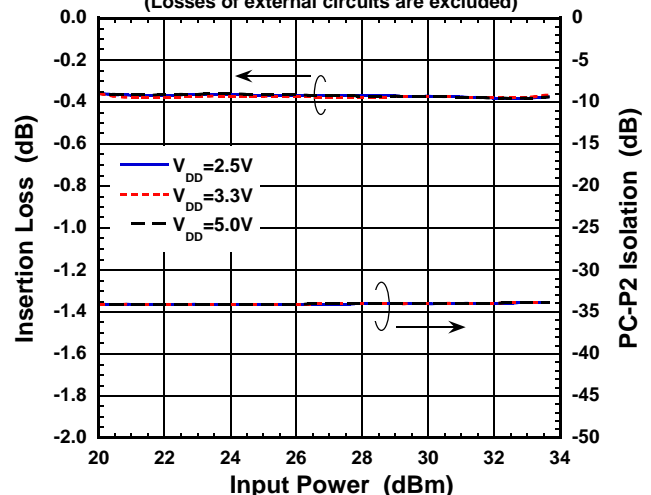
(Losses of external circuits are excluded)



Loss, ISL vs. Input Power

($f=3.5GHz$, PC-P1 ON, $V_{CTL(H)}=1.8V$)

(Losses of external circuits are excluded)

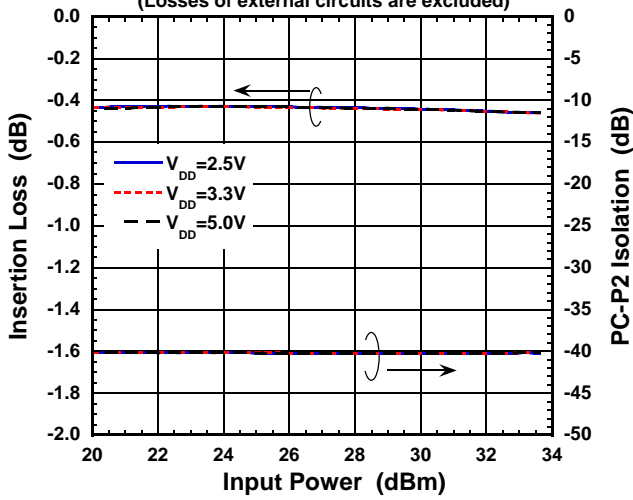


■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

Loss, ISL vs. Input Power

(f=5.85GHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)

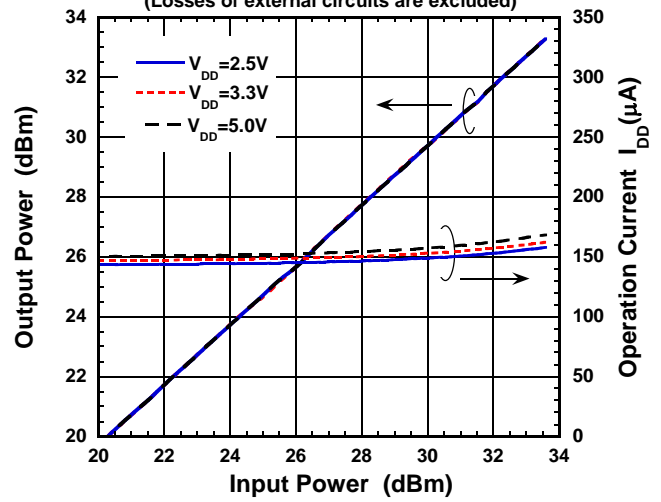
(Losses of external circuits are excluded)



Output Power, I_{DD} vs. Input Power

(f=0.7GHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)

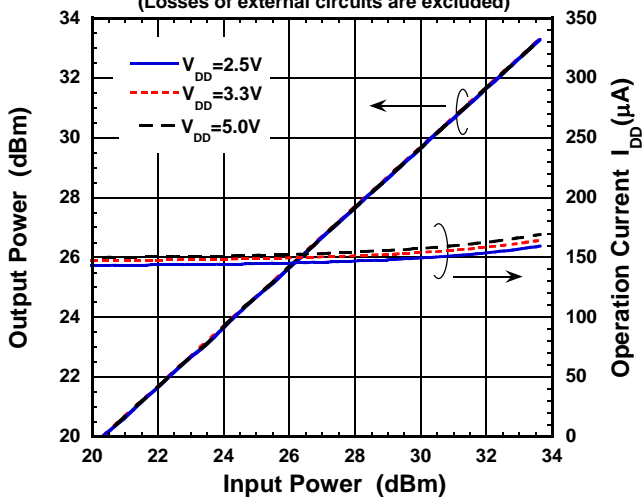
(Losses of external circuits are excluded)



Output Power, I_{DD} vs. Input Power

(f=2.0GHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)

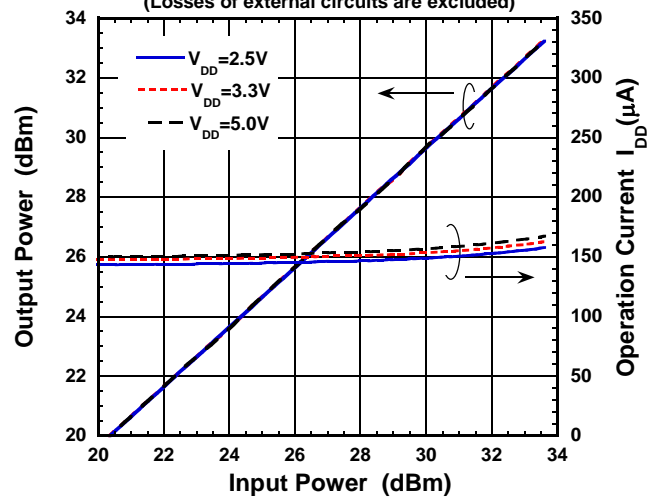
(Losses of external circuits are excluded)



Output Power, I_{DD} vs. Input Power

(f=2.7GHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)

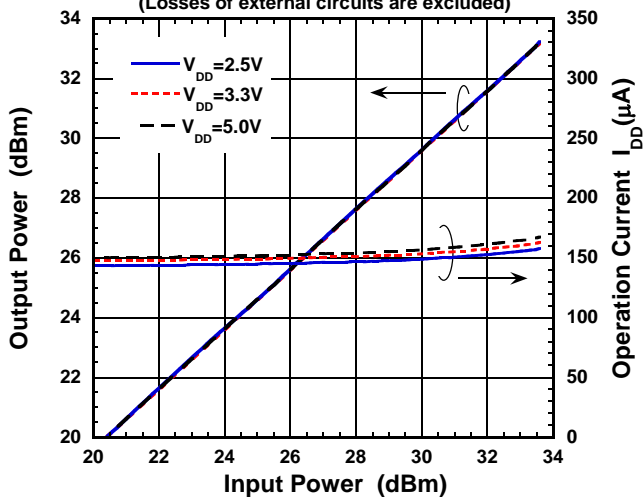
(Losses of external circuits are excluded)



Output Power, I_{DD} vs. Input Power

(f=3.5GHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)

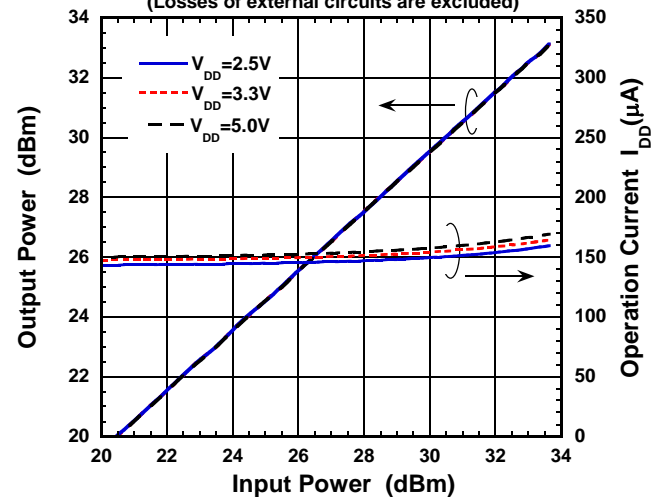
(Losses of external circuits are excluded)



Output Power, I_{DD} vs. Input Power

(f=5.85GHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)

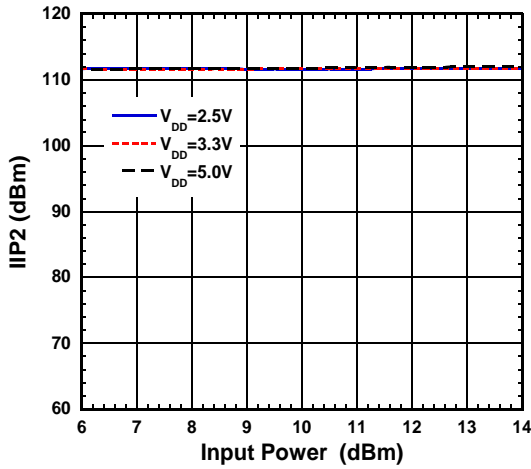
(Losses of external circuits are excluded)



■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

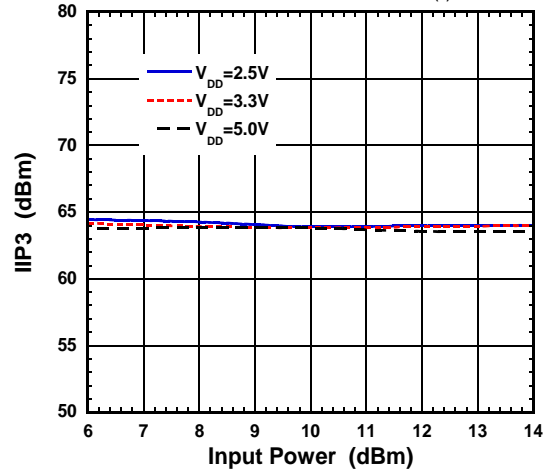
IIP2 vs. Input Power

(f=2480MHz+2690MHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)



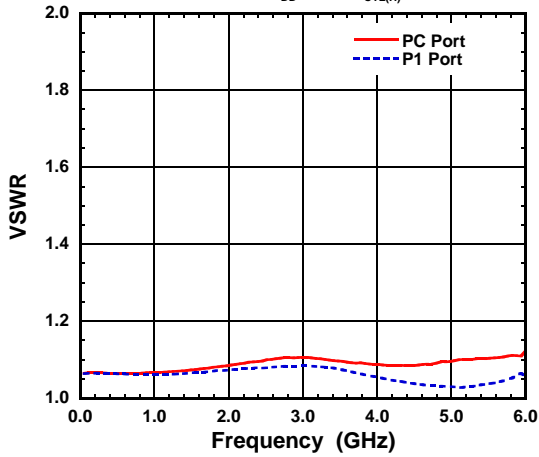
IIP3 vs. Input Power

(f=1710MHz+2400MHz, PC-P1 ON, $V_{CTL(H)}=1.8V$)



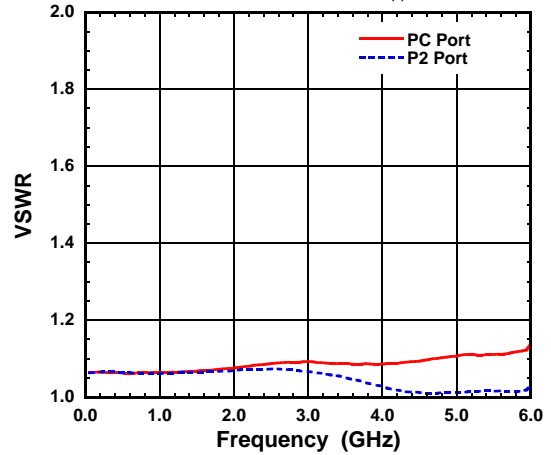
VSWR vs. Frequency

(PC-P1 ON, $V_{DD}=3.3V$, $V_{CTL(H)}=1.8V$)



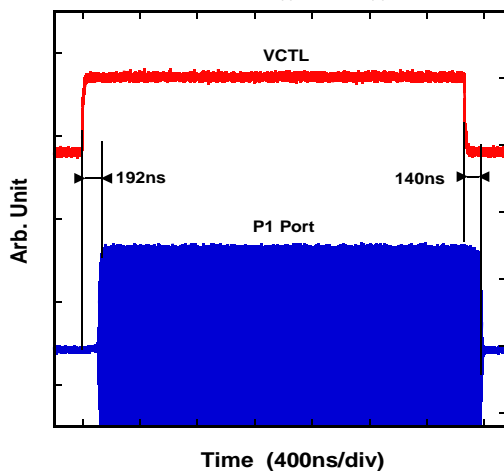
VSWR vs. Frequency

(PC-P2 ON, $V_{DD}=3.3V$, $V_{CTL(L)}=0V$)



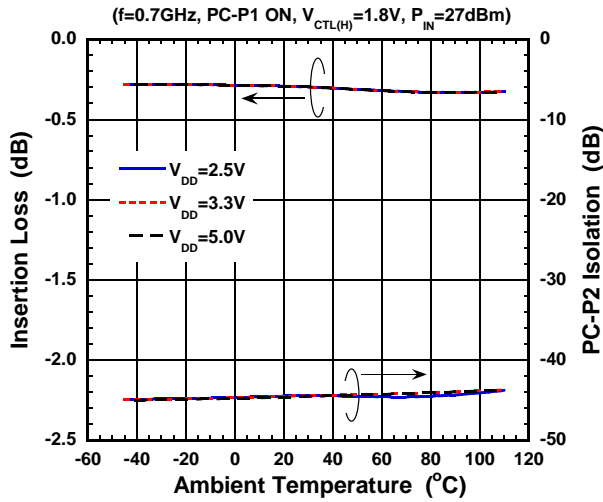
Switching Time

($V_{DD}=3.3V$, $V_{CTL(L)}=0V$, $V_{CTL(H)}=1.8V$)

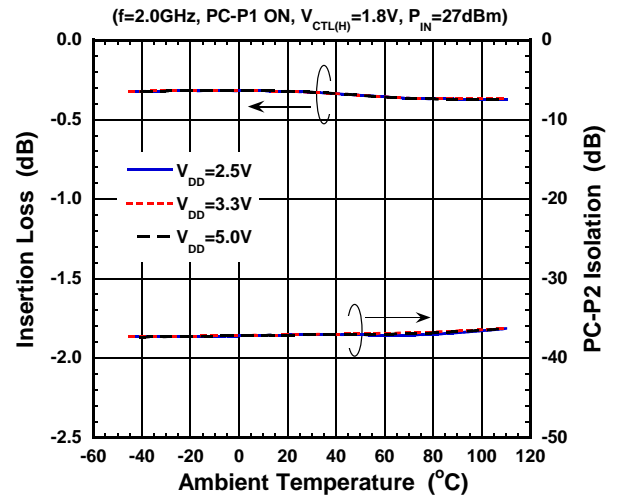


■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

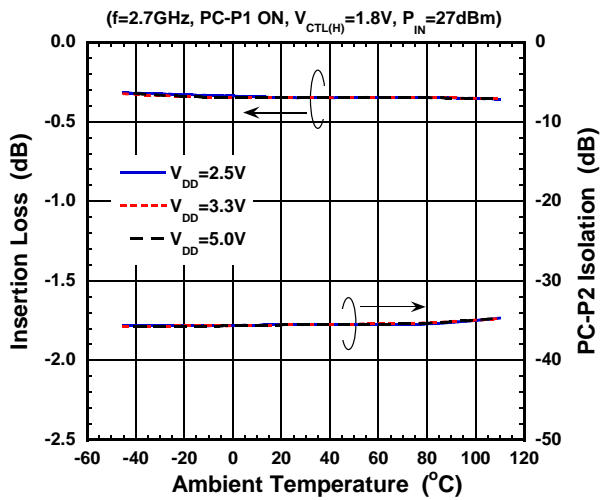
Loss, ISL vs. Ambient Temperature



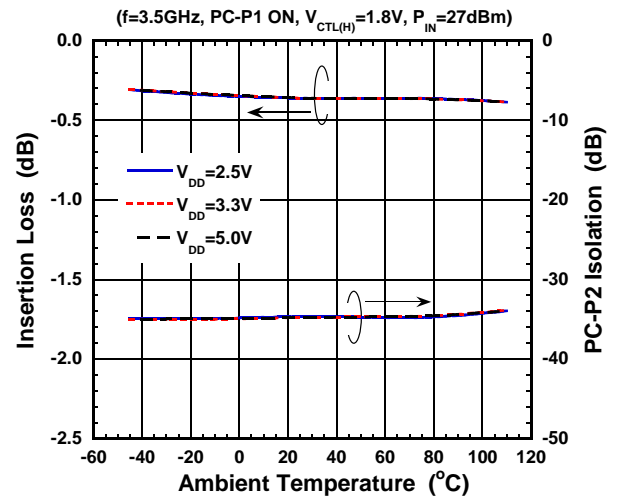
Loss, ISL vs. Ambient Temperature



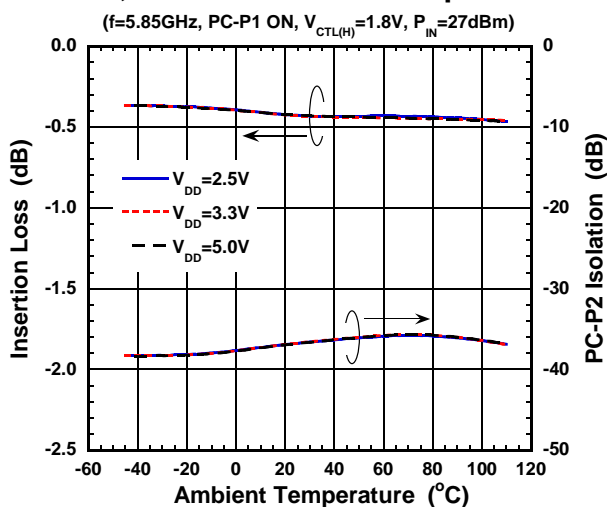
Loss, ISL vs. Ambient Temperature



Loss, ISL vs. Ambient Temperature



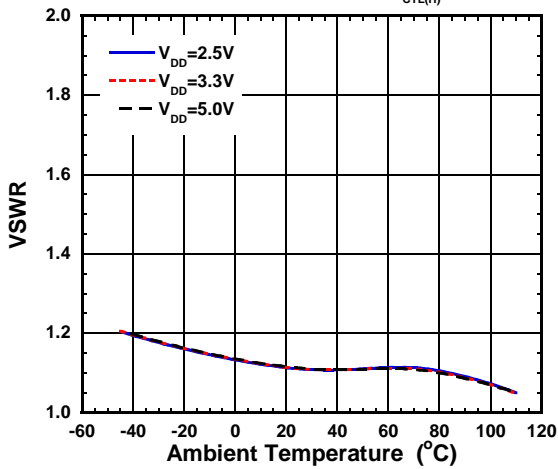
Loss, ISL vs. Ambient Temperature



■ ELECTRICAL CHARACTERISTICS (With application circuit, loss of external circuit are excluded.)

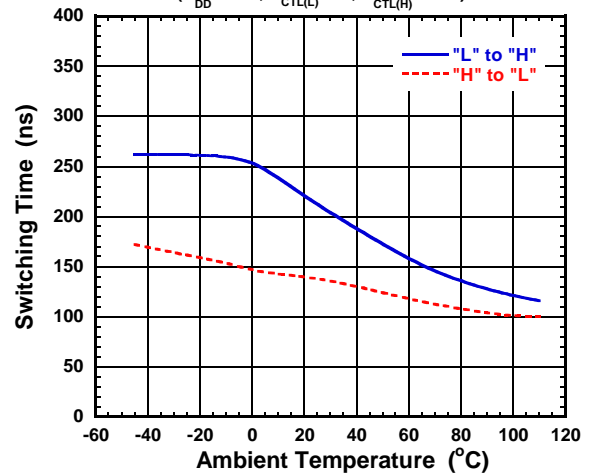
VSWR vs Ambient Temperature

(f=5850MHz, PC Port, PC-P1 ON, $V_{CTL(H)}=1.8V$)



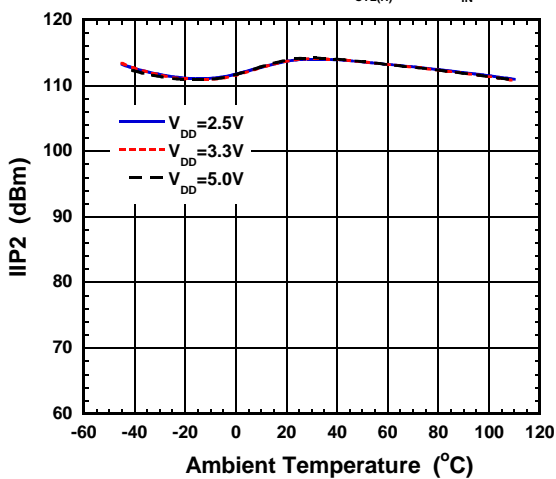
Switching Time vs. Ambient Temperature

($V_{DD}=3.3V$, $V_{CTL(L)}=0V$, $V_{CTL(H)}=1.8V$)



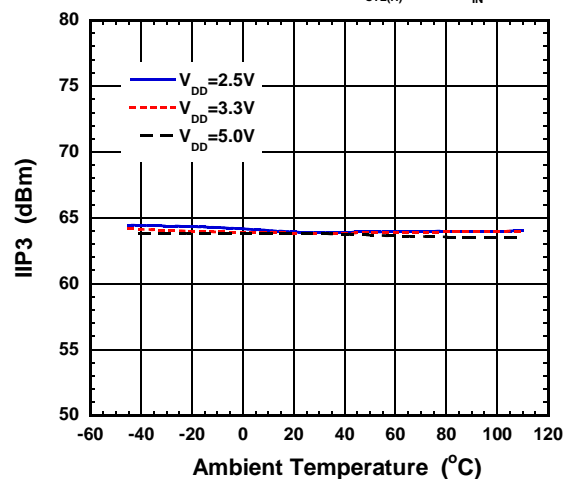
IIP2 vs. Ambient Temperature

(f=2480MHz+2690MHz, PC-P1 ON, $V_{CTL(H)}=1.8V$, $P_{IN}=10dBm$)



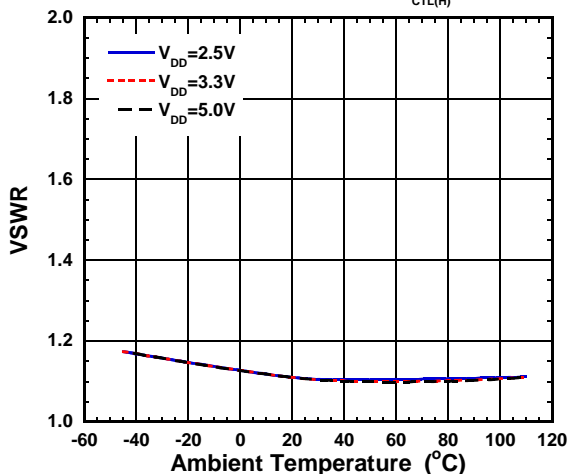
IIP3 vs. Ambient Temperature

(f=1710MHz+2400MHz, PC-P1 ON, $V_{CTL(H)}=1.8V$, $P_{IN}=10dBm$)



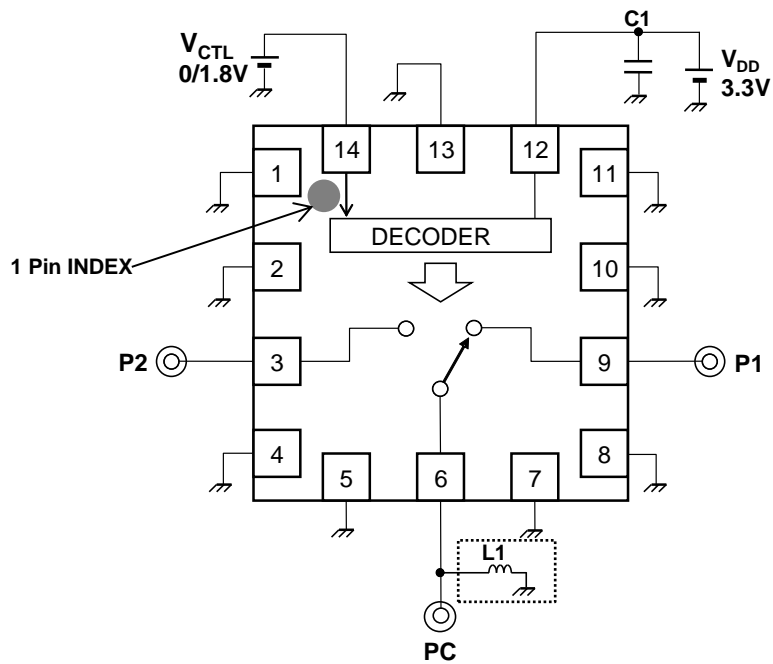
VSWR vs Ambient Temperature

(f=2700MHz, PC Port, PC-P1 ON, $V_{CTL(H)}=1.8V$)



APPLICATION CIRCUIT

(TOP VIEW)



Note:

[1] No DC blocking capacitors are required on all RF ports, unless DC is biased externally.

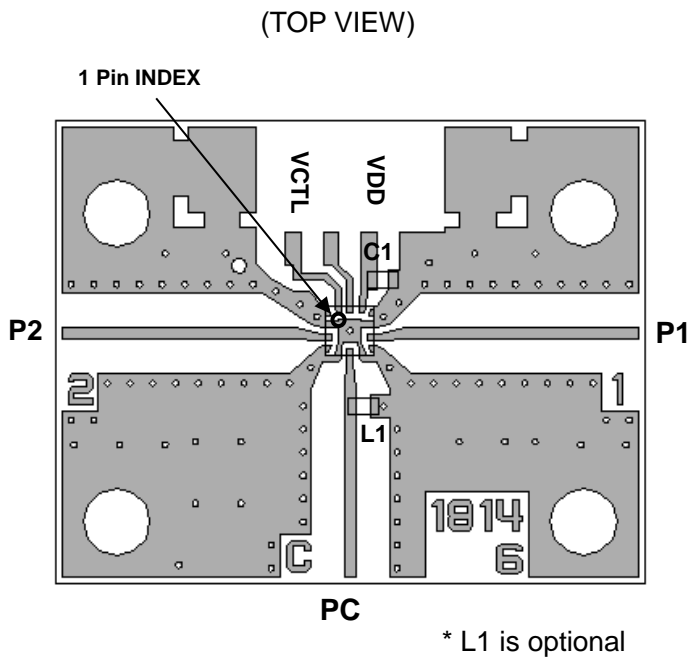
[2] The inductor L1 is optional in order to achieve enhancing ESD protection level.

[3] L1 is also recommended in order to keep the DC bias level of each RF port at 0V level tightly.

PARTS LIST

| No. | Parameters | Note |
|-----|------------|----------------------|
| C1 | 1000pF | MURATA (GRM15) |
| L1 | 56nH | TAIYO-YUDEN (HK1005) |

PCB LAYOUT



PCB size: 19.4 x 15.0 mm
 PCB: FR-4, t=0.2mm
 Micro strip line width: 0.38mm

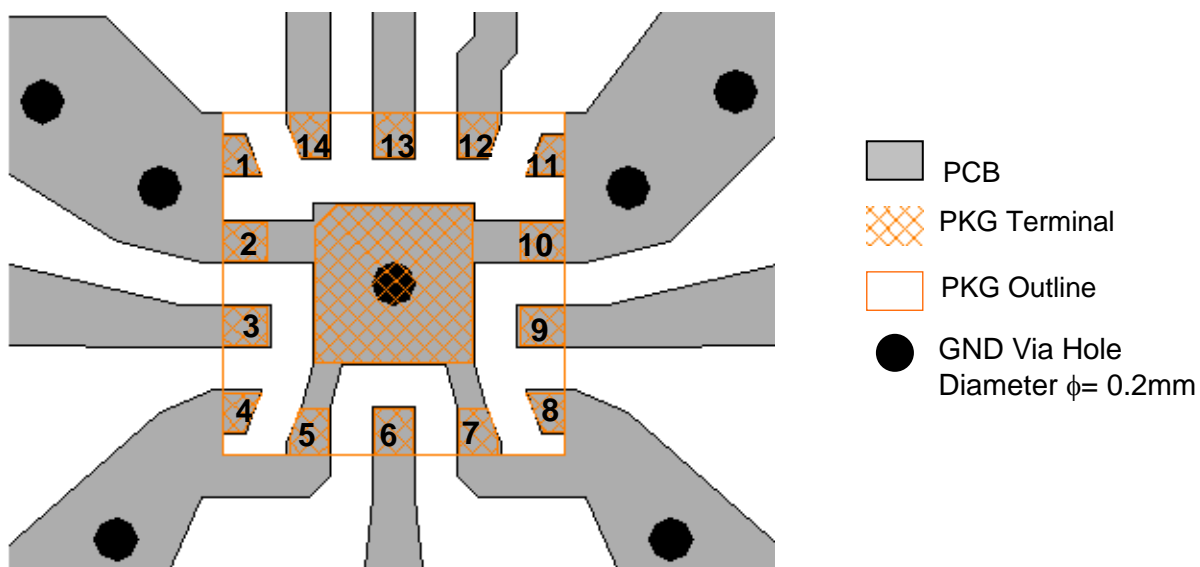
Losses of PCB and connectors, Ta=+25°C

| Frequency (GHz) | Loss (dB) |
|-----------------|-----------|
| 0.7 | 0.18 |
| 2.0 | 0.31 |
| 2.7 | 0.35 |
| 3.5 | 0.42 |
| 5.85 | 0.66 |




PRECAUTIONS

- [1] No DC blocking capacitors are required at each RF port normally. When the other device is biased at certain voltage and connected to the NJG1814MD7, a DC blocking capacitor is required between the device and the switch IC. This is because the each RF port of NJG1814MD7 is biased at 0V (GND).
- [2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal.
- [3] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through - holes for ground should be placed the IC near.

PCB LAYOUT GUIDELINE (EQFN14-D7)

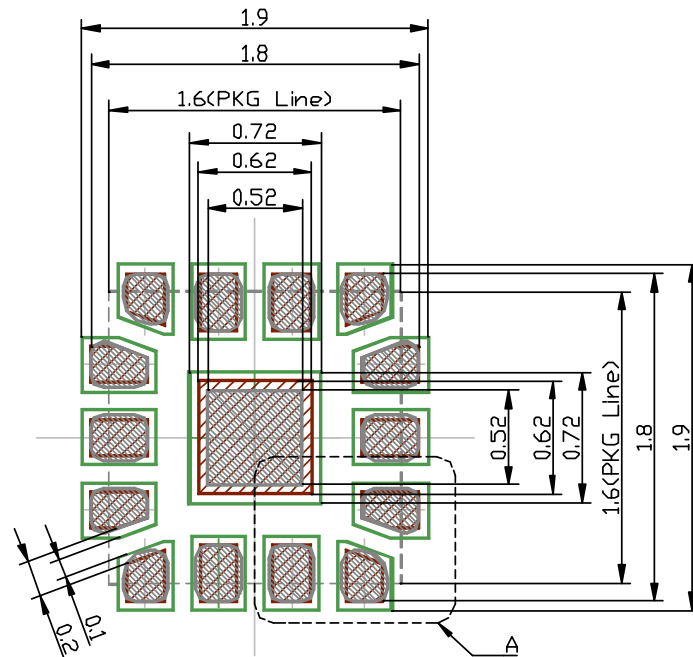


RECOMMENDED FOOTPRINT PATTERN (EQFN14-D7 PACKAGE Reference)

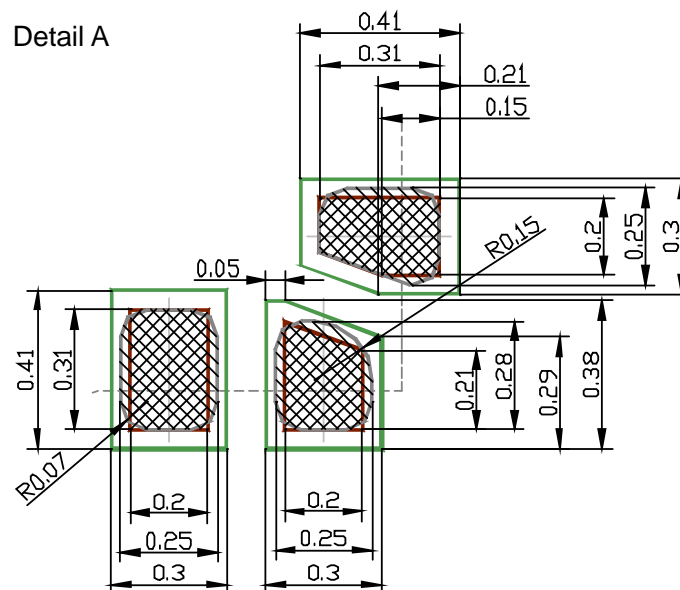
-  :Land
-  :Mask (Open area) *Metal mask thickness : 100μm
-  :Resist(Open area)

PKG: 1.6mm x 1.6mm
Pin pitch: 0.4mm

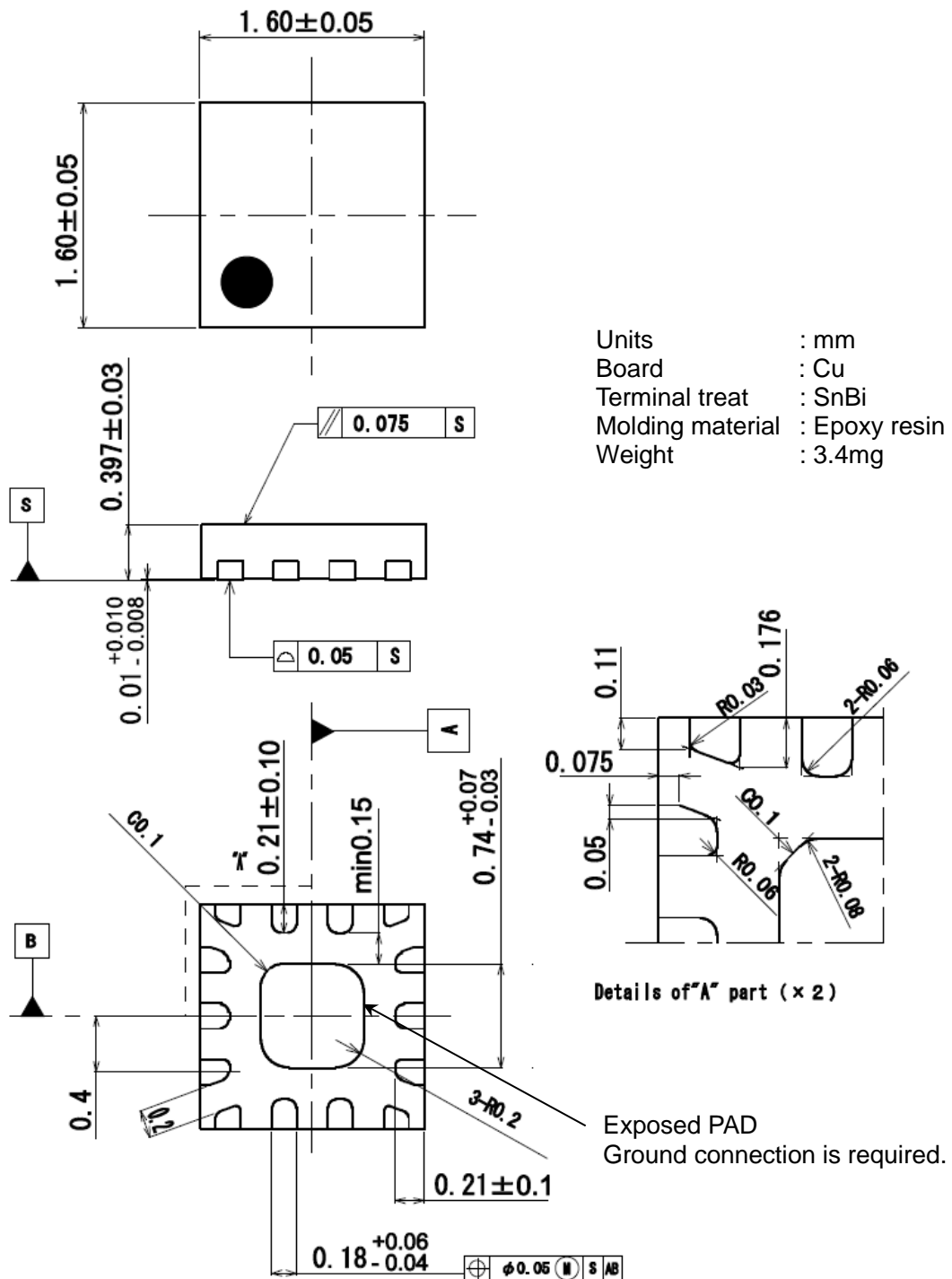
Units : mm



Detail A



■ PACKAGE OUTLINE (EQFN14-D7)



Cautions on using this product

- This product contains Gallium-Arsenide (GaAs) which is a harmful material.
- Do NOT eat or put into mouth.
 - Do NOT dispose in fire or break up this product.
 - Do NOT chemically make gas or powder with this product.
 - To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.