

High Isolation X-SP3T (DP6T) SWITCH

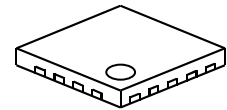
■ GENERAL DESCRIPTION

The NJG1683ME7 is a GaAs X (cross) - SP3T (DP6T) switch MMIC for switching of balanced (differential) triple band filters, upper pin compatible for NJG1655ME7. It features low insertion loss and very high isolation for balanced signal input which makes it much suited for balanced filter switching.

The ESD protection circuits are integrated in the IC to achieve high ESD tolerance.

The ultra-small and ultra-thin EQFN18-E7 package is adopted.

■ PACKAGE OUTLINE



NJG1683ME7

*) The X-SP3T is a paired SP3T switch that features two identical SP3T switches being integrated into one chip. The two SP3T switches are controlled synchronously, and their respective RF lines cross each other on the chip.

■ APPLICATIONS

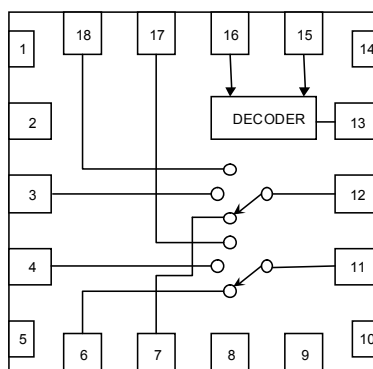
Switching of balanced type filters (Triple band) application
Suitable for 3G and LTE application

■ FEATURES

- Low operation voltage $V_{DD}=1.5\sim 4.5V$
- Low control voltage $V_{CTL(H)}=1.8V$ typ.
- High isolation (Balanced mode)
 - 55dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 47dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 45dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Low insertion loss
 - 0.35dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 0.45dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 0.60dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Small package EQFN18-E7 (Package size: 2.0mm x 2.0mm x 0.397mm typ.)
- RoHS compliant and Halogen Free
- MSL1

■ PIN CONFIGURATION

(Top View)



Pin connection

- | | |
|------------|-----------|
| 1. GND | 10. GND |
| 2. NC(GND) | 11. PCB |
| 3. P2A | 12. PCA |
| 4. P2B | 13. VDD |
| 5. GND | 14. GND |
| 6. P1B | 15. VCTL2 |
| 7. P1A | 16. VCTL1 |
| 8. GND | 17. P3B |
| 9. NC(GND) | 18. P3A |

■ TRUTH TABLE

ON PATH	"H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$	
	VCTL1	VCTL2
PCA-P1A PCB-P1B	H	L
PCA-P2A PCB-P2B	L	L
PCA-P3A PCB-P3B	L	H

NOTE: The information on this datasheet is subject to change without notice.

NJG1683ME7

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	$V_{DD}=2.7\text{V}$, $V_{CTL}=0\text{V}/1.8\text{V}$	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL1, VCTL2 terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (101.5x114.5mm), $T_j=150^{\circ}\text{C}$	1400	mW
Operating Temp.	T_{opr}		-40~+90	$^{\circ}\text{C}$
Storage Temp.	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

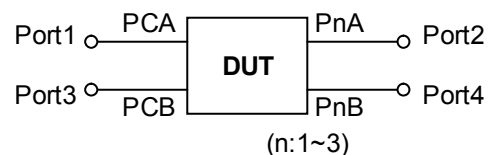
(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.5	2.7	4.5	V
Operating Current	I_{DD}		-	20	40	μA
Control Voltage (LOW)	$V_{CTL(L)}$		0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.35	1.8	4.5	V
Control Current	I_{CTL}		-	2	8	μA
Insertion Loss 1	LOSS1	$f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.35	0.55	dB
Insertion Loss 2	LOSS2	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.45	0.70	dB
Insertion Loss 3	LOSS3	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.60	0.85	dB
Balanced mode isolation 1 ^(Note1)	B-ISL1	$f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$ PC-P1,P2,P3	50	55	-	dB
Balanced mode isolation 2 ^(Note1)	B-ISL2	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$ PC-P1,P2,P3	42	47	-	dB
Balanced mode isolation 3 ^(Note1)	B-ISL3	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$ PC-P1,P2,P3	40	45	-	dB
Isolation 1	ISL1	$f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$ PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	28	31	-	dB
Isolation 2	ISL2	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$ PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	22	25	-	dB
Isolation 3	ISL3	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$ PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	18	21	-	dB
Isolation 4	ISL4	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$, PCA-PCB	15	18	-	dB
Input Power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2.0\text{GHz}$	19	23	-	dBm
VSWR	VSWR	$f=2.0\text{GHz}$, on state	-	1.2	1.5	
Switching Time	T_{sw}	50% V_{CTL} to 10%/90% RF	-	2	5	μs

Note1:

In application circuit, Calculation of "Balanced Mode Isolation" uses following formula.

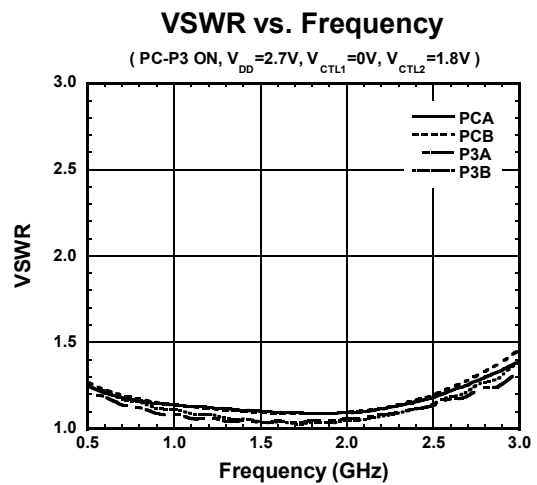
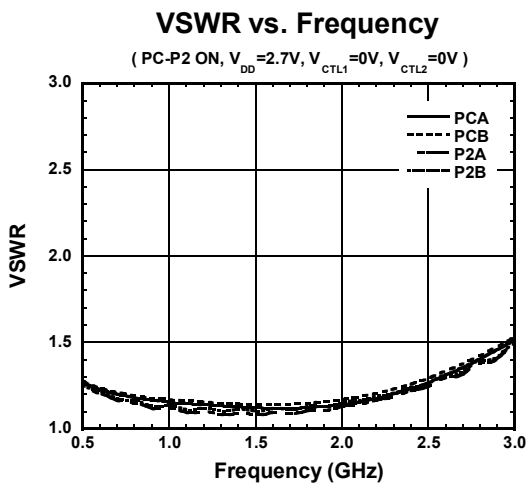
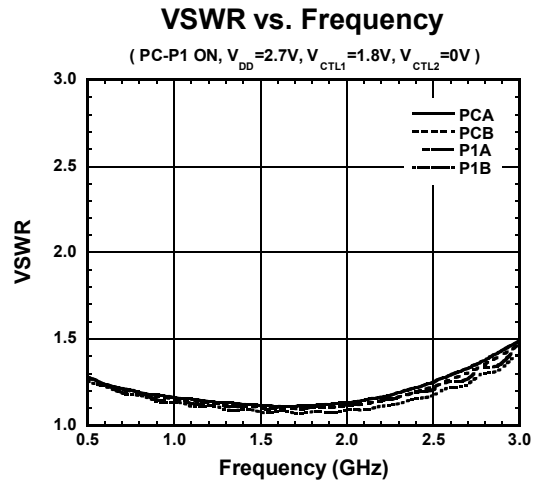
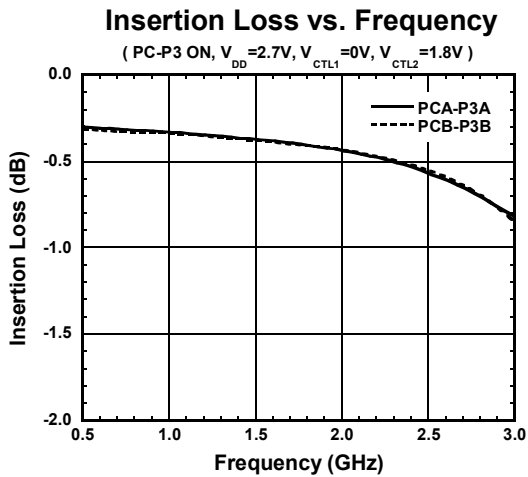
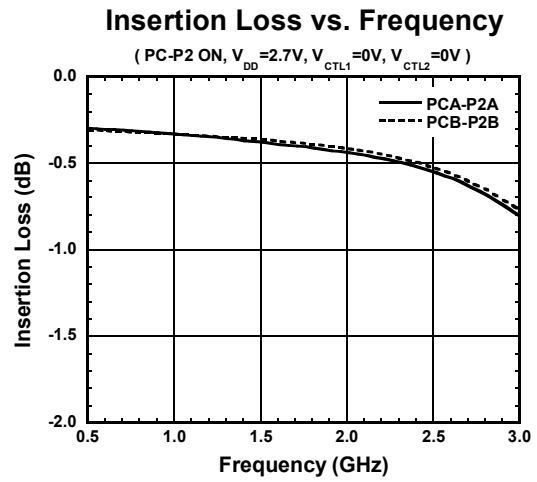
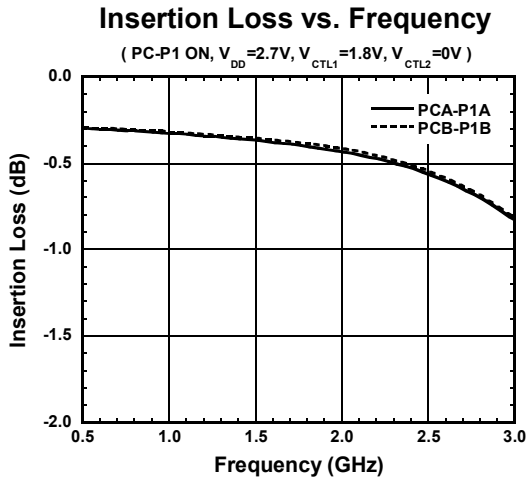
$$B-ISL = \frac{1}{2}(S_{21} - S_{23} - S_{41} + S_{43})$$



■ TERMINAL INFORMATION

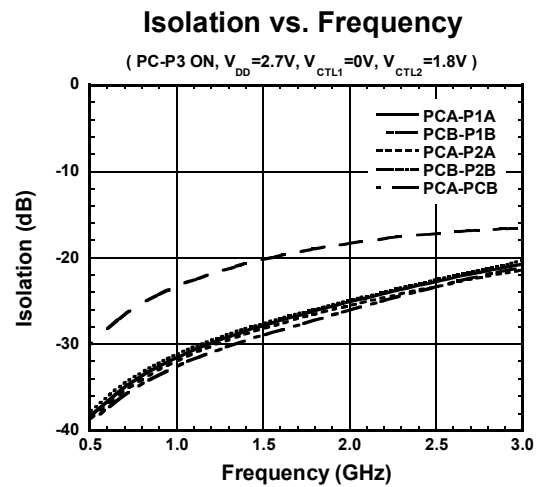
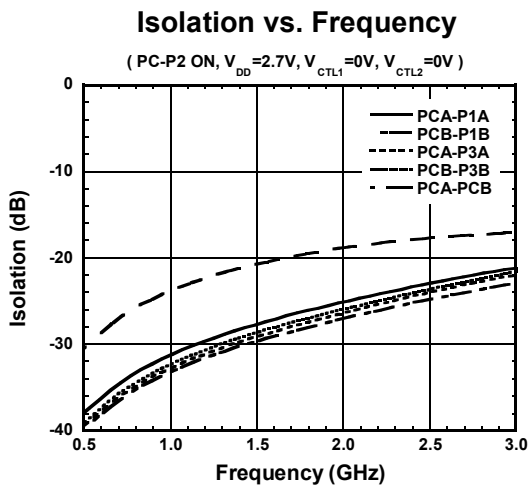
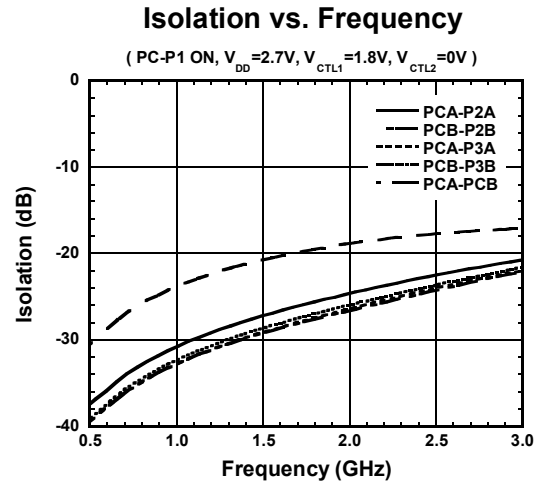
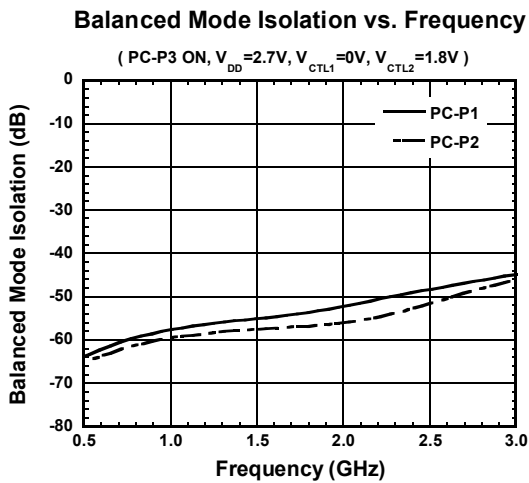
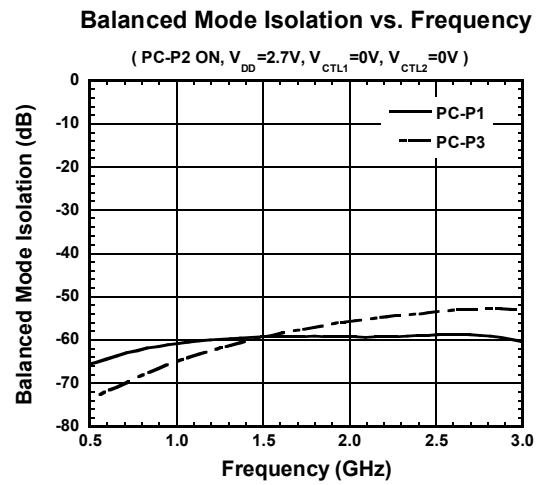
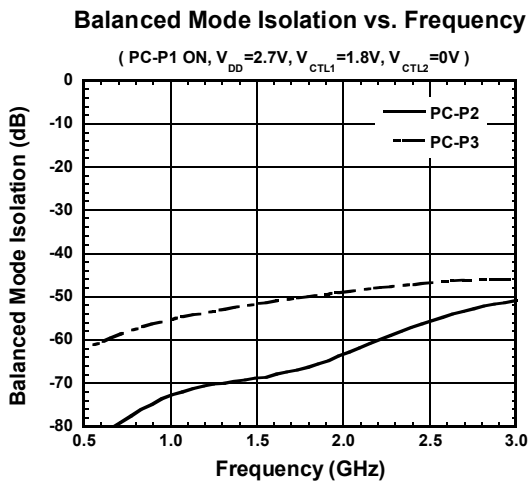
No.	SYMBOL	DESCRIPTION
1, 5, 8 10, 14,	GND	Ground terminal. Connect to the PCB ground plane.
2, 9	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Connect to the PCB ground plane.
3	P2A	The 2nd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P2B port at the same time. An external capacitor is required to block DC voltage.
4	P2B	The 2nd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P2A port at the same time. An external capacitor is required to block DC voltage.
6	P1B	The 1st RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P1A port at the same time. An external capacitor is required to block DC voltage.
7	P1A	The 1st RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P1B port at the same time. An external capacitor is required to block DC voltage.
11	PCB	Common RF port of the 2nd switch. This port is connected with either of P1B, P2B, and P3B port. An external capacitor is required to block DC voltage.
12	PCA	Common RF port of the 1st switch. This port is connected with either of P1A, P2A, and P3A port. An external capacitor is required to block DC voltage.
13	VDD	Positive voltage supply terminal. The positive voltage (+1.5~+4.5V) should be supplied. Please connect a bypass capacitor with GND terminal for best RF performance.
15	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35V~4.5V) or Low-Level (0~+0.45V).
16	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35V~4.5V) or Low-Level (0~+0.45V).
17	P3B	The 3rd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P3A port at the same time. An external capacitor is required to block DC voltage.
18	P3A	The 3rd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P3B port at the same time. An external capacitor is required to block DC voltage.

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

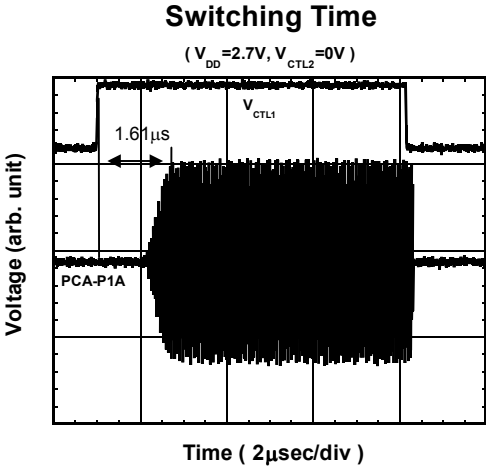
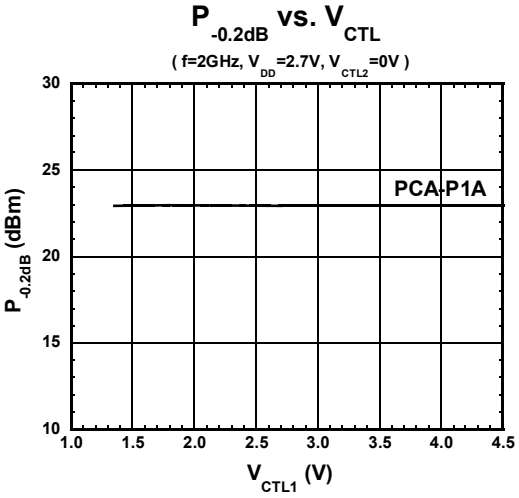
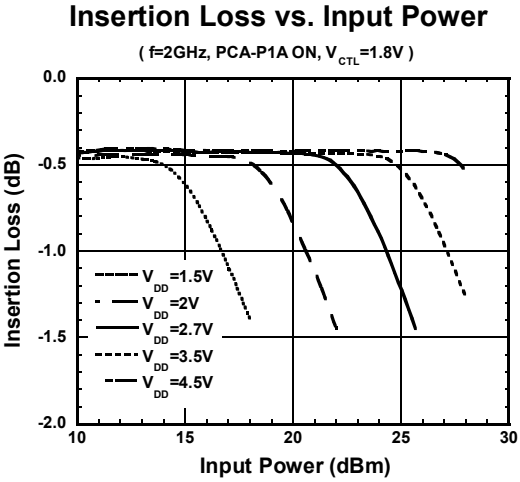
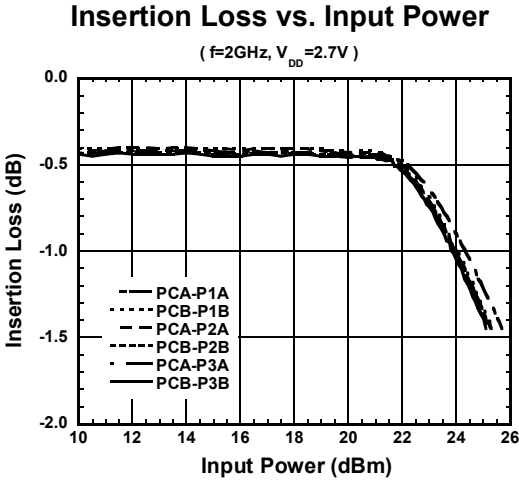


NJG1683ME7

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

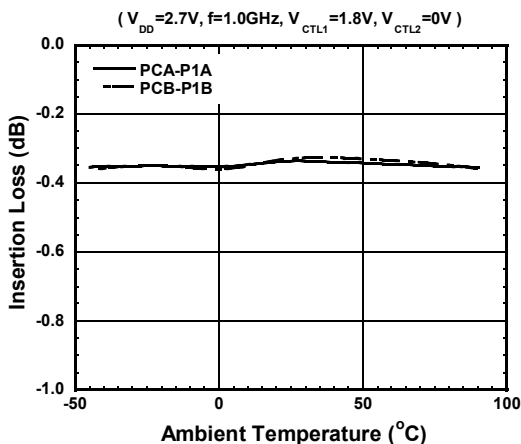


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

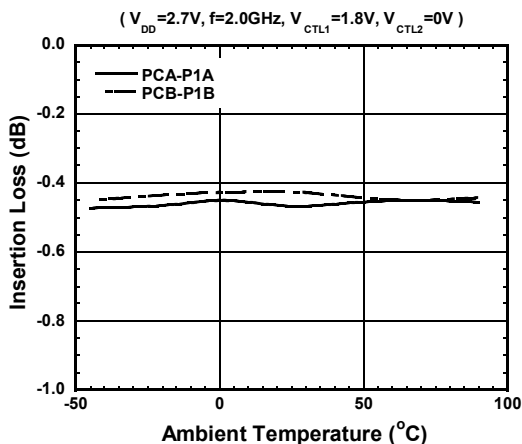


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

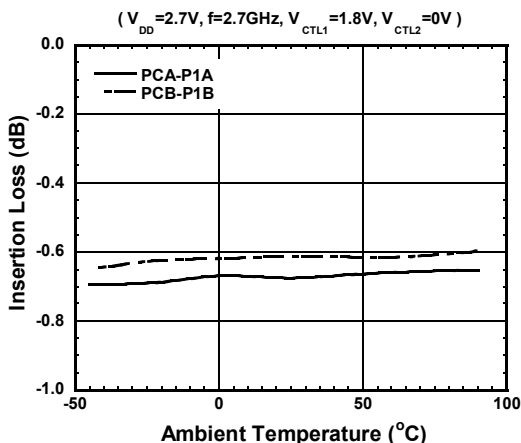
Insertion Loss vs. Ambient Temperature



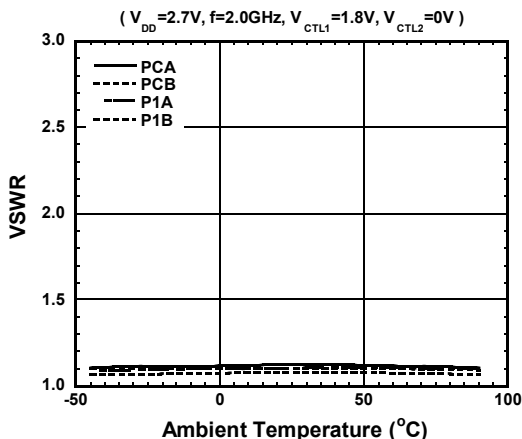
Insertion Loss vs. Ambient Temperature



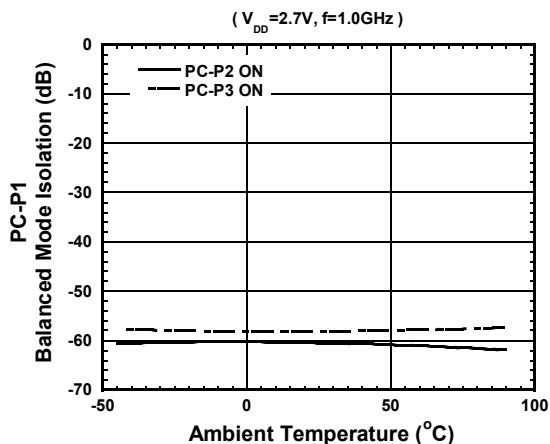
Insertion Loss vs. Ambient Temperature



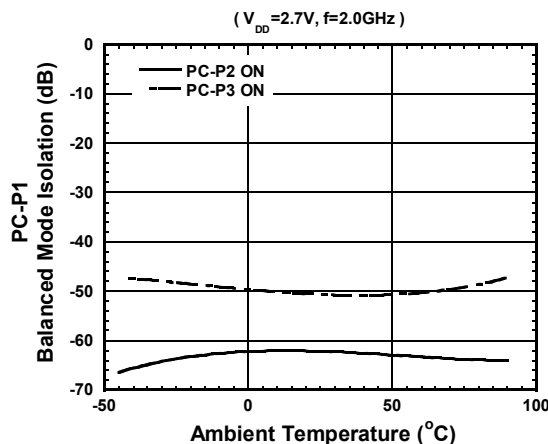
VSWR vs. Ambient Temperature



Balanced Mode Isolation vs. Ambient Temperature

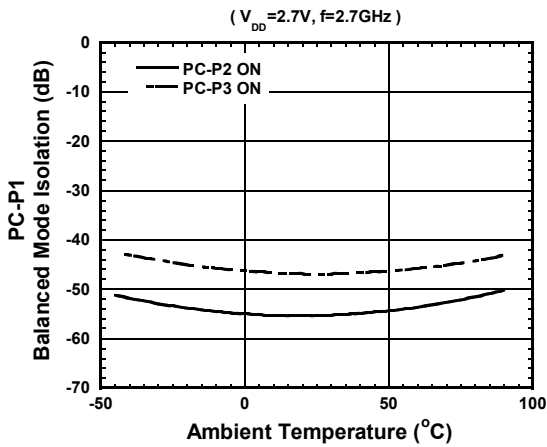


Balanced Mode Isolation vs. Ambient Temperature

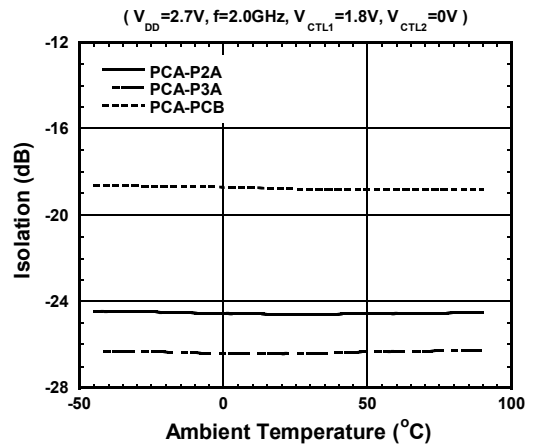


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

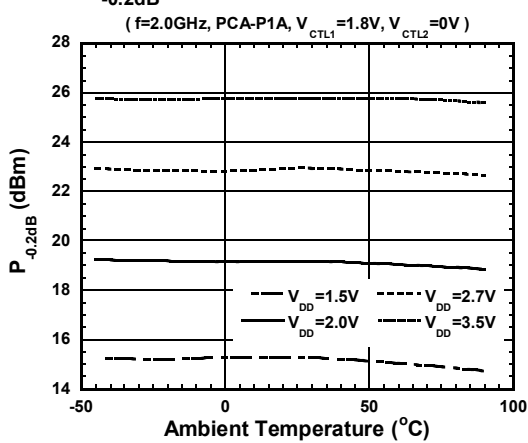
Balanced Mode Isolation vs. Ambient Temperature



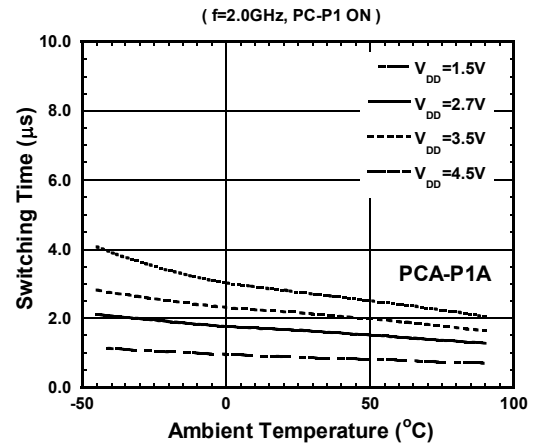
Isolation vs. Ambient Temperature



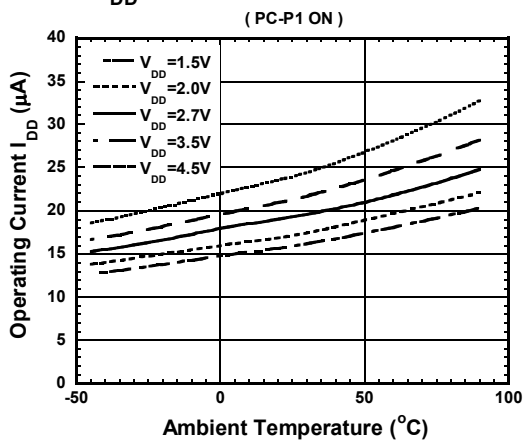
$P_{-0.2dB}$ vs. Ambient Temperature



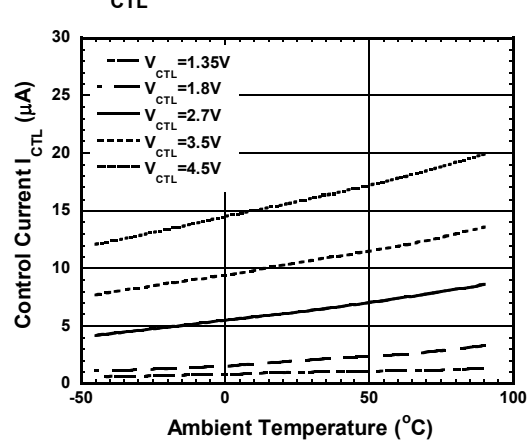
Switching Time vs. Ambient Temperature



I_{DD} vs. Ambient Temperature



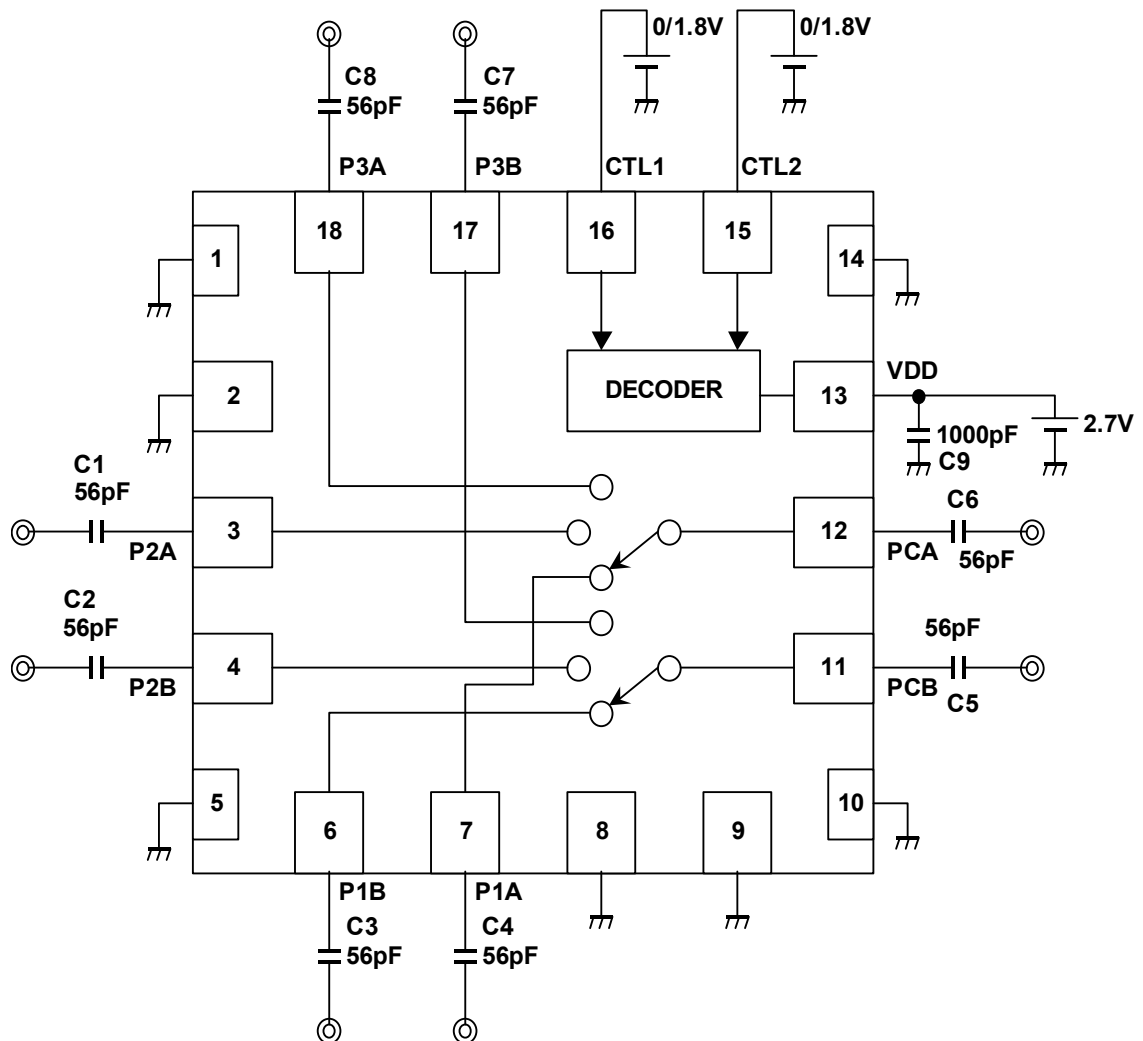
I_{CTL} vs. Ambient Temperature



NJG1683ME7

APPLICATION CIRCUIT

(TOP VIEW)

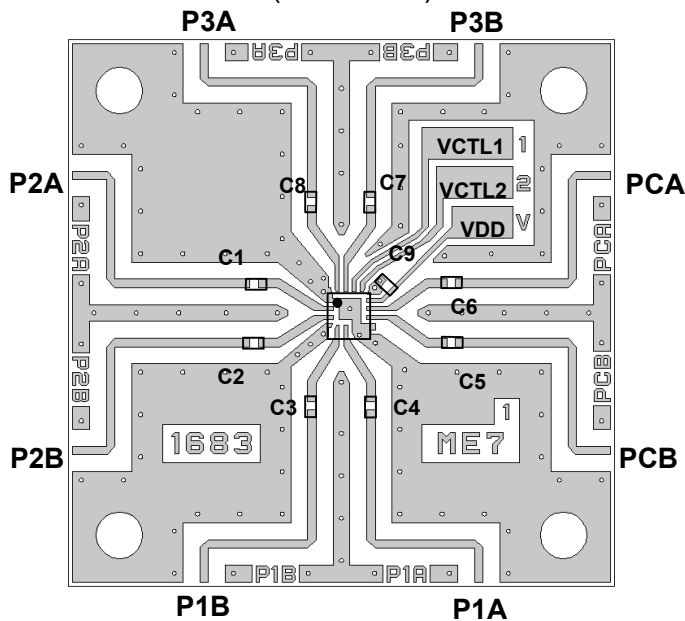


PARTS LIST

PART ID	Value	Notes
C1~C8	56pF	MURATA (GRM15)
C9	1000pF	

TEST PCB LAYOUT

(TOP VIEW)

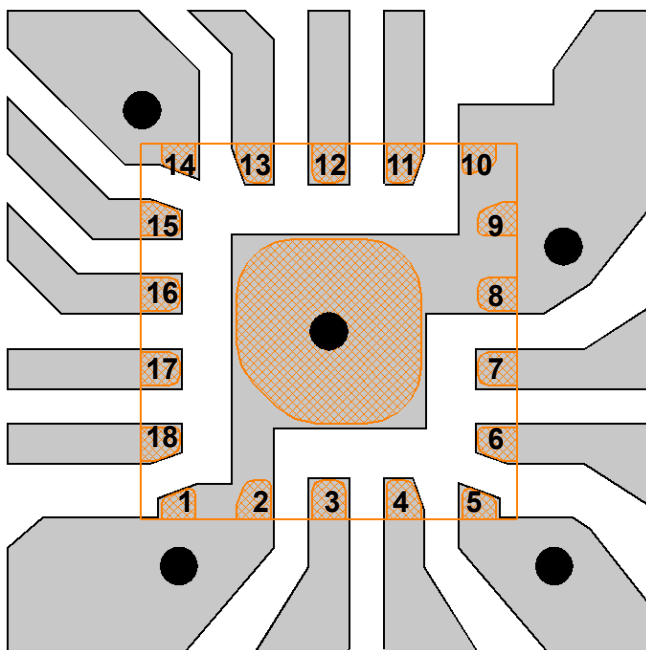


PCB: FR-4, t=0.2mm
 Capacitor Size: 1005
 Strip Line Width: 0.4mm
 PCB Size: 26 x 26mm

Losses of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
1.0	0.33
2.0	0.57
2.7	0.71

<PCB LAYOUT GUIDELINE>



PCB Pattern
 Through-hole (radius: 0.10mm)
 Pin

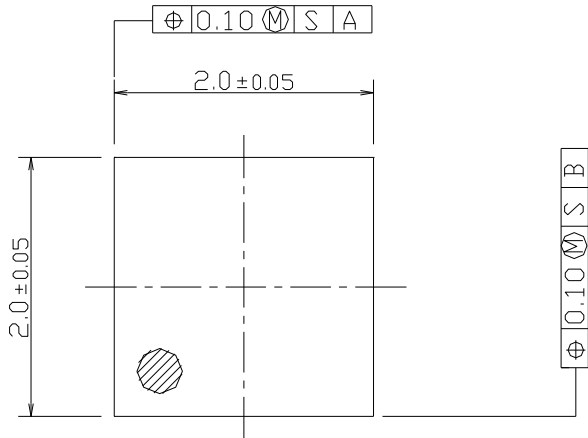
Note2:

The ground plane and the through-holes under Tab, as shown in the picture, are not necessities. There is no problem in deleting them in the practical PCB design, though in such case beware that the GND terminals (pin 1, 2, 8, 9 and 10 as for this particular design shown in the picture) still need through-holes being located in their vicinities.

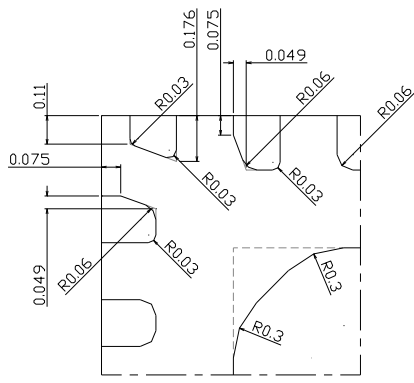
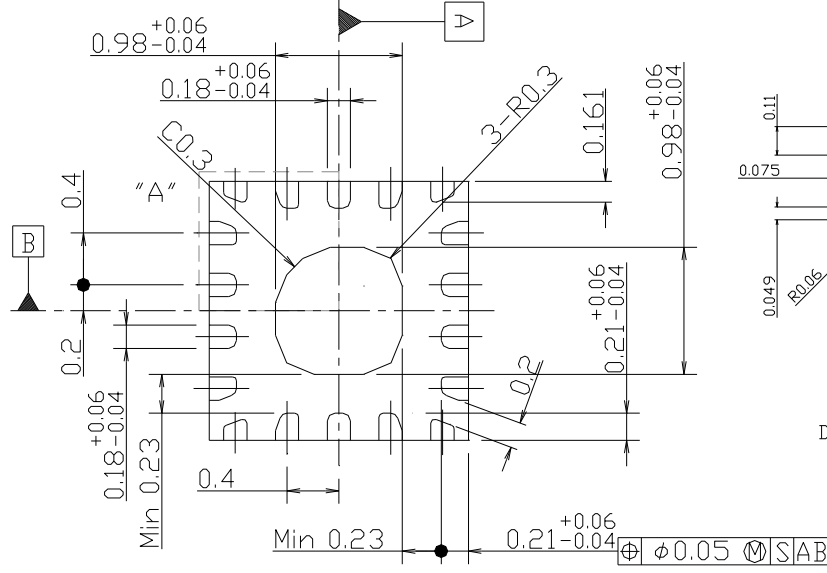
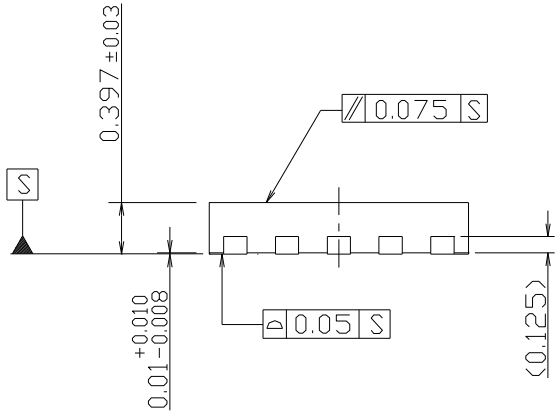
PRECAUTIONS

- [1] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1~C8).
 (However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, e.g. the RF signals are fed by SAW filters that block DC current by nature, etc.)
- [2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor (C9) close to VDD terminal.
- [3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

PACKAGE OUTLINE (EQFN18-E7)



Terminal Treat : SnBi
 Board : Copper
 Molding Material : Epoxy resin
 Weight : 5.0mg
 Unit : mm



Details of "A" part (x2)

Cautions on using this product
 This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]
 The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.