

NJG1139UA2

■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\ \text{ohm}$

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Drain voltage	V_{DD}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{IN}	$V_{DD}=1.8\text{V}$	+15	dBm
Power dissipation	P_D	4-layer FR4 PCB with through-hole (101.5x114.5mm), $T_j=150^{\circ}\text{C}$	590	mW
Operating temperature	T_{opr}		-40~+95	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

General conditions: $V_{DD}=1.8\text{V}$, $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\ \text{ohm}$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		1.7	1.8	3.6	V
Control voltage (High)	$V_{CTL(H)}$		1.5	1.8	3.6	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.4	V
Operating current1	I_{DD1}	RF OFF, $V_{CTL}=1.8\text{V}$	-	3.5	5.0	mA
Operating current2	I_{DD2}	RF OFF, $V_{CTL}=0\text{V}$	-	11	25	μA
Control current	I_{CTL}	RF OFF, $V_{CTL}=1.8\text{V}$	-	6	10	μA

■ ELECTRICAL CHARACTERISTICS2 (High Gain mode)

General conditions: $V_{DD}=1.8V$, $V_{CTL}=1.8V$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\text{ ohm}$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	f_{RF}		470	620	770	MHz
Small signal gain1	Gain1		11.0	14.0	17.0	dB
Noise figure	NF	Exclude PCB & connector losses*1	-	1.2	1.7	dB
Input power at 1dB gain compression point1	$P_{-1dB(IN)1}$		-18.0	-12.0	-	dBm
Input 3rd order intercept point1	IIP3_1	$f1=f_{RF}$, $f2=f_{RF}+100kHz$, $P_{IN}=-25dBm$	-8.0	-4.0	-	dBm
RF IN VSWR1	VSWRi1		-	1.5	4.9	-
RF OUT VSWR1	VSWRo1		-	1.5	3.0	-

■ ELECTRICAL CHARACTERISTICS3 (Low Gain mode)

General conditions: $V_{DD}=1.8V$, $V_{CTL}=0V$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\text{ ohm}$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	f_{RF}		470	620	770	MHz
Small signal gain2	Gain2	Exclude PCB & connector losses*2	-2.5	-2.0	-	dB
Input power at 1dB gain compression point2	$P_{-1dB(IN)2}$		+5.0	+15.0	-	dBm
Input 3rd order intercept point2	IIP3_2	$f1=f_{RF}$, $f2=f_{RF}+100kHz$, $P_{IN}=-8dBm$	+15.0	+30.0	-	dBm
RF IN VSWR2	VSWRi2		-	1.5	2.5	-
RF OUT VSWR2	VSWRo2		-	1.5	2.5	-

*1 Input PCB and connector losses: 0.033dB(at 470MHz), 0.047dB(at 770MHz)

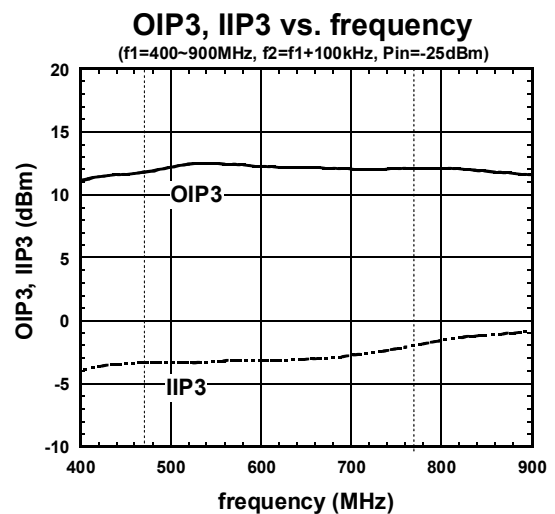
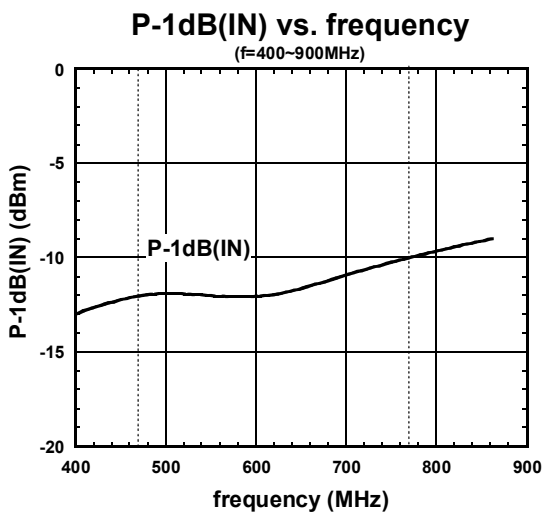
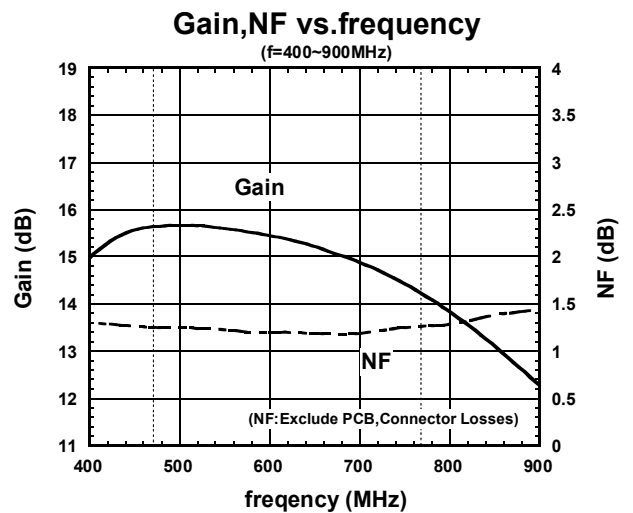
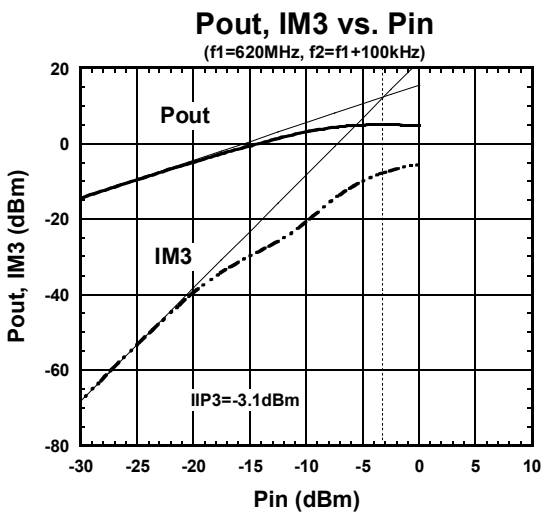
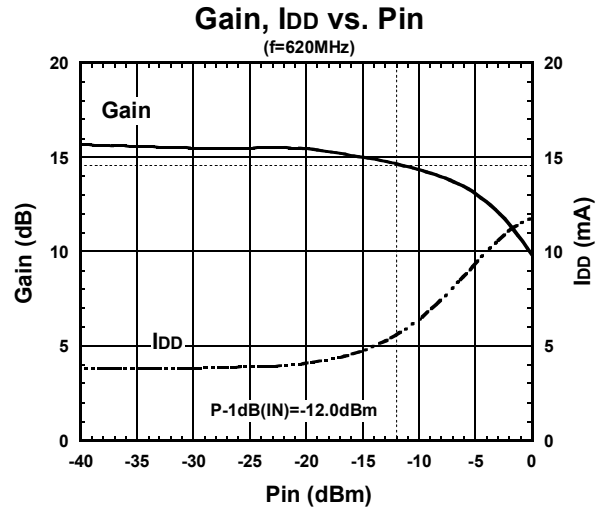
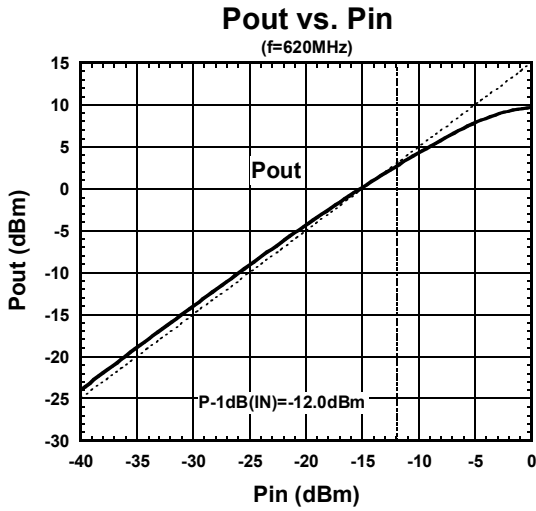
*2 Input & output PCB and connector losses: 0.057dB(at 470MHz), 0.085dB(at 770MHz)

■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. These terminals should be connected to the ground plane as close as possible for excellent RF performance.
2	VDD	This terminal is a power supply terminal of LNA and the logic circuit. Inductor L2 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA.
3	RFOUT	RF input terminal. Since this IC is integrated an input DC blocking capacitor.
4	VCTL	Control voltage supply terminal.
5	GND	Ground terminal. These terminals should be connected to the ground plane as close as possible for excellent RF performance.
6	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. Since this IC is integrated an input DC blocking capacitor.

■ ELECTRICAL CHARACTERISTICS (High Gain mode)

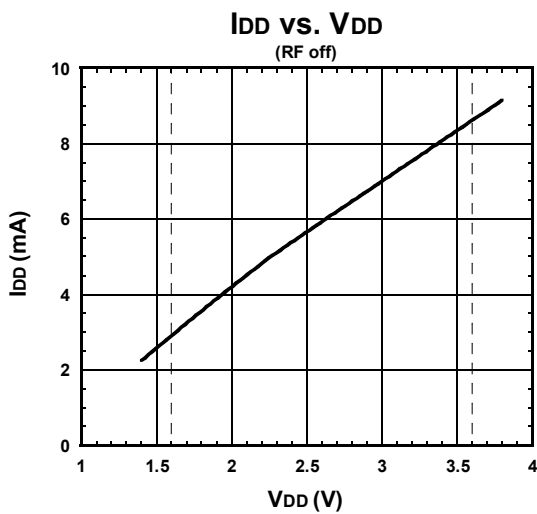
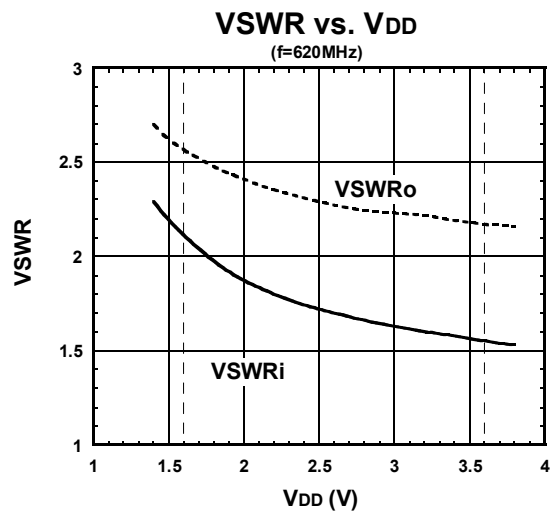
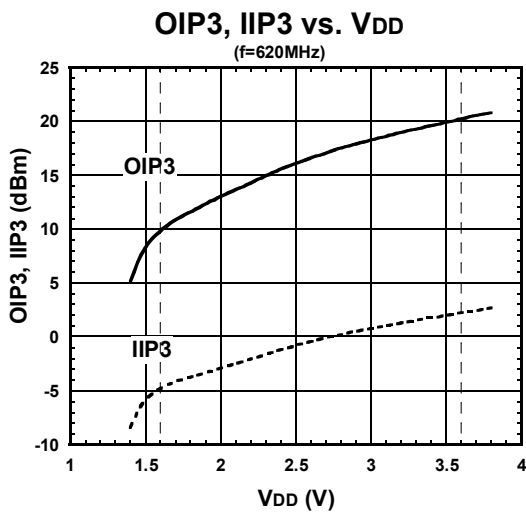
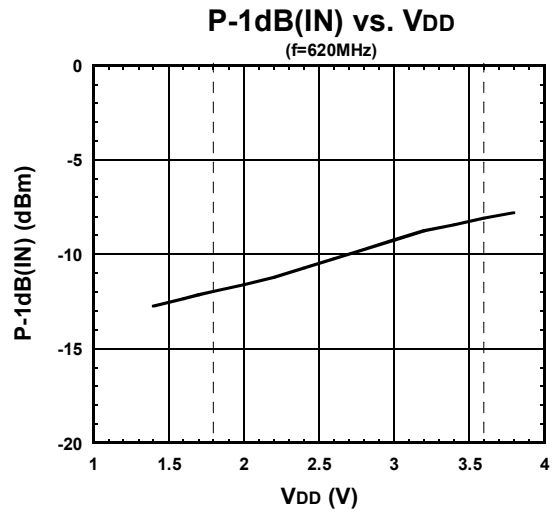
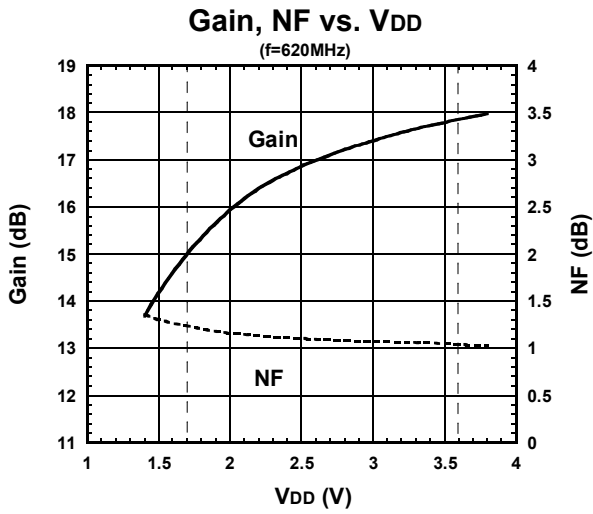
Conditions: $T_a=+25^\circ\text{C}$, $V_{DD}=1.8\text{V}$, $V_{CTL}=1.8\text{V}$, $Z_S=Z_I=50\text{ ohm}$, with application circuit



NJG1139UA2

■ ELECTRICAL CHARACTERISTICS (High Gain mode)

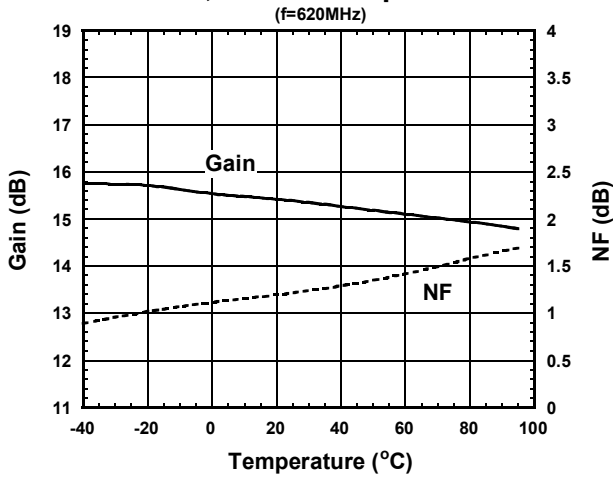
Conditions: $T_a = +25^\circ\text{C}$, $V_{CTL} = 1.8\text{V}$, $Z_s = Z_L = 50\ \Omega$, with application circuit



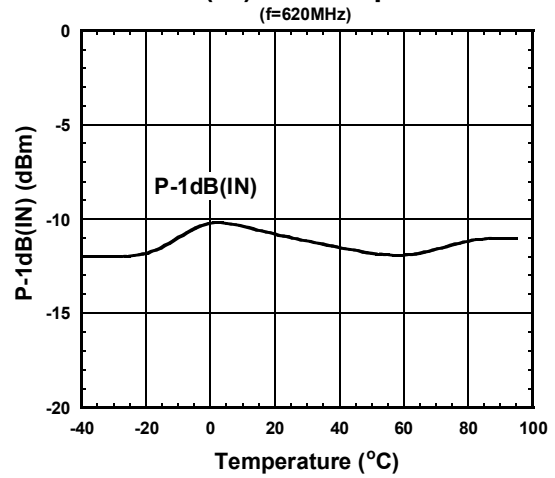
■ ELECTRICAL CHARACTERISTICS (High Gain mode)

Conditions: $V_{DD}=1.8V$, $V_{CTL}=1.8V$, $Z_s=Z_l=50\ \text{ohm}$, with application circuit

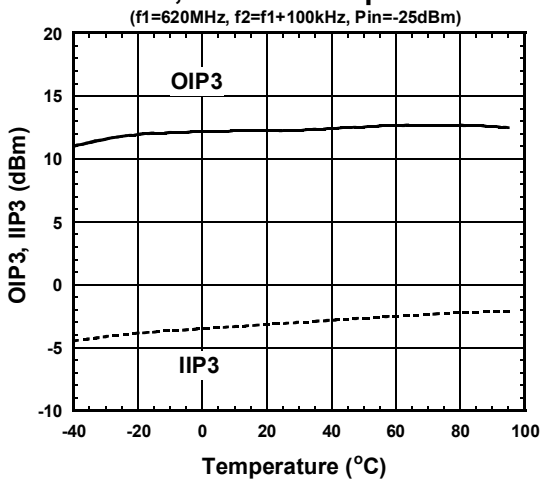
Gain, NF vs. Temperature



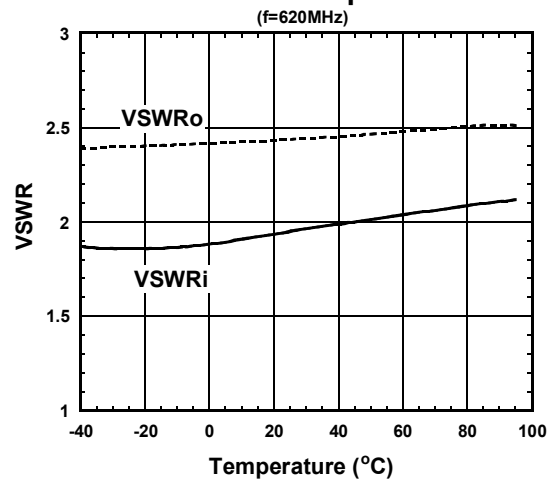
P-1dB(IN) vs. Temperature



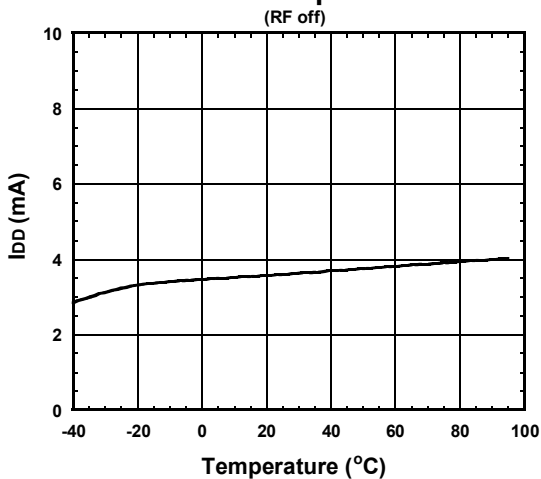
OIP3, IIP3 vs. Temperature



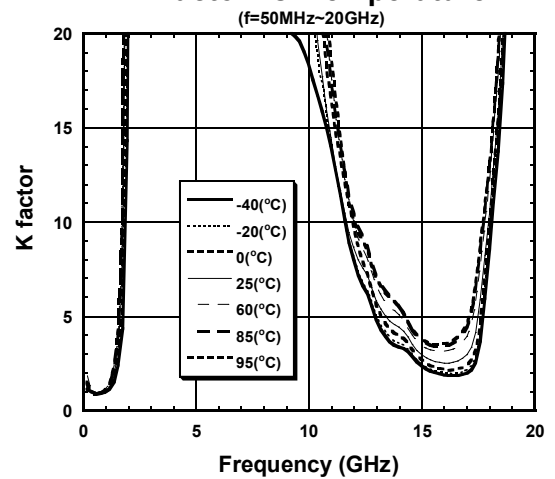
VSWR vs. Temperature



I_{DD} vs. Temperature



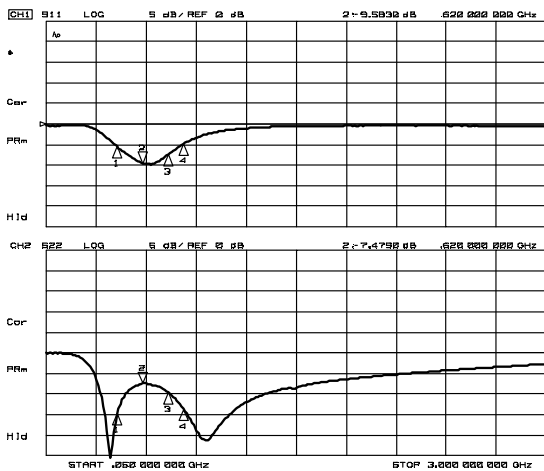
K factor vs. Temperature



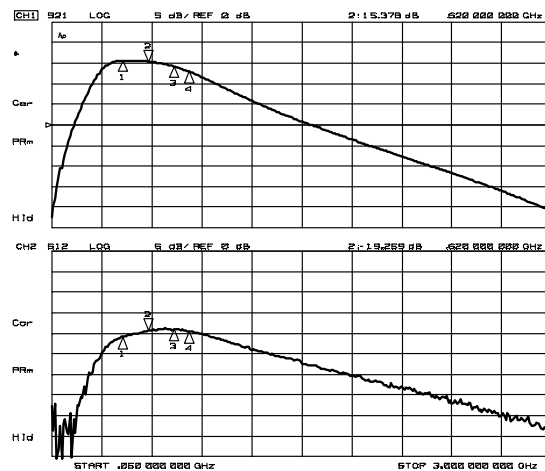
NJG1139UA2

ELECTRICAL CHARACTERISTICS (High Gain mode)

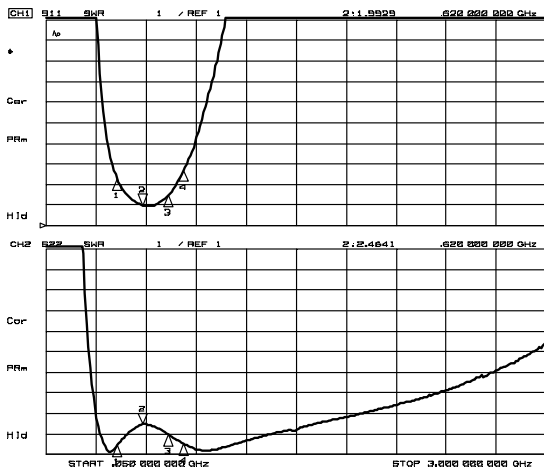
Conditions: $T_a = +25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, $V_{CTL} = 1.8\text{V}$, $Z_S = Z_I = 50\ \Omega$, with application circuit



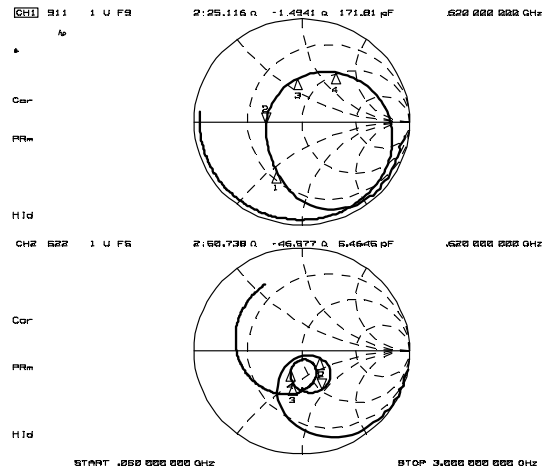
S11, S22



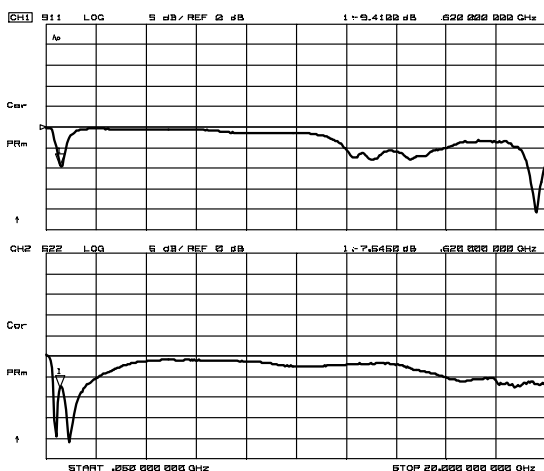
S21, S12



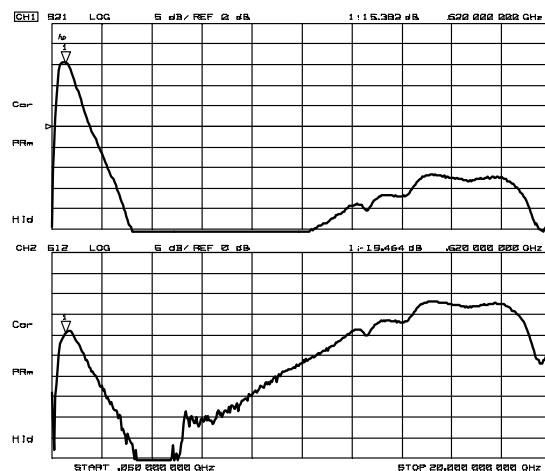
VSWRi, VSWRo



Zin, Zout



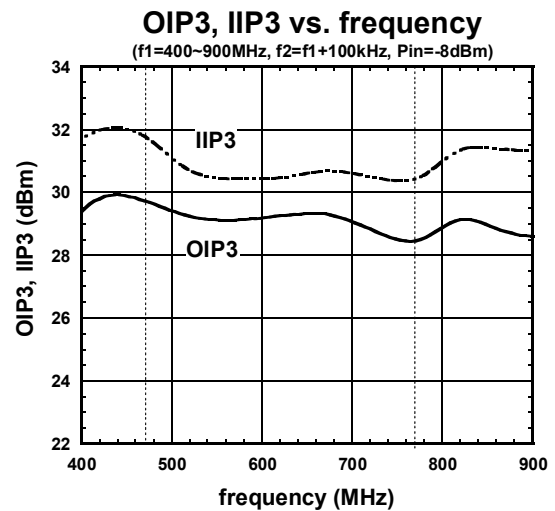
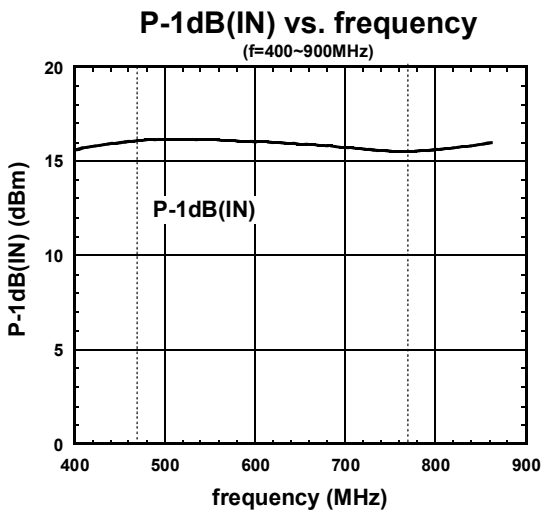
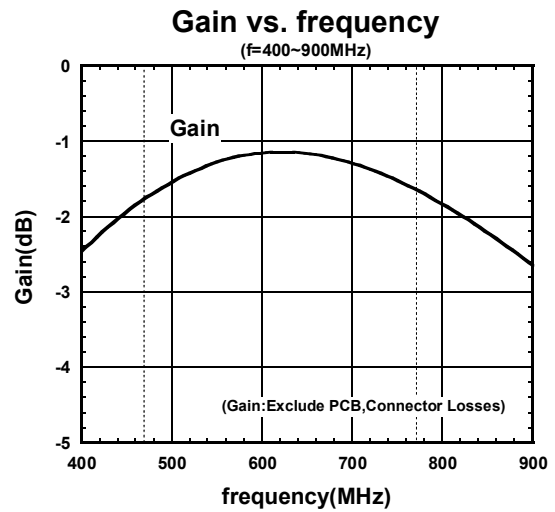
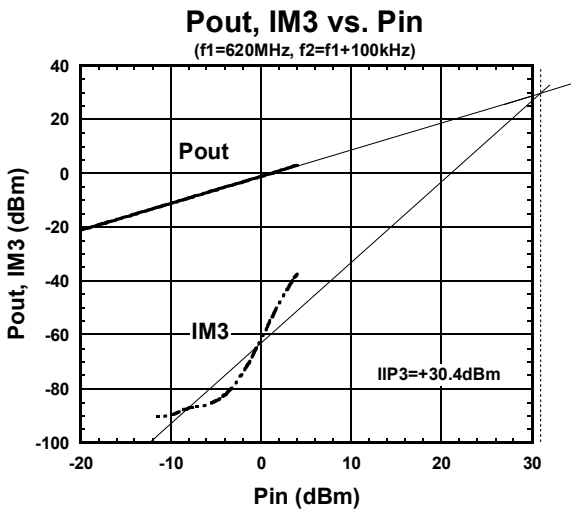
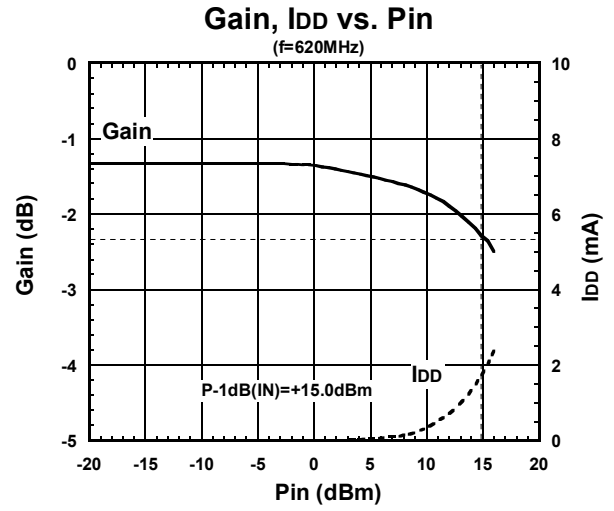
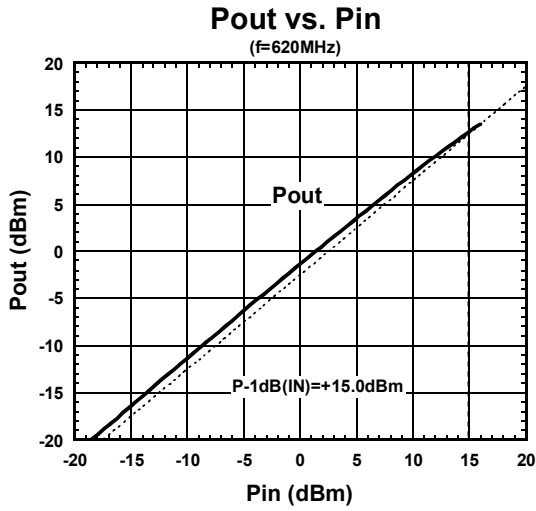
S11, S22 (50MHz~20GHz)



S21, S12 (50MHz~20GHz)

■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

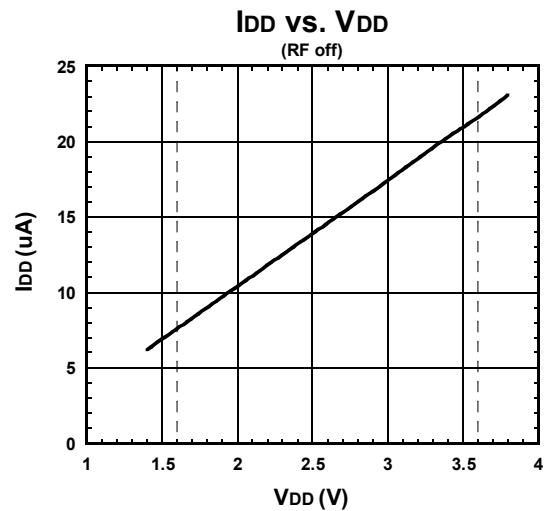
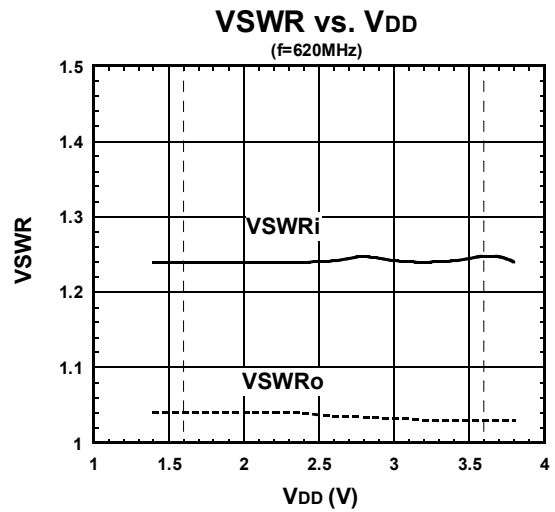
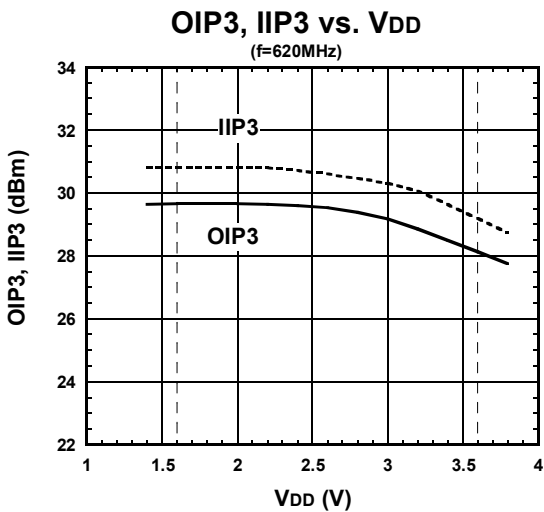
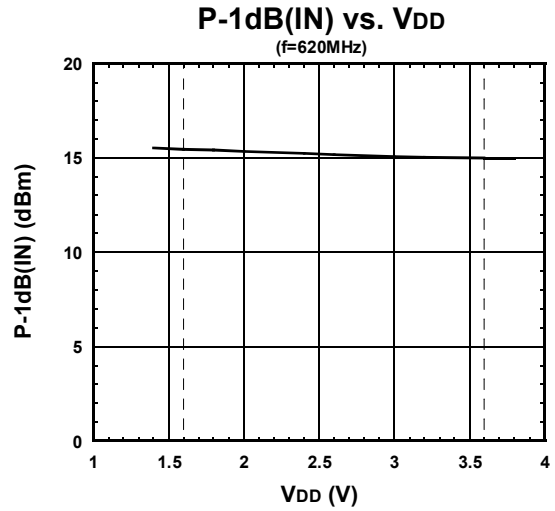
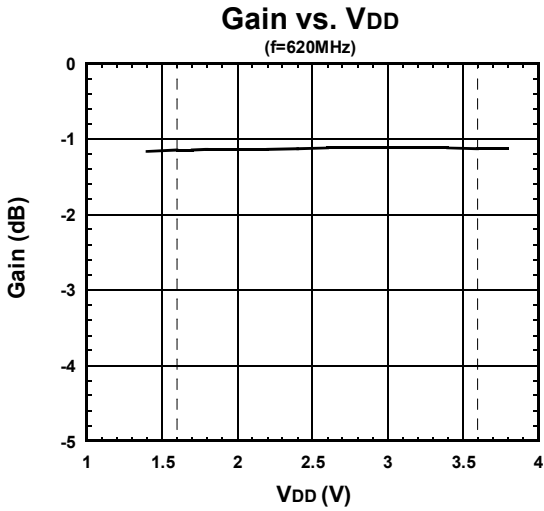
Conditions: $T_a=+25^{\circ}\text{C}$, $V_{DD}=1.8\text{V}$, $V_{CTL}=0\text{V}$, $Z_s=Z_l=50\ \text{ohm}$, with application circuit



NJG1139UA2

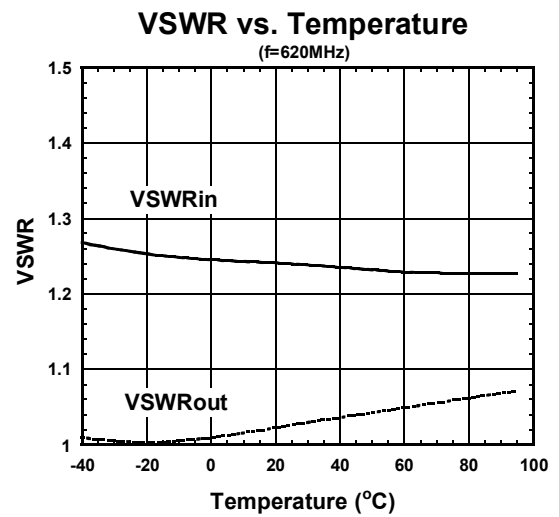
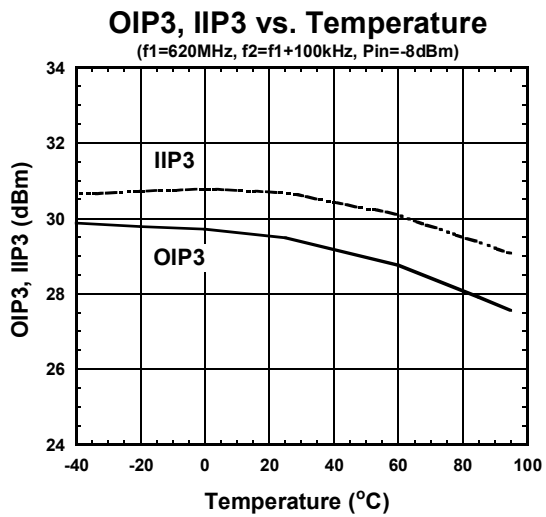
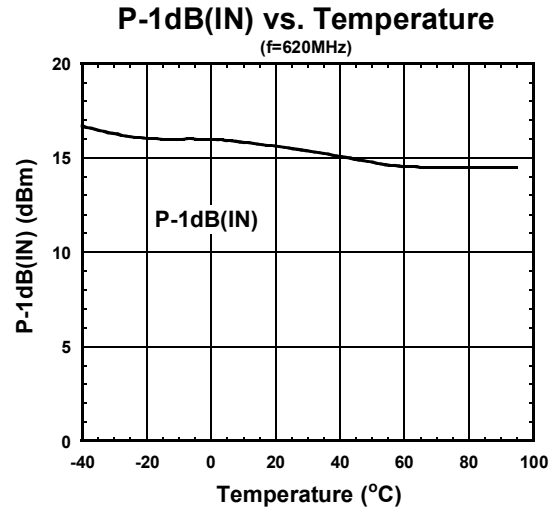
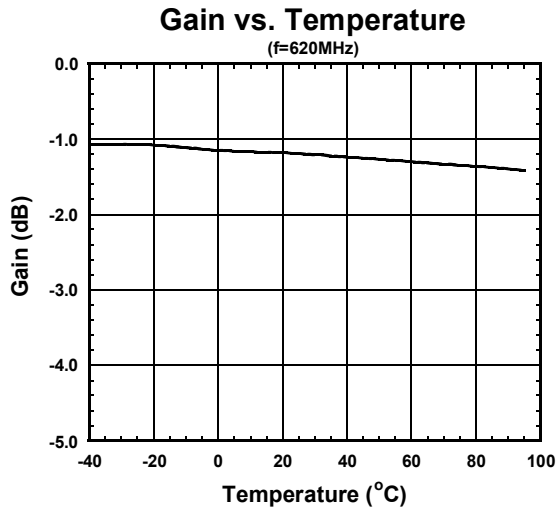
■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

Conditions: $T_a=+25^{\circ}\text{C}$, $V_{\text{CTL}}=0\text{V}$, $Z_s=Z_l=50\ \text{ohm}$, with application circuit



■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

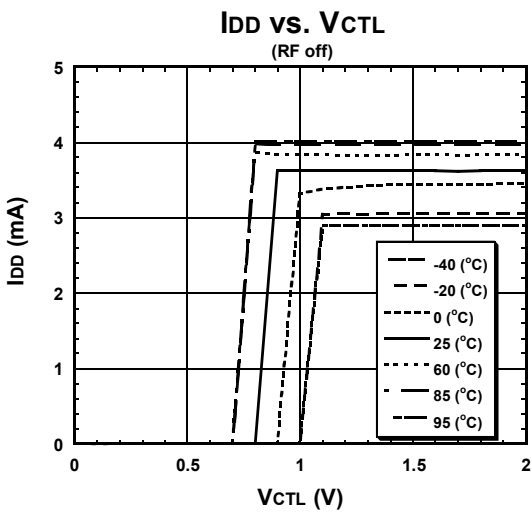
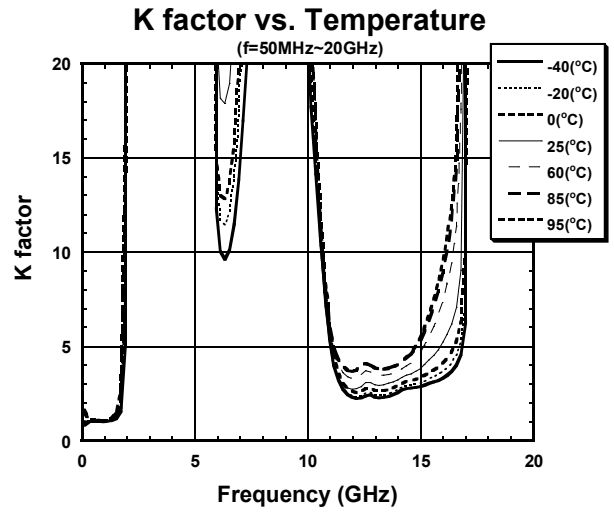
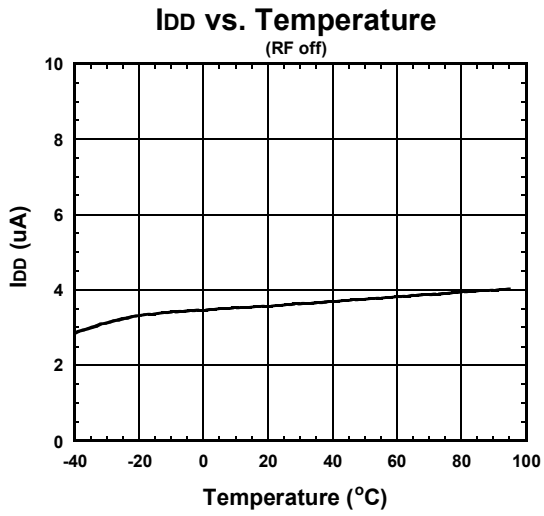
Conditions: $V_{DD}=1.8V$, $V_{CTL}=0V$, $Z_s=Z_l=50\text{ ohm}$, with application circuit



NJG1139UA2

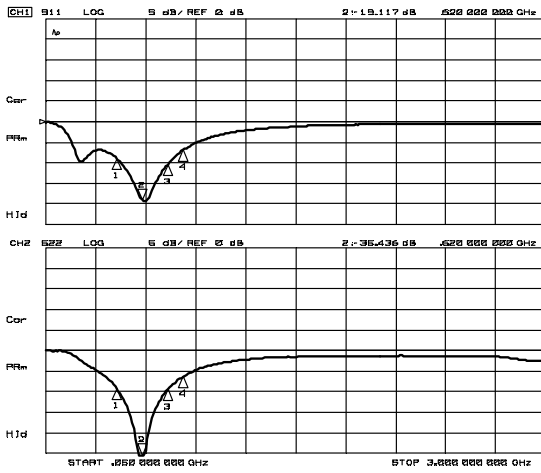
■ ELECTRICAL CHARACTERISTICS (Low Gain mode)

Conditions: $V_{DD}=1.8V$, $V_{CTL}=0V$, $Z_s=Z_l=50\text{ ohm}$, with application circuit

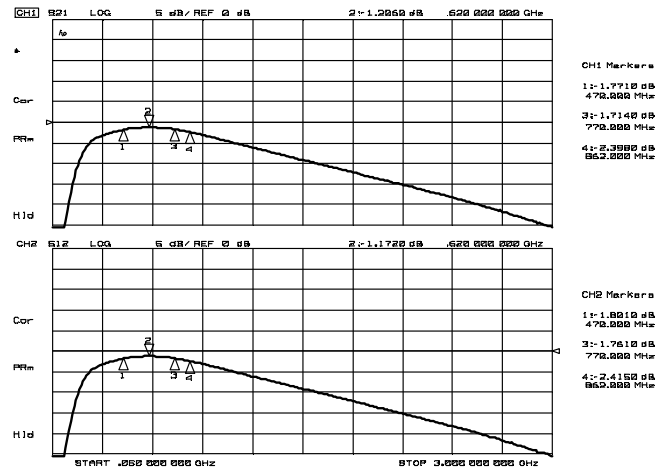


ELECTRICAL CHARACTERISTICS (Low Gain mode)

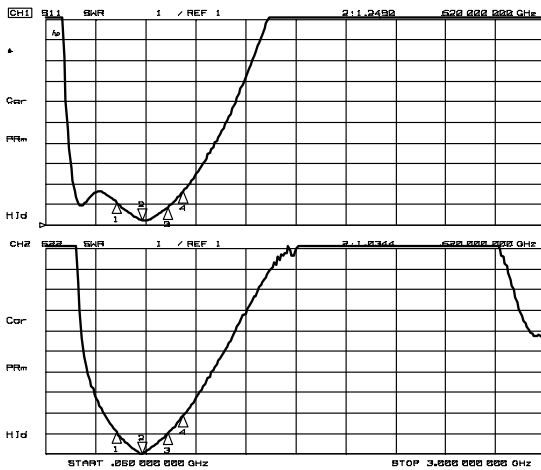
Conditions: $T_a=+25^{\circ}\text{C}$, $V_{DD}=1.8\text{V}$, $V_{CTL}=0\text{V}$, $Z_S=Z_L=50\text{ ohm}$, with application circuit



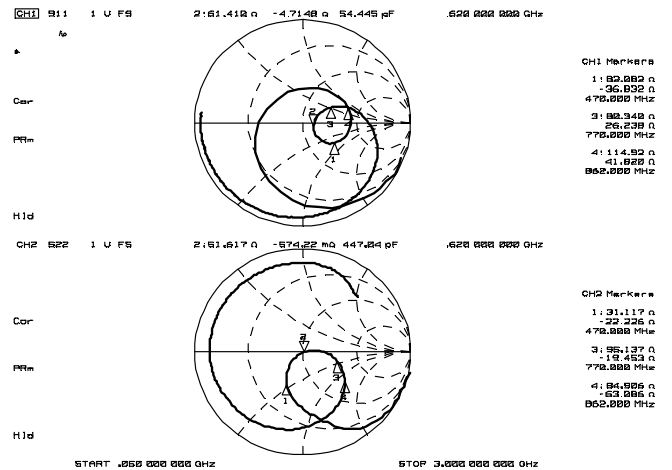
S11, S22



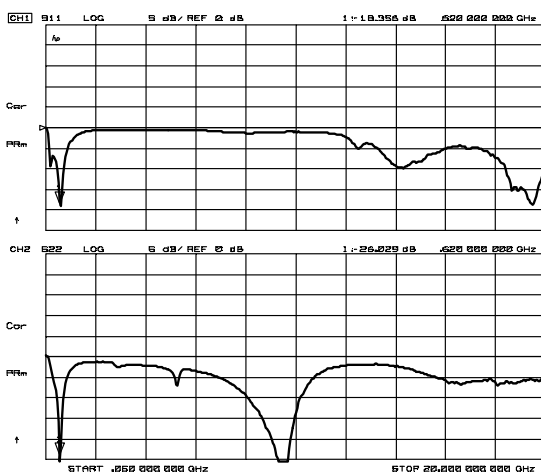
S21, S12



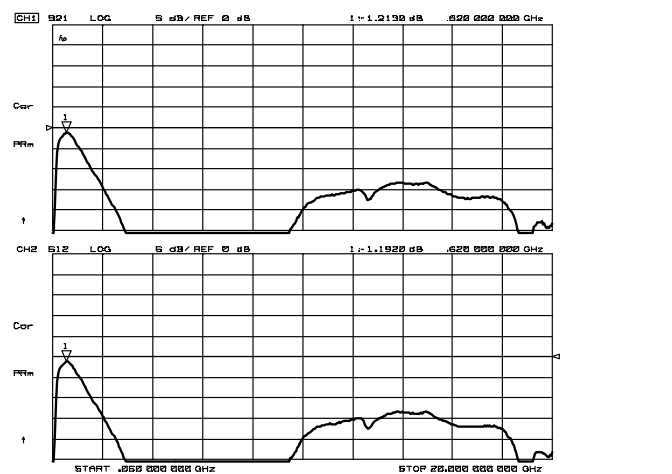
VSWRi, VSWRo



Zin, Zout



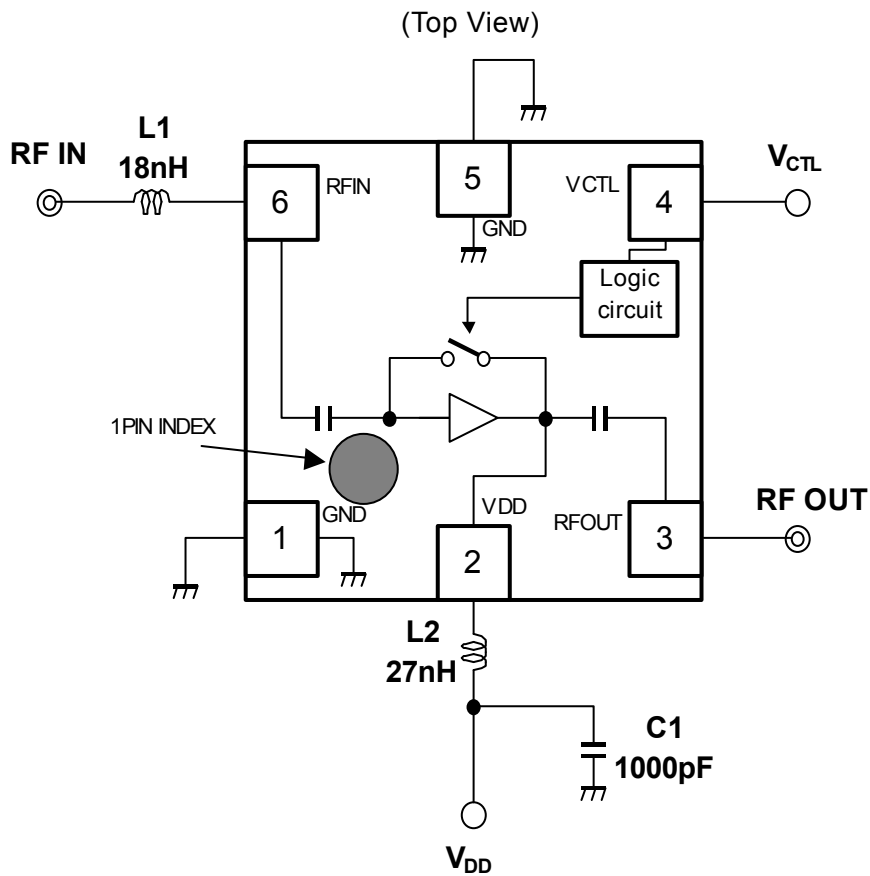
S11, S22 (50MHz~20GHz)



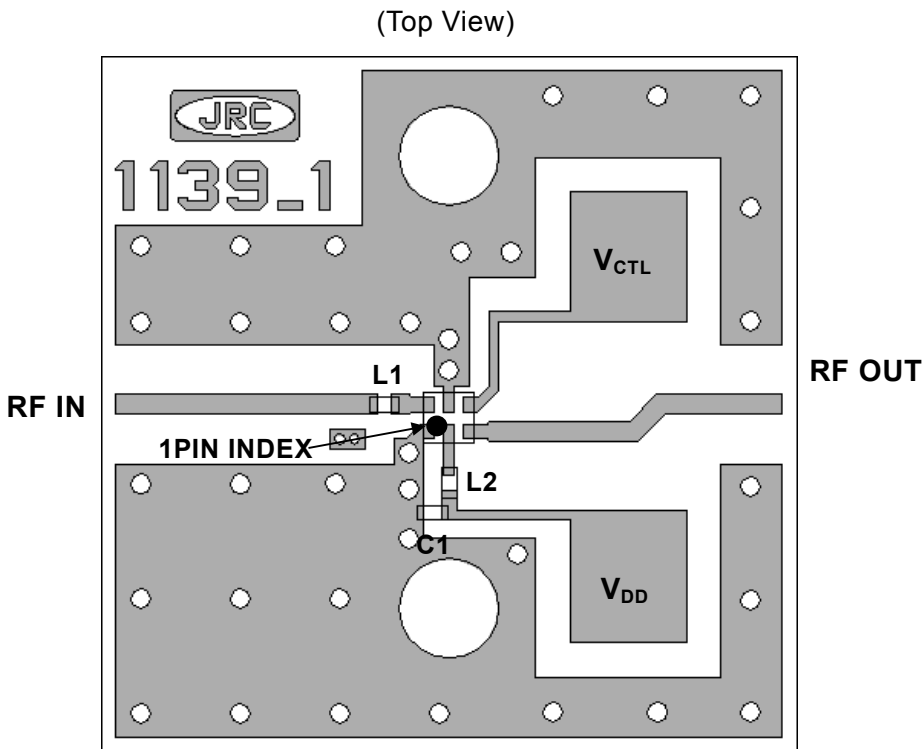
S21, S12 (50MHz~20GHz)

NJG1139UA2

APPLICATION CIRCUIT



TEST PCB LAYOUT



Parts List

Parts ID	Notes
L1, L2	MURATA LQP03T series
C1	MURATA GRM03 series

PCB (FR-4):
 t=0.2mm
 MICROSTRIP LINE WIDTH
 =0.4mm ($Z_0=50 \text{ ohm}$)
 PCB SIZE=14.0mm × 14.0mm

* Please place all external parts around the IC as close as possible.

