Process：SG-6 with HV 20V/30V/36V

0.7um LV CMOS With HV CMOS for Analog IC

■Key Features

LV CMOS for Digital and Analog circuit

- Operating Voltage 5.0V (5.5V Max.)
- Min. Gate Length 0.8um
- Vtp / Vtn [V] 0.65 / 0.65 (Typ.)
- Low Vtp / Vtn [V] 0.50 / 0.50 (Typ.)

Capacitor

- MOS・PIP

Resistor

- Poly ・HR Poly・N-・P-・etc.

Embedded Devices

HV MOS (HV20/ HV30/ HV36)

- Max. Drain Voltage HV20/ HV30/ HV36 20V/ 30V/ 36V
- Max. Gate Voltage same as Drain

Substrate PNP for Voltage reference

- β 8.0
- Vbe 0.65V @ Ic=1uA

Photo Diode

- Peak of Photo Sensitivity λ = 780nm