Single High Side Switch

**GENERAL DESCRIPTION**

The NJW4830 is the single high-side switch that can supply 0.5A. The active clamp circuit, overcurrent and thermal shutdown are built-in with Pch MOS FET. It can be controlled by a logic signal (3V/5V) directly. Therefore, it is suitable for Car accessory, Industrial Equipments and other applications.

**FEATURES**

- Drain-Source Voltage 45V
- Drain Current 0.5A
- Corresponding with Logic Voltage Operation: 3V/5V
- Low On-Resistance 0.35Ω (typ.)
- Low Consumption Current 110µA (typ.)
- Active Clamp Circuit
- Over Current Protection
- Thermal Shutdown
- Package Outline SOT89-5

**PIN CONFIGURATION**

1. IN
2. GND
3. FLT
4. VDD
5. OUT

**BLOCK DIAGRAM**
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>RATINGS</th>
<th>UNIT</th>
<th>REMARK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage</td>
<td>( V_{DS} )</td>
<td>+45 V</td>
<td>V</td>
<td>VDD–OUT Pin</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>( V_{DD} )</td>
<td>+45 V</td>
<td>V</td>
<td>VDD–GND Pin</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>( V_{IN} )</td>
<td>−0.3 to +6 V</td>
<td>V</td>
<td>IN–GND Pin</td>
</tr>
<tr>
<td>FLT Pin Voltage</td>
<td>( V_{FLT} )</td>
<td>−0.3 to +6 V</td>
<td>V</td>
<td>FLT–GND Pin</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>( P_D )</td>
<td>625 (*1) 2,400 (*2) mW</td>
<td>mW</td>
<td>–</td>
</tr>
<tr>
<td>Active Clamp Tolerance</td>
<td>( E_{AS} )</td>
<td>10 mJ</td>
<td>mJ</td>
<td>–</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>( T_j )</td>
<td>−40 to +150 °C</td>
<td>°C</td>
<td>–</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>( T_{op} )</td>
<td>−40 to +85 °C</td>
<td>°C</td>
<td>–</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>( T_{stg} )</td>
<td>−50 to +150 °C</td>
<td>°C</td>
<td>–</td>
</tr>
</tbody>
</table>

(*1): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: based on EIA/JDEC standard size, 2 Layers, Cu area 100mm²)

(*2): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: based on EIA/JDEC standard, 4 Layers)

(For 4 Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
<th>REMARK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain–Source Voltage</td>
<td>( V_{DS} )</td>
<td>0 V</td>
<td>–</td>
<td>40 V</td>
<td>V</td>
<td>VDD–OUT Pin</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>( V_{DD} )</td>
<td>4.6 V</td>
<td>–</td>
<td>40 V</td>
<td>V</td>
<td>VDD–GND Pin</td>
</tr>
<tr>
<td>Output Current</td>
<td>( I_O )</td>
<td>0 A</td>
<td>–</td>
<td>0.5 A</td>
<td></td>
<td>VDD–OUT Pin</td>
</tr>
<tr>
<td>Input Pin Voltage</td>
<td>( V_{IN} )</td>
<td>0 V</td>
<td>–</td>
<td>5.5 V</td>
<td>V</td>
<td>IN–GND Pin</td>
</tr>
<tr>
<td>FLT Pin Voltage</td>
<td>( V_{FLT} )</td>
<td>0 V</td>
<td>–</td>
<td>5.5 V</td>
<td>V</td>
<td>FLT–GND Pin</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{DS}=13V$, $Ta=25°\text{C}$)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Output Clamp Voltage</td>
<td>$V_{DSS_CL}$</td>
<td>$V_{IN}=0V, I_{D}=1mA, V_{DD}=40V$</td>
<td>$V_{DD}$45</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>High Level Input Voltage</td>
<td>$V_H$</td>
<td>$I_D=10mA$</td>
<td>2.64</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Low Level Input Voltage</td>
<td>$V_L$</td>
<td>$I_D=100\mu A$</td>
<td>–</td>
<td>–</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td>Protection Circuit Function</td>
<td>$V_{IN_opr}$</td>
<td></td>
<td>2.64</td>
<td>–</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>OUT Pin Leak Current at OFF State</td>
<td>$I_{OLEAKOUT}$</td>
<td>$V_{IN}=0V, V_{DD}=40V$</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Quiescent Current 1</td>
<td>$I_{DD1}$</td>
<td>$V_{IN}=0V, V_{DD}=40V$</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Quiescent Current 2</td>
<td>$I_{DD2}$</td>
<td>$V_{IN}=5V$</td>
<td>–</td>
<td>110</td>
<td>150</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Input Current</td>
<td>$I_{IN}$</td>
<td>$V_{IN}=5V$</td>
<td>–</td>
<td>150</td>
<td>190</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>On-state Resistance</td>
<td>$R_{DS_ON}$</td>
<td>$V_{IN}=5V, I_{D}=0.5A$</td>
<td>–</td>
<td>0.35</td>
<td>0.6</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>Over Current Protection 1</td>
<td>$I_{LIMIT1}$</td>
<td>$V_{IN}=5V, V_{DS}=5V$</td>
<td>0.5</td>
<td>0.75</td>
<td>1.2</td>
<td>$A$</td>
</tr>
<tr>
<td>Over Current Protection 2</td>
<td>$I_{LIMIT2}$</td>
<td>$V_{IN}=5V, V_{DD}=V_{DS}=40V$</td>
<td>0.1</td>
<td>0.4</td>
<td>–</td>
<td>$A$</td>
</tr>
<tr>
<td>Turn-on Time</td>
<td>$t_{ON}$</td>
<td>$V_{IN}=0$ to 5V, $I_{D}=0.5A$</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>$\mu s$</td>
</tr>
<tr>
<td>Turn-off Time</td>
<td>$t_{OFF}$</td>
<td>$V_{IN}=5$ to 0V, $I_{D}=0.5A$</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>$\mu s$</td>
</tr>
<tr>
<td>OUT–VDD Voltage Difference</td>
<td>$V_{PDOV}$</td>
<td>$V_{IN}=0V, I_{DRH}=1A$</td>
<td>–</td>
<td>0.85</td>
<td>1.2</td>
<td>$V$</td>
</tr>
<tr>
<td>FLT Pin Low Level</td>
<td>$V_{VFLT}$</td>
<td>$I_{FLT}=500\mu A$</td>
<td>–</td>
<td>0.25</td>
<td>0.5</td>
<td>$V$</td>
</tr>
<tr>
<td>Output Voltage</td>
<td></td>
<td>$V_{FLT}=5.5V$</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>OUTPUT Pin at High Level</td>
<td>$I_{OLEAKFLT}$</td>
<td>$V_{FLT}=5.5V$</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>FLT Delay Time</td>
<td>$t_{DFLT}$</td>
<td>$V_{IN}=0$ to 5V, $V_{DS}=22V$</td>
<td>–</td>
<td>5</td>
<td>–</td>
<td>$ms$</td>
</tr>
</tbody>
</table>

### TRUTH TABLE

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Operating Condition</th>
<th>FLT Pin</th>
<th>Output Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Normal</td>
<td>H</td>
<td>OFF</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>ON</td>
</tr>
<tr>
<td>L</td>
<td>Over Current $I_{LIMIT1}$</td>
<td>H</td>
<td>OFF</td>
</tr>
<tr>
<td>L</td>
<td>Over Current $I_{LIMIT2}$</td>
<td>L</td>
<td>$I_{LIMIT1}$</td>
</tr>
<tr>
<td>L</td>
<td>$T_j&gt;150°\text{C}$</td>
<td>H</td>
<td>OFF</td>
</tr>
<tr>
<td>H</td>
<td></td>
<td>H</td>
<td>OFF</td>
</tr>
</tbody>
</table>
TIMING CHART
ON, OFF Switching Time (VIN=0 to 5V, VDD=13V, Io=0.5A)

 FLT Delay Time (VIN=0 to 5V, VDD=VDS=22V)

FLT Delay Time Measurement Circuit
Input signal

Over Current Protection

Thermal Protection

Output voltage

Output current

Fault signal

ILIMIT1

VDD

V_{DSS,CL}

Inductive load

Normal

Current limit1

Current limit2

Thermal shutdown

Active clamp

0A

High

Low

OFF

ON

0V

IL_{\text{LIM1}}

I_{\text{LIM2}}

I_{\text{DFL}}
OVER CURRENT PROTECTION CHARACTERISTIC

```
I_D [A]

I_LIMIT1

I_LIMIT2

VDS [V]

FLT Terminal L H
```

TYPICAL APPLICATION

```
Logic Voltage ex. 5V, 3V

Micro Controller

NJW4830

VDD

IN OUT

FAULT

FLT GND

R_L

New Japan Radio Co., Ltd.

Ver.2014-01-08
```
CHARACTERISTICS

Drain-Source Clamp Voltage vs. Ambient Temperature

Quiescent Current2 vs. Ambient Temperature

Input Current vs. Input Voltage

Input Current vs. Ambient Temperature
CHARACTERISTICS

ON-state Resistance vs. Supply Voltage

ON-state Resistance vs. Ambient Temperature

Over Current Protection1 vs. Ambient Temperature

Over Current Limit1 [A]

Over Current Protection2 vs. Ambient Temperature

Over Current Limit2 [A]

Output Current vs. Drain-Source Voltage

Output Current [A]
CHARACTERISTICS

Turn-on Time vs. Ambient Temperature

Turn-off Time vs. Ambient Temperature

FLT Pin Low Level Output Voltage vs. Ambient Temperature

FLT Delay Time vs. Ambient Temperature

TSD Detect / Release Temperature vs. Input Voltage

Detection Temperature

Release Temperature
**Application Tips**

### Technical Information

#### Regarding Active Clamp Capacity of High/Low side Switch Products

- **What is “Active Clamp Capacity”.**
  The IC might suffer to damage by the inductive kickback at the transient time of ON state to OFF state, when an inductive load such as a solenoid or motor is used for the load of the high-side/low-side switch.
  The protection circuit for the inductive kickback is the active clamp circuit. The energy that can be tolerated by the active clamp circuit is called “Active Clamp Capacity (EAS)”.

When using an inductive load to the high-side/low-side switch, you should design so that the $E_{SW}$ does not exceed the active clamp capability.

- **IC operation without an external protection parts (Fig 1)**

![Active Clamp Waveform](image)

**Fig1. Active Clamp Waveform (Left: Low-side Switch / Light High-side Switch)**

At when the $V_N$ turns off, the drain-source voltage ($V_{DS}$) increases rapidly by the behavior of the inductive load that is keeping current flowing. However, it will be clamped at $V_{DSS_{CL}}$ by the active clamp circuit. At the same time, the drain current is flowed by adjusting the gate voltage of the output transistor, and the energy is dissipated at the output transistor.

The energy: $E_{SW}$ is shown by the following formula.

$$E_{SW} = \int_0^t V_{DS}(t) \cdot I_D(t) dt = \frac{1}{2} \cdot LI_{AP}^2 \cdot \frac{V_{DSS_{CL}}}{V_{DSS_{CL}} - V_{DD}}$$

The $E_{SW}$ is consumed inside IC as heat energy. However, the thermal shutdown does not work when the $V_N$ is 0V. Therefore in worst case the IC might break down. When using the active clamp, you should design $E_{SW}$ does not exceed the $E_{AS}$. 
• Application Hint

The simplest protection example is to add an external flywheel diode at the load to protect IC from an inductive kickback. (Fig.2)

![Diagrams showing application circuit of inductance load driving (Left: Low-side Switch / Light High-side Switch)](image)

Fig 2. Application Circuit of Inductance Load Driving (Left: Low-side Switch / Light High-side Switch)