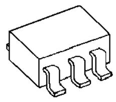
Single Low Side Switch

■ GENERAL DESCRIPTION

The NJW4820 is the single low-side switch that can supply 0.5A. The active clamp, overcurrent and thermal shutdown are built in with Nch MOS FET.

It can be controlled by a logic signal (3V/5V) directly. Therefore, it is suitable for a various power drive application of the motor, the solenoid and the lamp etc.

■ PACKAGE OUTLINE

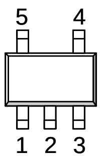


NJW4820F

■ FEATURES

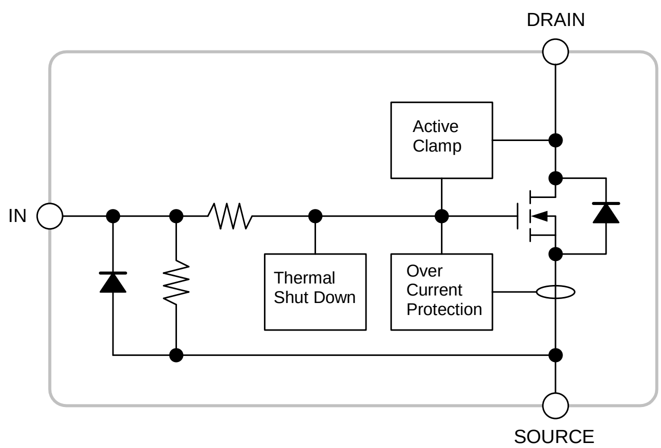
- Drain-Source Voltage 43V
- Drain Current 0.5A
- Corresponding with Logic Voltage Operation: 3V/5V
- Low On-Resistance 0.27Ω typ. (V_{IN}=5V)
  0.30Ω typ. (V_{IN}=3.3V)
- Low Consumption Current 80μA typ. (V_{IN}=5V)
  65μA typ. (V_{IN}=3.3V)
- Active Clamp Circuit
- Over Current Protection (Self recovery type current limiting function)
- Thermal Shutdown
- Package Outline SOT23-5

■ PIN CONFIGURATION



1. N.C.
2. SOURCE
3. IN
4. N.C.
5. DRAIN

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYNBOL	RATINGS	UNIT	REMARK
Drain-Source Voltage	V_{DS}	+43	V	DRAIN–SOURCE Pin
Input Voltage	V_{IN}	–0.3 to +6	V	IN–SOURCE Pin
Power Dissipation	P_D	480 (*1) 640 (*2)	mW	–
Active Clamp Tolerance (Single Pulse)	E_{AS}	10	mJ	–
Active Clamp Current	I_{AP}	1	A	–
Junction Temperature	T_j	–40 to +150	°C	–
Operating Temperature	T_{opr}	–40 to +85	°C	–
Storage Temperature	T_{stg}	–50 to +150	°C	–

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm

■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Drain-Source Voltage	V_{DS}	–	–	40	V	DRAIN–SOURCE Pin
Drain Current	I_D	0	–	0.5	A	DRAIN–SOURCE Pin
Input Pin Voltage	V_{IN}	0	–	5.5	V	IN–SOURCE Pin

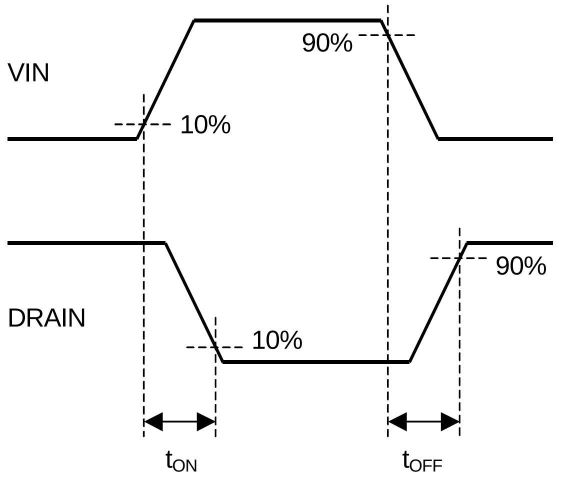
■ ELECTRICAL CHARACTERISTICS

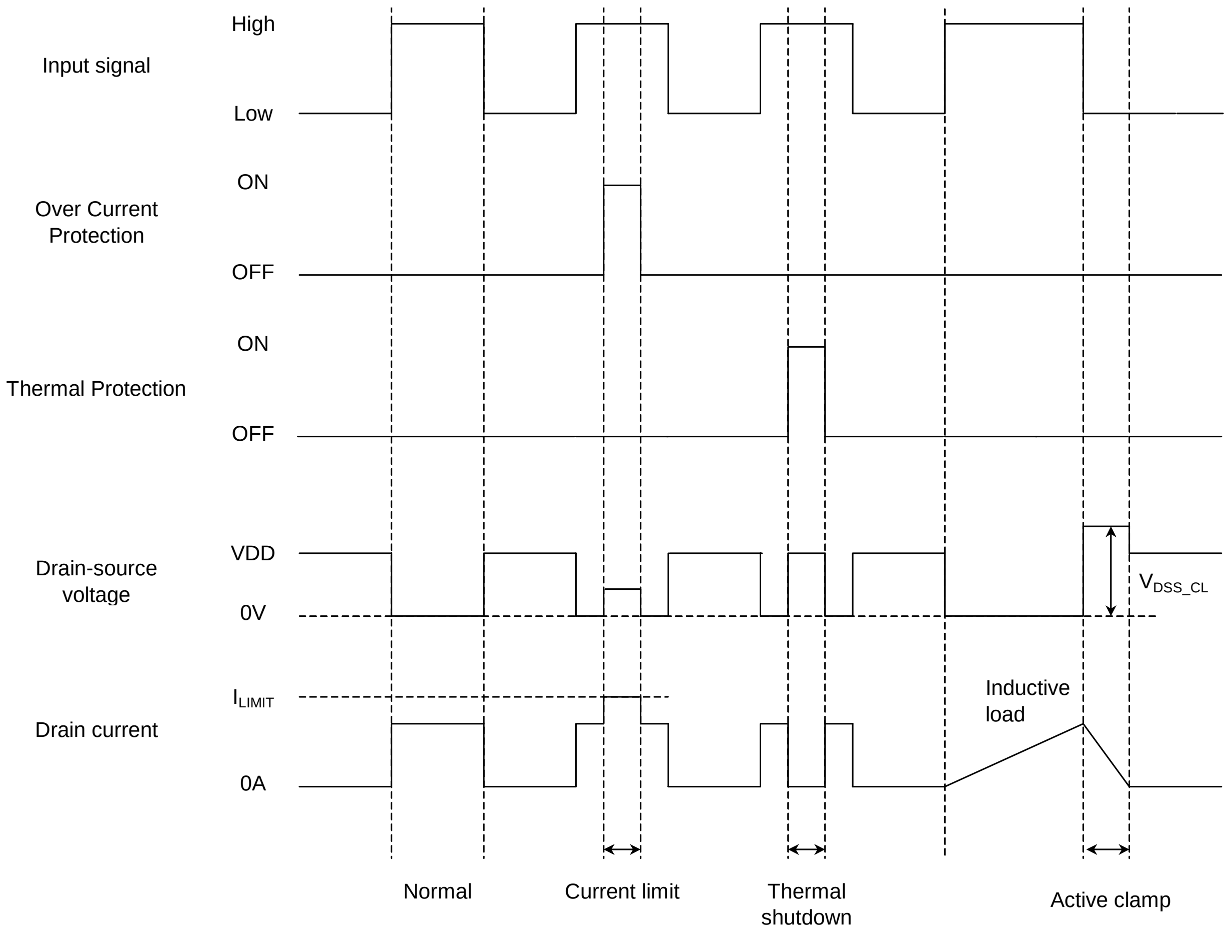
(Unless otherwise noted, V_{DS}=13V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Clamp Voltage	V_{DSS_CL}	V_{IN}=0V, I_D=1mA	43	–	–	V
Input Threshold Voltage	V_{th}	V_{DS}=13V, I_D=10mA	0.65	0.9	1.15	V
Protection Circuit Function Input Voltage Range	V_{IN_opr}		2.64	–	5.5	V
Zero-gate-voltage drain Current	I_{DSS}	V_{IN}=0V, V_{DS}=40V	–	–	1	µA
Input Current 1 (at Normal Operation)	I_{IN1}	V_{IN}=5V	–	80	110	µA
Input Current 2 (at Normal Operation)	I_{IN2}	V_{IN}=3.3V	–	65	90	µA
Input Current 3 (at OCP Operation)	I_{IN3}	V_{IN}=5V, V_{DD}=13V	–	160	200	µA
Input Current 4 (at OCP Operation)	I_{IN4}	V_{IN}=3.3V, V_{DD}=13V	–	105	130	µA
On-state Resistance 1	R_{DS_ON1}	V_{IN}=5V, I_D=0.5A	–	0.27	0.6	Ω
On-state Resistance 2	R_{DS_ON2}	V_{IN}=3.3V, I_D=0.5A	–	0.3	0.65	Ω
Drain-Source Voltage At Short Circuit Protection	$V_{DS(SC)}$	V_{IN}=5V	28	–	–	V
Over Current Protection 1	I_{LIMIT1}	V_{IN}=5V, V_{DD}=13V	1	1.6	2.3	A
Over Current Protection 2	I_{LIMIT2}	V_{IN}=3.3V, V_{DD}=13V	0.75	1.3	2	A
Turn-on Time 1	t_{ON1}	V_{IN}=0 to 5V, V_{DD}=13V, I_D=0.5A	–	5	–	µs
Turn-on Time 2	t_{ON2}	V_{IN}=0 to 3.3V, V_{DD}=13V, I_D=0.5A	–	8.5	–	µs
Turn-off Time 1	t_{OFF1}	V_{IN}=5 to 0V, V_{DD}=13V, I_D=0.5A	–	42	–	µs
Turn-off Time 2	t_{OFF2}	V_{IN}=3.3 to 0V, V_{DD}=13V, I_D=0.5A	–	35	–	µs
Source–Drain Voltage Difference	V_{PDSD}	V_{IN}=0V, I_{DR}=1A	–	0.95	1.25	V

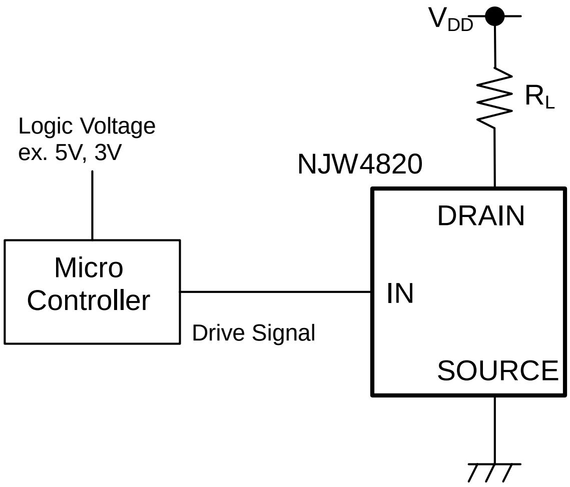
■ TIMING CHART

ON, OFF Switching Time (V_{IN}=0 to 5V, V_{DS}=13V, I_D=0.5A)



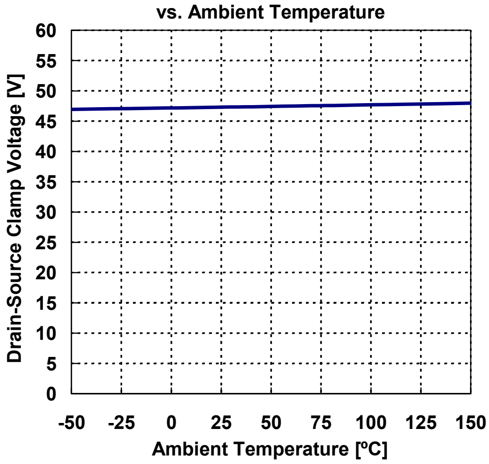


■ TYPICAL APPLICATION

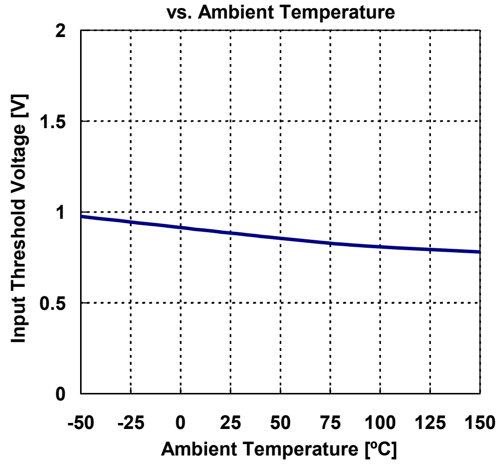


■ CHARACTERISTICS

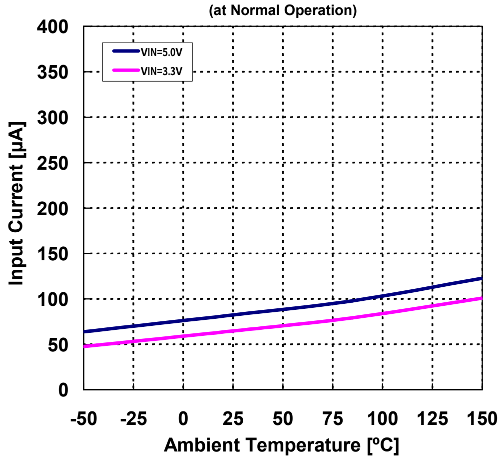
Drain-Source Clamp Voltage
vs. Ambient Temperature



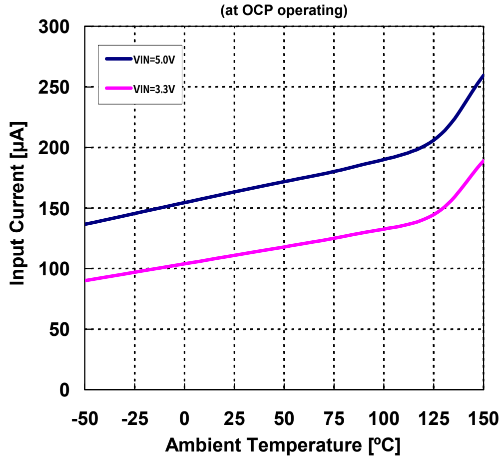
Input Threshold Voltage
vs. Ambient Temperature



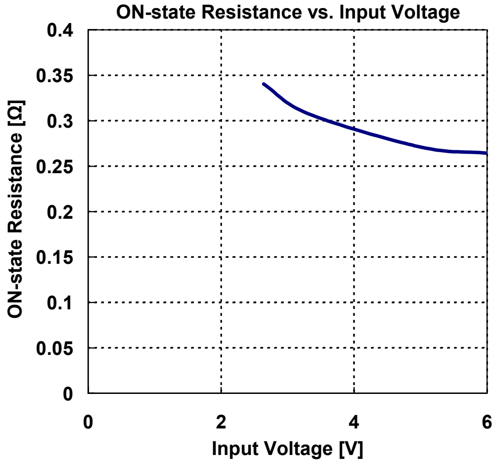
Input Current vs. Ambient Temperature
(at Normal Operation)



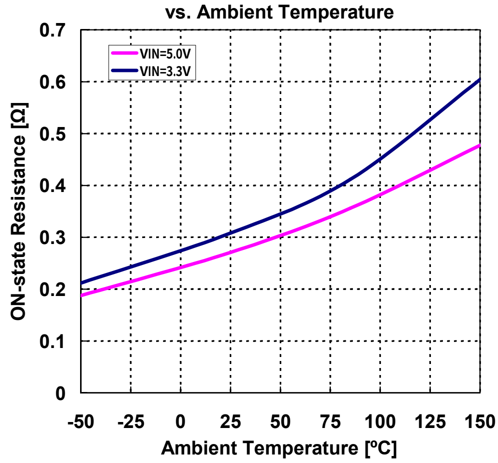
Input Current vs. Ambient Temperature
(at OCP operating)



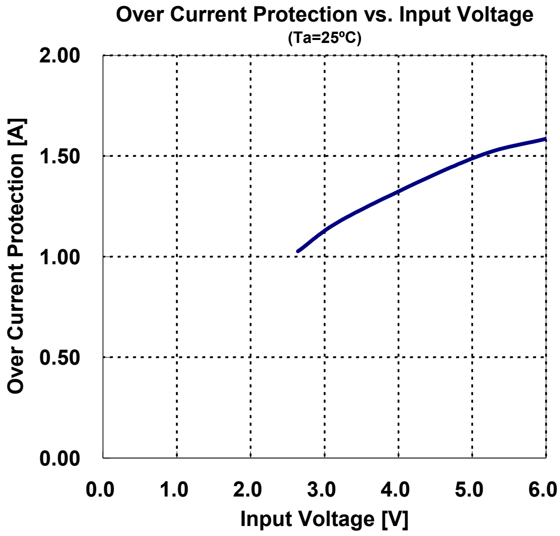
ON-state Resistance vs. Input Voltage

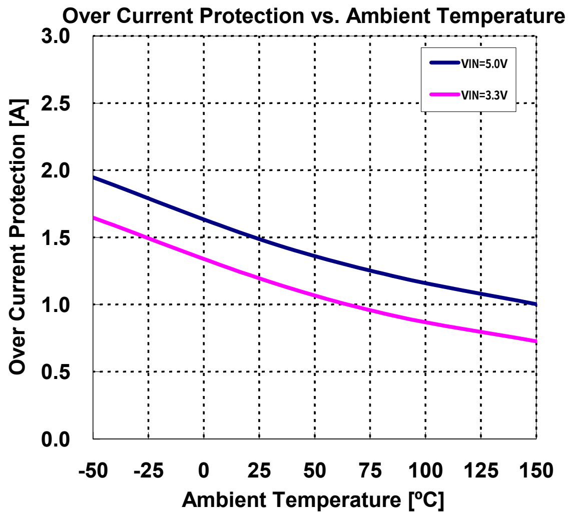


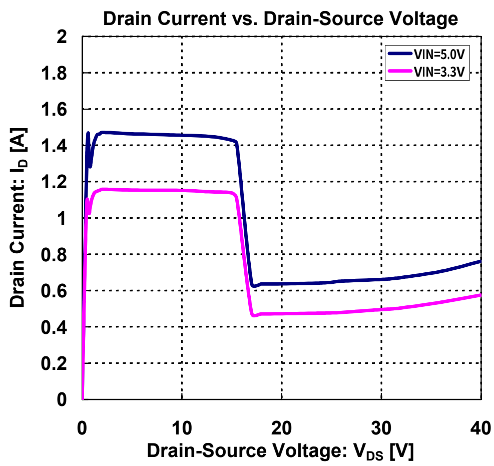
ON-state Resistance
vs. Ambient Temperature

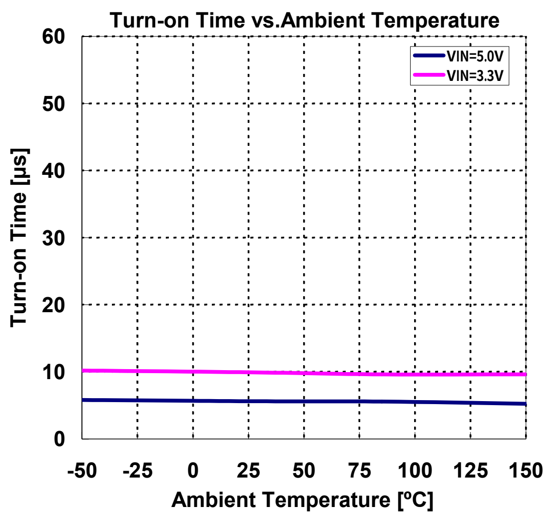


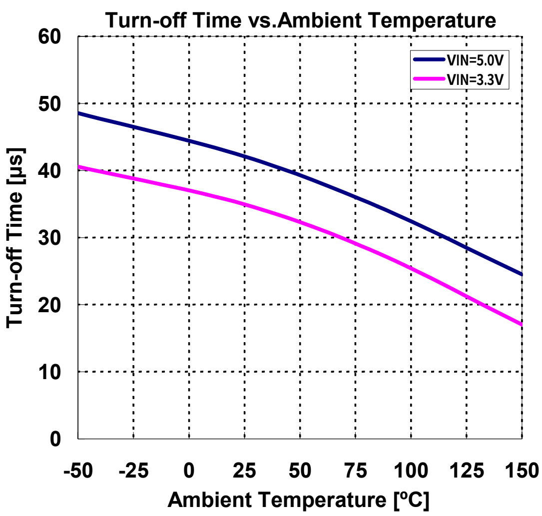
■ CHARACTERISTICS

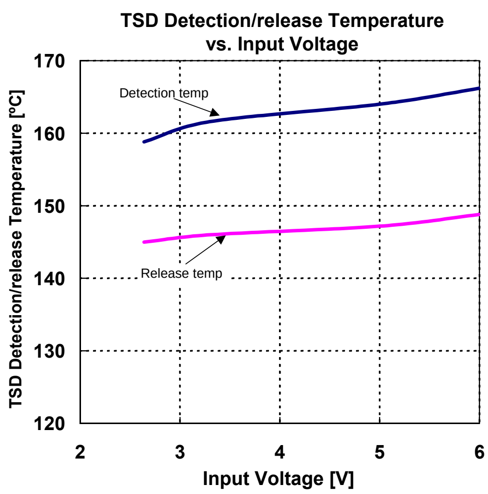












■ Regarding Active Clamp Capacity of High/Low side Switch Products

● What is "Active Clamp Capacity".

The IC might suffer to damage by the inductive kickback at the transient time of ON state to OFF state, when an inductive load such as a solenoid or motor is used for the load of the high-side/low-side switch.

The protection circuit for the inductive kickback is the active clamp circuit. The energy that can be tolerated by the active clamp circuit is called "Active Clamp Capacity (E_{AS})".

When using an inductive load to the high-side/low-side switch, you should design so that the E_{SW} does not exceed the active clamp capability.

● IC operation without an external protection parts (Fig 1)

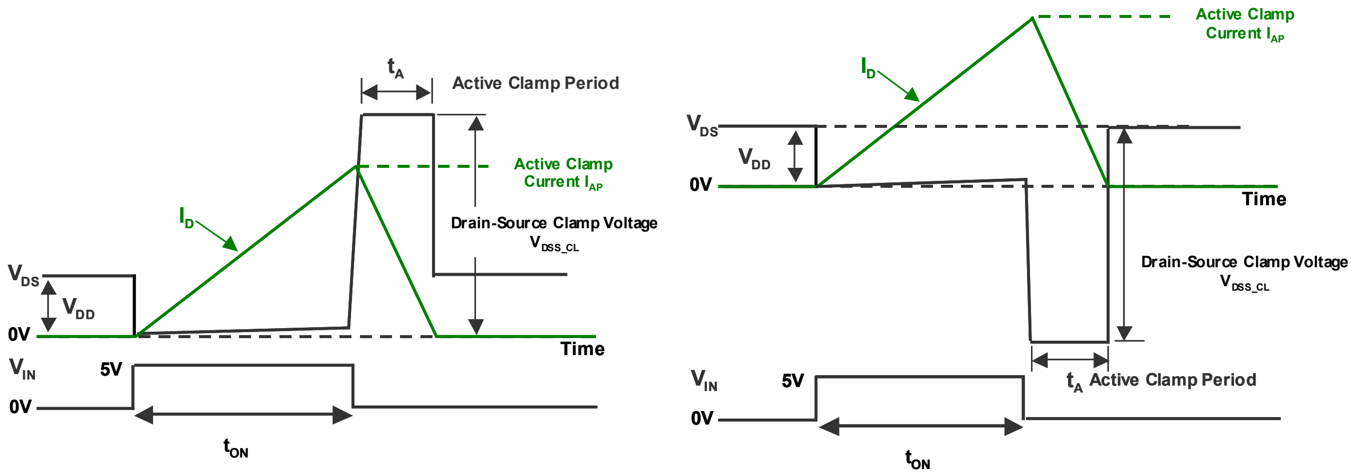


Fig1. Active Clamp Waveform (Left: Low-side Switch / Light High-side Switch)

At when the V_{IN} turns off, the drain-source voltage (V_{DS}) increases rapidly by the behavior of the inductive load that is keeping current flowing. However, it will be clamped at V_{DSS_CL} by the active clamp circuit. At the same time, the drain current is flowed by adjusting the gate voltage of the output transistor, and the energy is dissipated at the output transistor. The energy: E_{SW} is shown by the following formula.

$$E_{SW} = \int_0^{t_A} V_{DS}(t) \cdot I_D(t)dt = \frac{1}{2} L I_{AP}{}^2 \cdot \frac{V_{DSS\_CL}}{V_{DSS\_CL} - V_{DD}}$$

The E_{SW} is consumed inside IC as heat energy. However, the thermal shutdown does not work when the V_{IN} is 0V. Therefore in worst case the IC might break down. When using the active clamp, you should design E_{SW} does not exceed the E_{AS}.

- Application Hint

The simplest protection example is to add an external flywheel diode at the load to protect IC from an inductive kickback. (Fig.2)

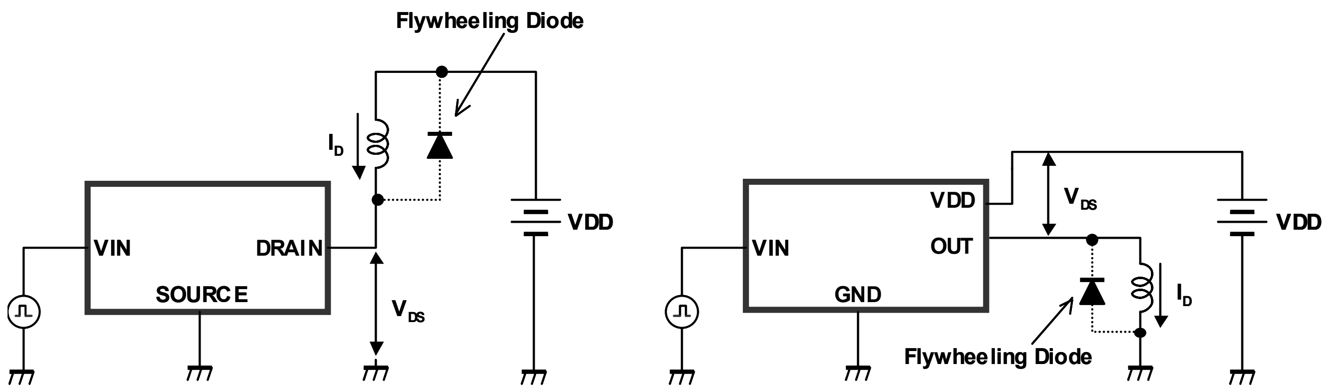


Fig 2. Application Circuit of Inductance Load Driving (Left: Low-side Switch / Light High-side Switch)