Low Noise Amplifier with Bypass for 5 GHz band

■ FEATURES

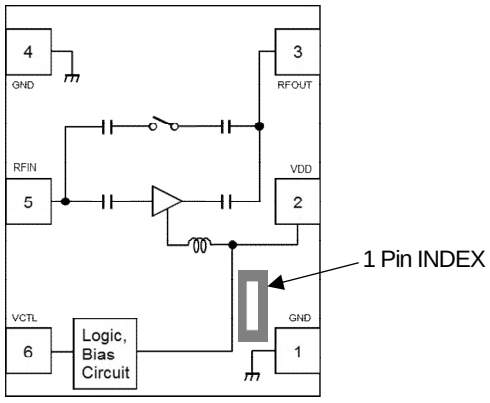
- Wide frequency range 4900MHz to 5950MHz
- Low operating voltage 1.5V to 3.3 V
- Low current 5.0/3.5mA typ. @ V_{DD}=2.8/1.8V
- High gain
  15.0dB typ. @ V_{DD}=2.8V, f_{RF}=5500 MHz
- Low noise figure
  1.1dB typ. @ V_{DD}=2.8V, f_{RF}=5500MHz
- High IIP3
  +2.0dBm typ.@V_{DD}=2.8V,f_{RF}=5500MHz+5501MHz
- Low insertion loss (bypass mode)
  3.5dB typ.@ V_{DD}=2.8V, f_{RF}=5500MHz
- Ultra-small package size 1.1 x 0.7 x 0.37mm typ.
- RoHS compliant and Halogen Free, MSL1

■ APPLICATION

- LTE-U/LAA receive application
- WiMAX 5GHz receive application
- WLAN 5GHz receive application
- RF front-end modules, data cards, and other mobile applications

■ BLOCK DIAGRAM (EPFFP6-X2)

(Top view)



■ GENERAL DESCRIPTION

NJG1182UX2 is low noise amplifier with bypass switch for 5GHz application such as LTE-U/LAA, which covers frequency from 4900MHz to 5950MHz.

NJG1182UX2 is able to select LNA active mode or bypass mode by low control voltage. This LNA achieves low noise figure and high linearity.

Integrated ESD protection device on each port achieves excellent ESD robustness.

A very small and ultra-thin package EPFFP6-X2 is adopted.

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

V_{CTL}	Mode
H	LNA active mode
L	Bypass mode

■ PIN CONFIGURATION

PIN NO.	SYMBOL	DESCRIPTION
1	GND	Ground
2	VDD	Power supply
3	RFOUT	RF output
4	GND	Ground
5	RFIN	RF input
6	VCTL	Control voltage

■ PRODUCT NAME INFORMATION

NJG1182 UX2 (TE1)
| | |
Part number Package Taping form

■ ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
NJG1182UX2	EPFFP6-X2	Yes	Yes	Ni/Pd/Au	5	0.7	5,000

■ ABSOLUTE MAXIMUM RATINGS

T_a = 25°C, Z_s = Z_l = 50 Ω

PARAMETER	SYMBOL	RATINGS	UNIT
Operating voltage	V_{DD}	5.0	V
Control voltage	V_{CTL}	5.0	V
Input power	P_{IN}	+15 (1)	dBm
Power dissipation	P_D	430 (2)	mW
Operating temperature	T_{opr}	-40 to +105	°C
Storage temperature	T_{stg}	-55 to +150	°C

(1): V_{DD}=2.8V

(2): 4-layer FR4 PCB with through-hole (101.5x114.5mm), T_j=150°C

■ ELECTRICAL CHARACTERISTICS 1 (DC)

General condition: T_a=+25°C, with application circuit

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating voltage	V_{DD}		1.5	-	3.3	V
Control voltage (High)	$V_{CTL(H)}$		1.3	1.8	3.3	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.3	V
Operating current 1	$I_{DD}1$	RF OFF, V_{DD}=2.8V, V_{CTL}=1.8V	-	5.0	8.0	mA
Operating current 2	$I_{DD}2$	RF OFF, V_{DD}=1.8V, V_{CTL}=1.8V	-	3.5	8.0	mA
Operating current 3	$I_{DD}3$	RF OFF, V_{DD}=2.8V, V_{CTL}=0V	-	20	60	μA
Operating current 4	$I_{DD}4$	RF OFF, V_{DD}=1.8V, V_{CTL}=0V	-	10	60	μA
Control current	I_{CTL}	RF OFF, V_{CTL}=1.8V	-	7	20	μA

■ELECTRICAL CHARACTERISTICS 2 (LNA active mode)

General condition: V_{DD}=2.8V, V_{CTL}=1.8V, f_{RF}=5500MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Small signal gain1	Gain1	Exclude PCB & connector losses *1	12.0	15.0	17.5	dB
Noise figure1	NF1	Exclude PCB & connector losses *2	-	1.1	1.7	dB
Input power at 1dB gain compression point1(1)	P-1dB(IN) 1(1)		-16.0	-11.0	-	dBm
Input 3rd order intercept point1(1)	IIP3_1(1)	f1=f_{RF}, f2= f_{RF}+1MHz, P_{IN}=-30dBm	-5.0	+2.0	-	dBm
RF IN return loss1(1)	RLi1(1)		8.0	16.0	-	dB
RF OUT return loss1(1)	RLo1(1)		5.0	8.0	-	dB
Gain settling time1(1)	Ts1(1)	Bypass to LNA active mode to be within 1 dB of the final gain	-	1.0	2.5	μs
Gain settling time1(2)	Ts1(2)	LNA active to Bypass mode to be within 1 dB of the final insertion loss	-	0.8	2.5	μs

*1: PCB and connector losses: 0.64 dB

*2: PCB and connector losses: 0.30 dB

■ ELECTRICAL CHARACTERISTICS 3 (Bypass mode)

General condition: V_{DD}=2.8V, V_{CTL}=0V, f_{RF}=5500MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion Loss1	Loss1	Exclude PCB & connector losses *1	-	3.5	5.0	dB
Input power at 1dB compression point1(2)	P-1dB(IN) 1(2)		+2.0	+7.5	-	dBm
Input 3rd order intercept point1(2)	IIP3_1(2)	f1=f_{RF}, f2=f_{RF}+1MHz, P_{IN}=-10dBm	+10.0	+18.0	-	dBm
RF IN return loss1(2)	RLi1(2)		6.0	13.0	-	dB
RF OUT return loss1(2)	RLo1(2)		4.0	6.0	-	dB

*1: PCB and connector losses: 0.64 dB

■ **ELECTRICAL CHARACTERISTICS 4 (LNA active mode)**

General condition: V_{DD}=1.8V, V_{CTL}=1.8V, f_{RF}=5500MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Small signal gain2	Gain2	Exclude PCB & connector losses *1	-	14.5	-	dB
Noise figure2	NF2	Exclude PCB & connector losses *2	-	1.4	-	dB
Input power at 1dB gain compression point2(1)	P-1dB(IN) 2(1)			-13.0		dBm
Input 3rd order intercept point2(1)	IIP3_2(1)	f1=f_{RF}, f2= f_{RF}+1MHz, P_{IN}=-30dBm	-	-1.0	-	dBm
RF IN return loss2(1)	RLi2(1)		-	11.0	-	dB
RF OUT return loss2(1)	RLo2(1)		-	8.0	-	dB
Gain settling time2(1)	Ts2(1)	Bypass to LNA active mode To be within 1 dB of the final gain	-	2.0	-	μs
Gain settling time2(2)	Ts2(2)	LNA active to Bypass mode To be within 1 dB of the final insertion loss	-	0.8	-	μs

*1: PCB and connector losses: 0.64 dB

*2: PCB and connector losses: 0.30 dB

■ **ELECTRICAL CHARACTERISTICS 5 (Bypass mode)**

General condition: V_{DD}=1.8V, V_{CTL}=0V, f_{RF}=5500MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit

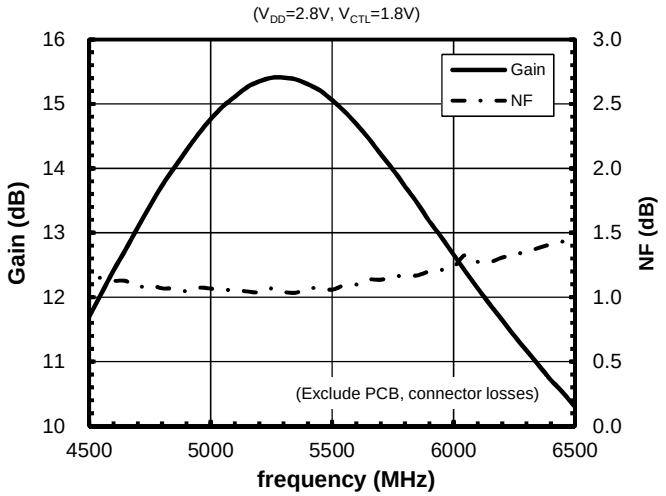
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion Loss2	Loss2	Exclude PCB & connector losses *1	-	3.5	-	dB
Input power at 1dB compression point2(2)	P-1dB(IN) 2(2)		-	+7.0	-	dBm
Input 3rd order intercept point2(2)	IIP3_2(2)	f1=f_{RF}, f2=f_{RF}+1MHz, P_{IN}=-10dBm	-	+18.0	-	dBm
RF IN return loss2(2)	RLi2(2)		-	13.0	-	dB
RF OUT return loss2(2)	RLo2(2)		-	7.0	-	dB

*1: PCB and connector losses: 0.64 dB

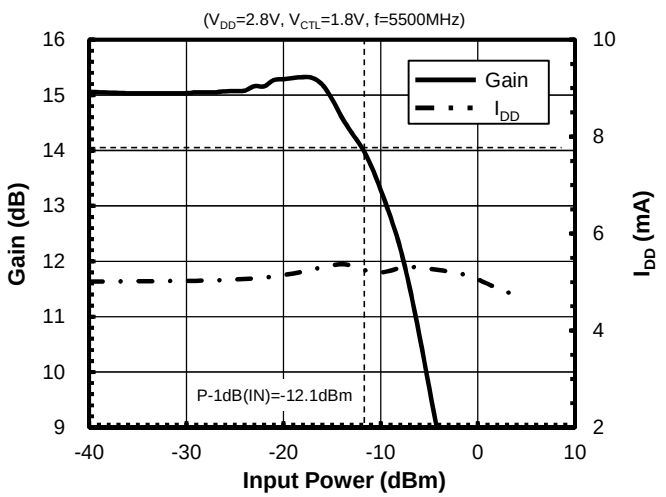
■ **ELECTRICAL CHARACTERISTICS** (LNA active mode)

Conditions: V_{DD}=2.8V, V_{CTL}=1.8V, f_{RF}=5500MHz, T_a=+25°C, Z_S=Z_l=50Ω, with application circuit

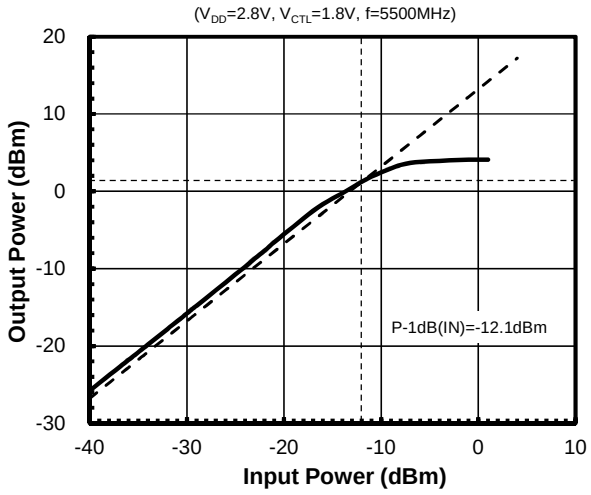
Gain, NF vs. frequency



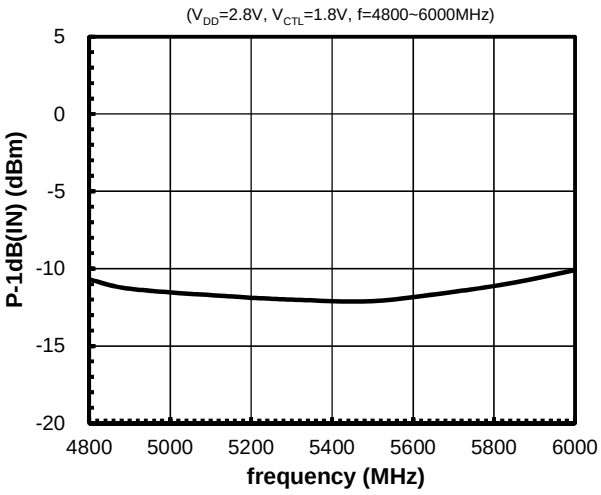
Gain, I_{DD} vs. Pin



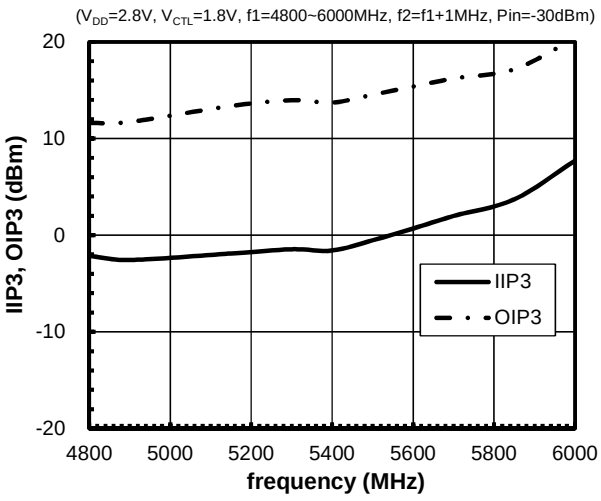
Pout vs. Pin



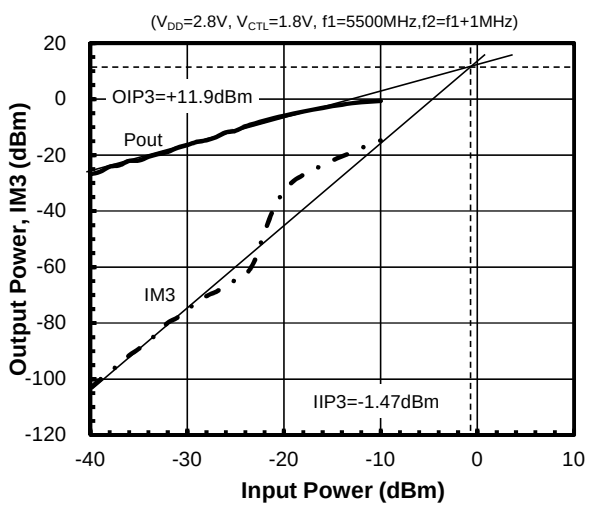
P-1dB(IN) vs. frequency



IIP3, OIP3 vs. frequency



Pout, IM3 vs. Pin

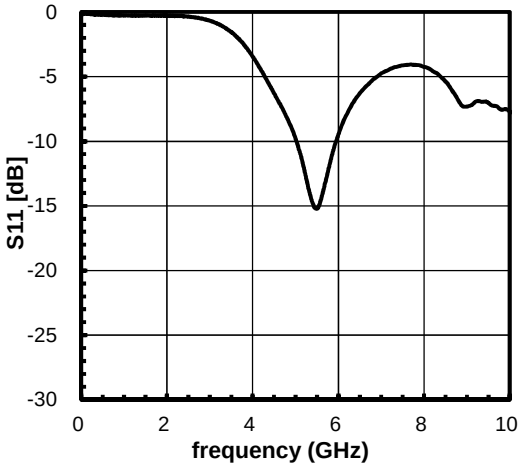


■ **ELECTRICAL CHARACTERISTICS** (LNA active mode)

Conditions: V_{DD}=2.8V, V_{CTL}=1.8V, f_{RF}=50MHz to 10000MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit

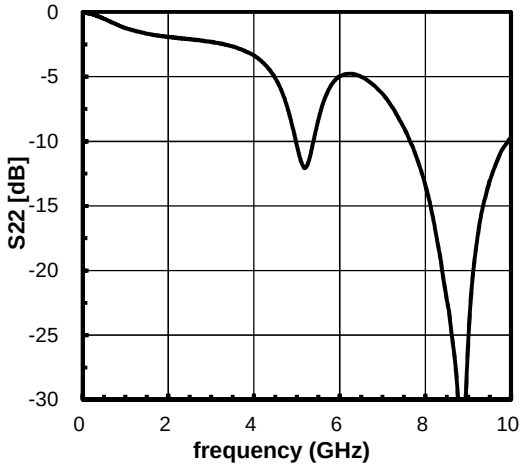
S11 vs. frequency

(V_{DD} = 2.8V, V_{CTL}=1.8V)



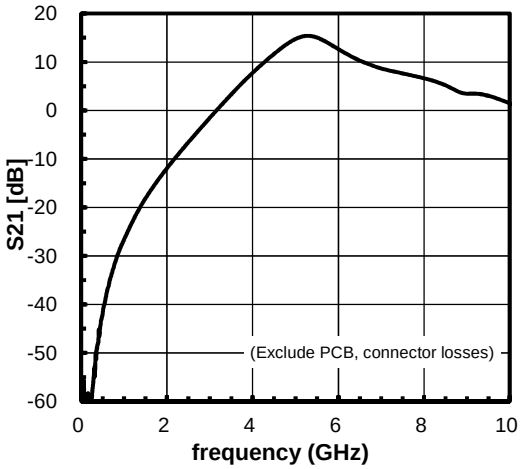
S22 vs. frequency

(V_{DD} = 2.8V, V_{CTL}=1.8V)



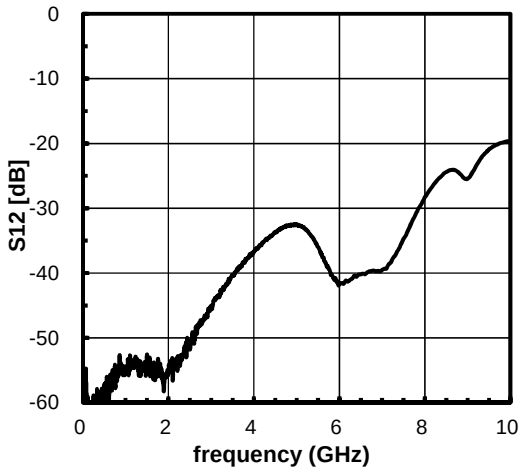
S21 vs. frequency

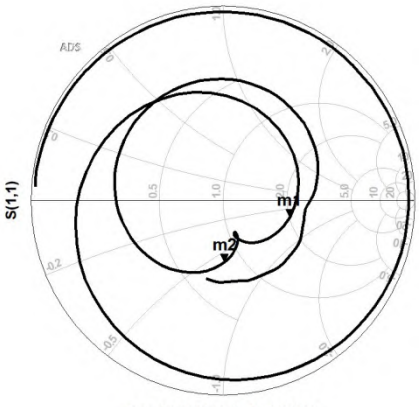
(V_{DD} = 2.8V, V_{CTL}=1.8V)



S12 vs. frequency

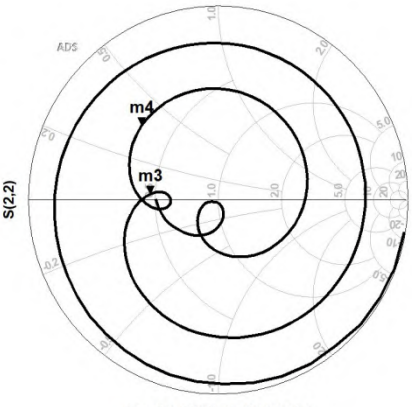
(V_{DD} = 2.8V, V_{CTL}=1.8V)





m1
freq=4.900GHz
S(1,1)=0.358 / -14.219
impedance = Z0 * (2.010 - j0.406)

m2
freq=5.950GHz
S(1,1)=0.317 / -88.662
impedance = Z0 * (0.828 - j0.585)



m3
freq=4.900GHz
S(2,2)=0.360 / 175.137
impedance = Z0 * (0.472 + j0.033)

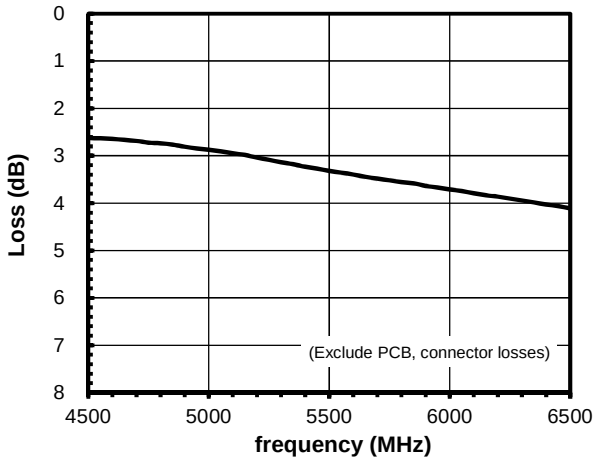
m4
freq=5.950GHz
S(2,2)=0.558 / 136.434
impedance = Z0 * (0.325 + j0.363)

■ **ELECTRICAL CHARACTERISTICS** (Bypass mode)

Conditions: V_{DD}=2.8V, V_{CTL}=0V, f_{RF}=5500MHz, T_a=+25°C, Z_S=Z_L=50Ω, with application circuit

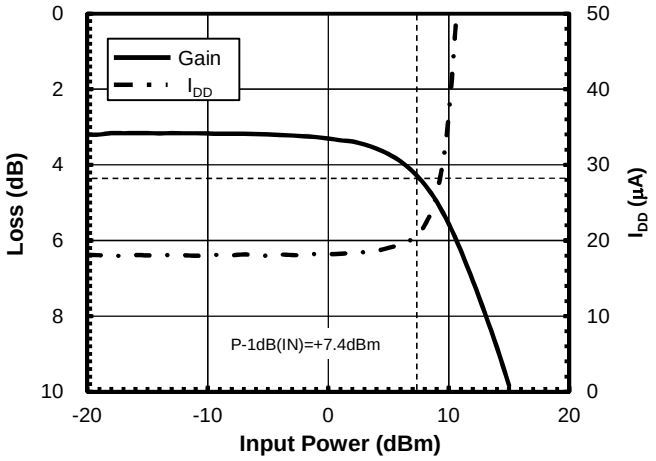
Loss vs. frequency

(V_{DD}=2.8V, V_{CTL}=0V)



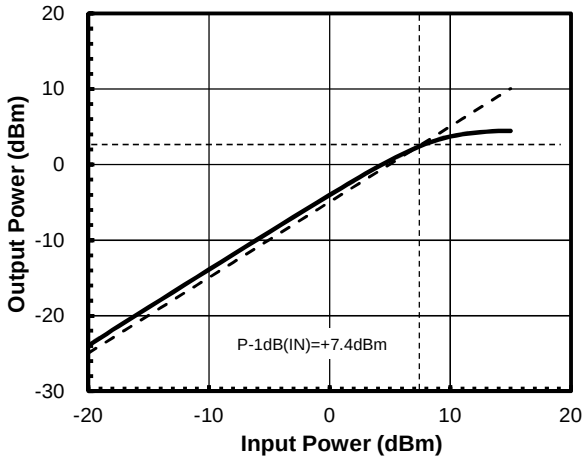
Loss, I_{DD} vs. Pin

(V_{DD}=2.8V, V_{CTL}=0V, f=5500MHz)



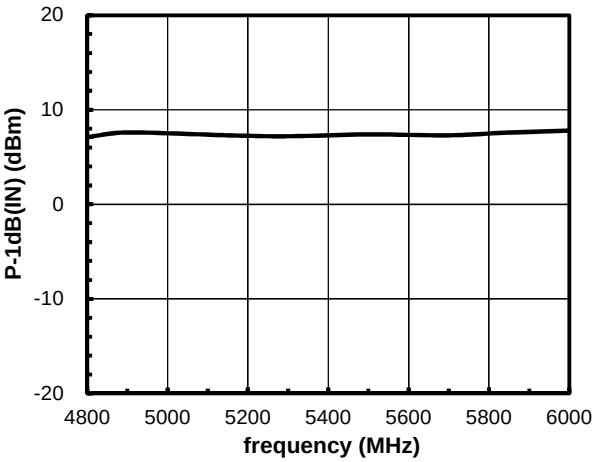
Pout vs. Pin

(V_{DD}=2.8V, V_{CTL}=0V, f=5500MHz)



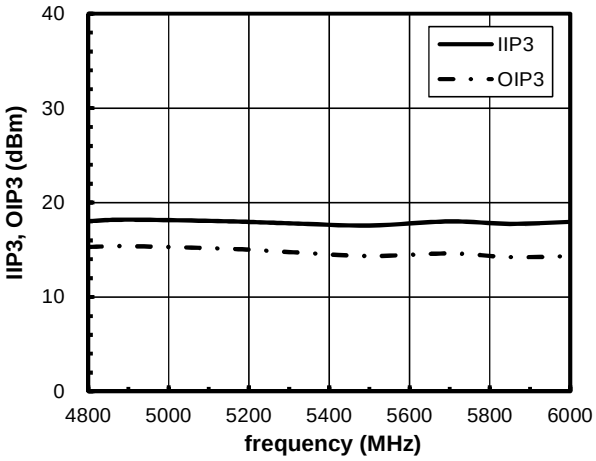
P-1dB(IN) vs. frequency

(V_{DD}=2.8V, V_{CTL}=0V, f=4800~6000MHz)



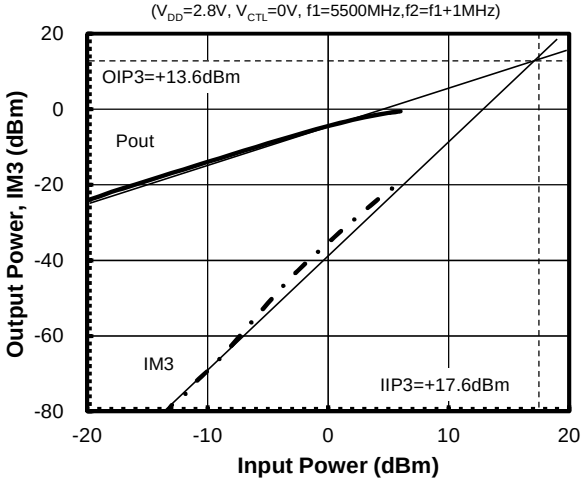
IIP3, OIP3 vs. frequency

(V_{DD}=2.8V, V_{CTL}=0V, f1=4800~6000MHz, f2=f1+1MHz, Pin=-10dBm)



Pout, IM3 vs. Pin

(V_{DD}=2.8V, V_{CTL}=0V, f1=5500MHz,f2=f1+1MHz)

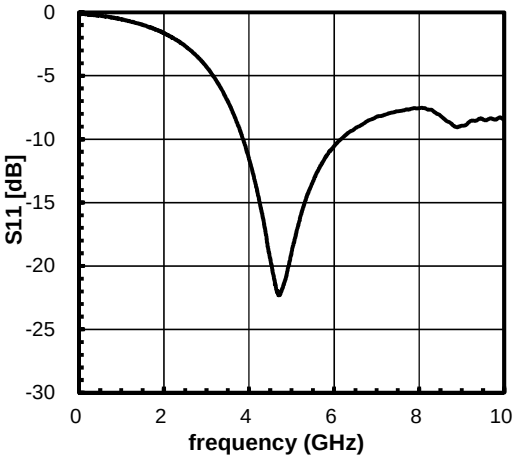


■ **ELECTRICAL CHARACTERISTICS** (Bypass mode)

Conditions: V_{DD}=2.8V, V_{CTL}=0V, f_{RF}=50MHz to 10000MHz, T_a=+25°C, Z_S=Z_L=50Ω, with application circuit

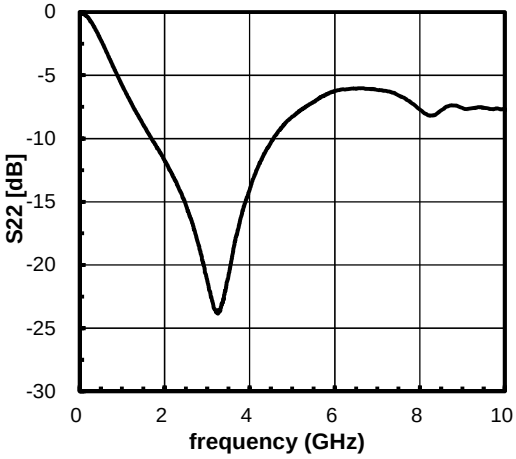
S11 vs. frequency

(V_{DD} = 2.8V, V_{CTL}=0V)



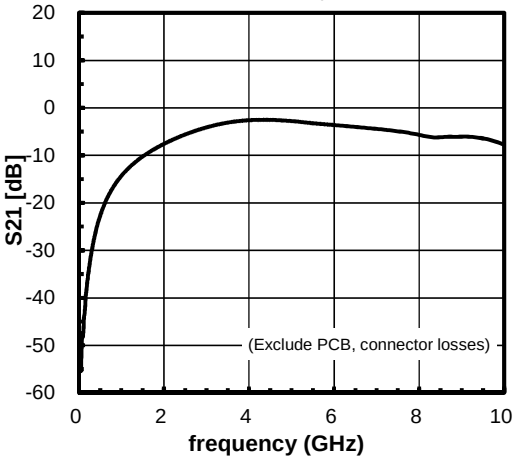
S22 vs. frequency

(V_{DD} = 2.8V, V_{CTL}=0V)



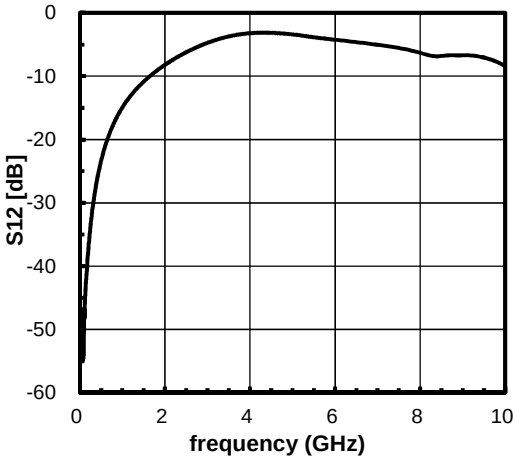
S21 vs. frequency

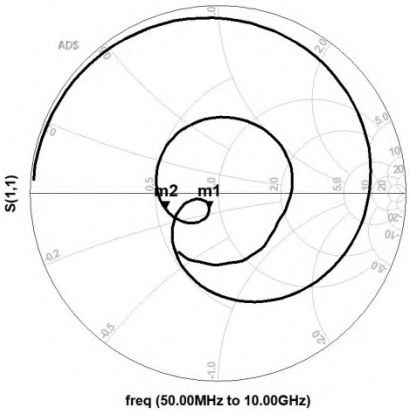
(V_{DD} = 2.8V, V_{CTL}=0V)



S12 vs. frequency

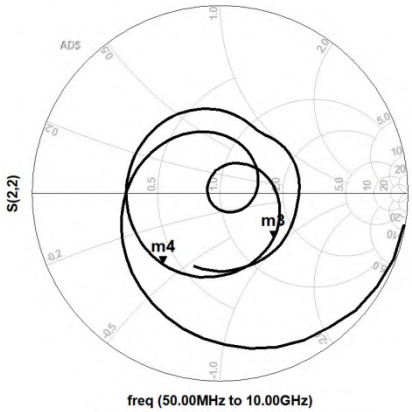
(V_{DD} = 2.8V, V_{CTL}=0V)





m1
freq=4.900GHz
S(1,1)=0.095 / -119.355
impedance = Z0 * (0.899 - j0.151)

m2
freq=5.950GHz
S(1,1)=0.290 / -163.234
impedance = Z0 * (0.559 - j0.102)

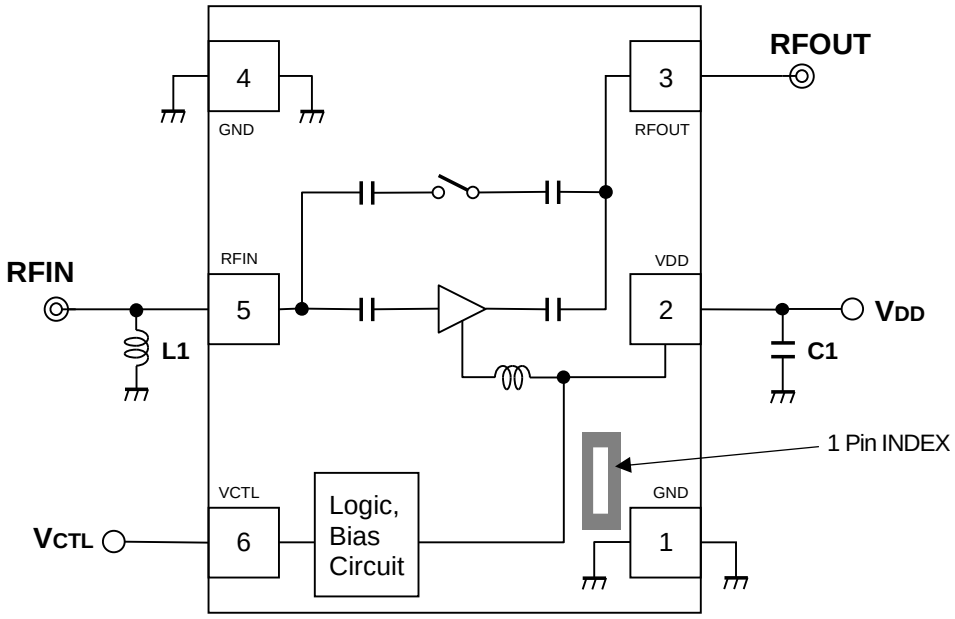


m3
freq=4.900GHz
S(2,2)=0.373 / -40.290
impedance = Z0 * (1.510 - j0.846)

m4
freq=5.950GHz
S(2,2)=0.485 / -128.876
impedance = Z0 * (0.415 - j0.409)

■ APPLICATION CIRCUIT

(Top view)



Parts list

Part ID	Value	Notes
L1	1.6nH	LQP03TN_02 series (MURATA)
C1	4700pF	GRM03 series (MURATA)

■ **NF MEASUREMENT BLOCK DIAGRAM**

Measuring instruments

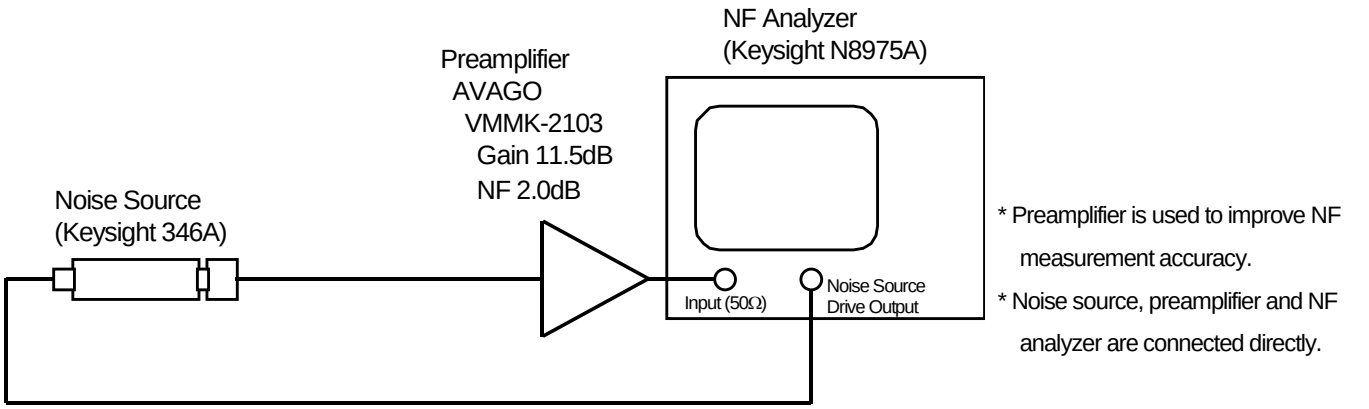
NF Analyzer : Keysight N8975A
Noise Source : Keysight 346A

Setting the NF analyzer

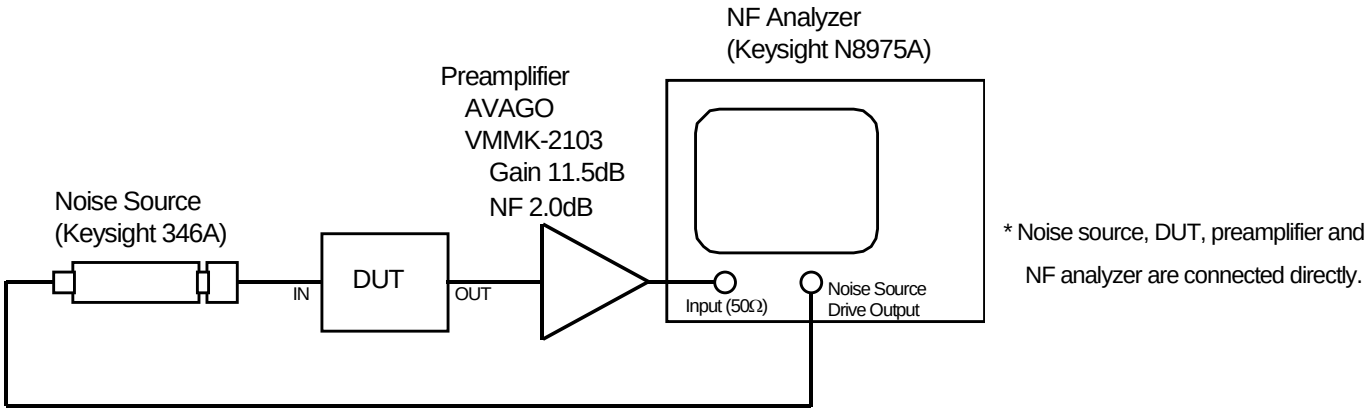
Measurement mode form
- Device under test : Amplifier
- System downconverter : off

Mode setup form
- Sideband : LSB

Averages : 16
Average mode : Point
Bandwidth : 4MHz
Loss comp : off
Tcold : setting the temperature of noise source (305.15K)



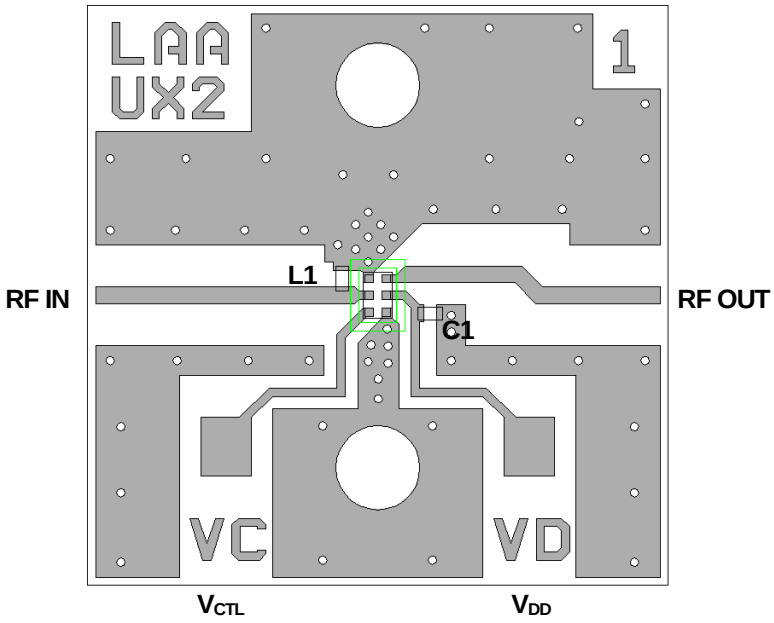
Calibration setup



Measurement Setup

■ EVALUATION BOARD

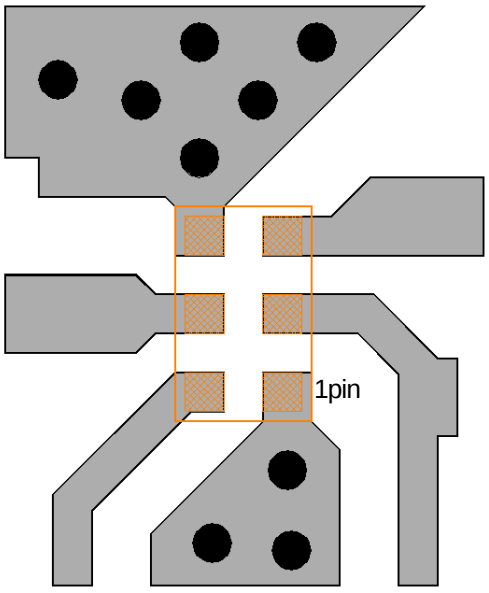
(Top View)

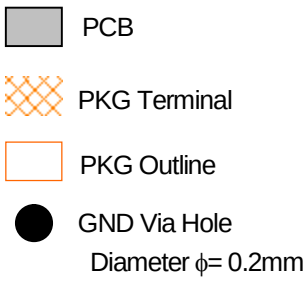


PCB Information

Substrate: FR-4
Thickness: 0.2mm
Microstrip line width: 0.4mm (Z_0=50Ω)
Size: 14.0mm x 14.0mm

< PCB LAYOUT GUIDELINE>



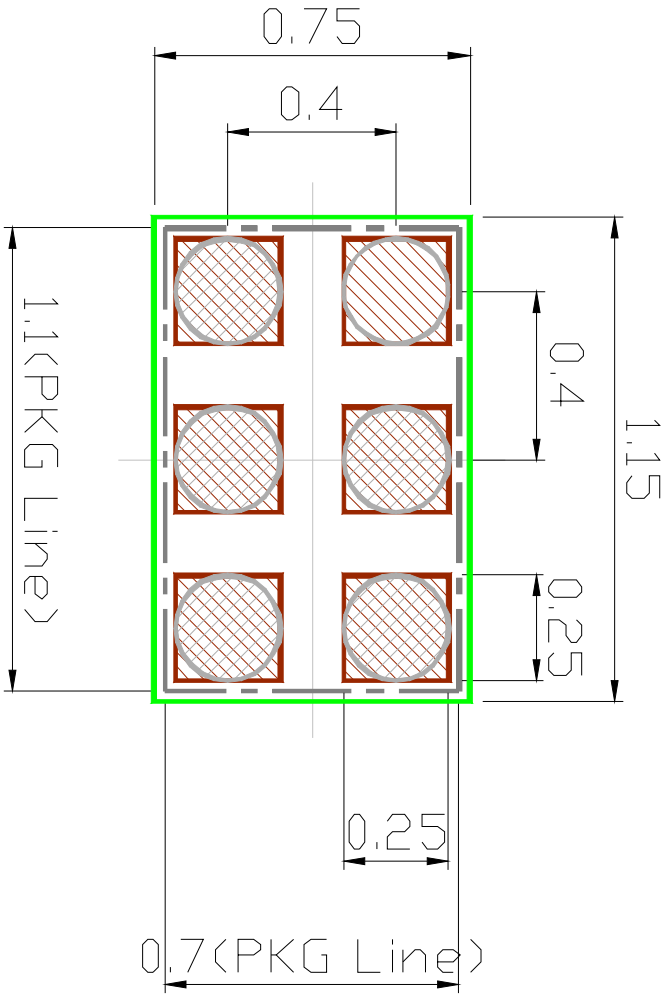


PRECAUTIONS

- All external parts should be placed as close as possible to the IC.
- For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.

■ **RECOMMENDED FOOTPRINT PATTERN** (EPFFP6-X2)

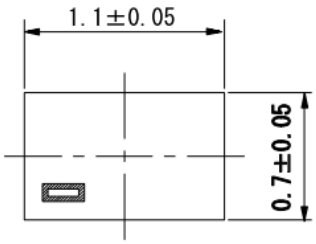
: Land
: Mask (Open area) *Metal mask thickness: 100 μm
: Resist (Open area)



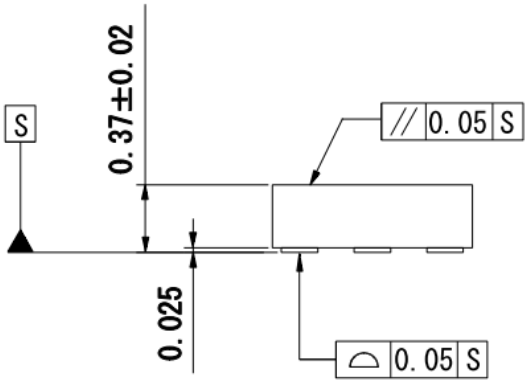
Unit: mm

■ **PACKAGE OUTLINE (EPFFP6-X2)**

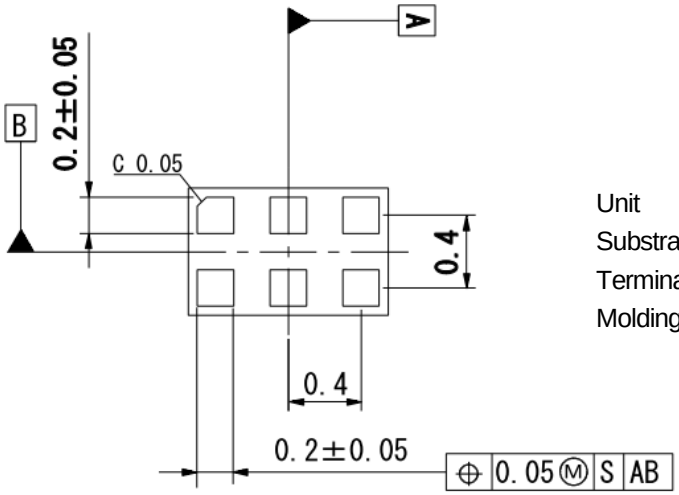
TOP VIEW



SIDE VIEW



BOTTOM VIEW

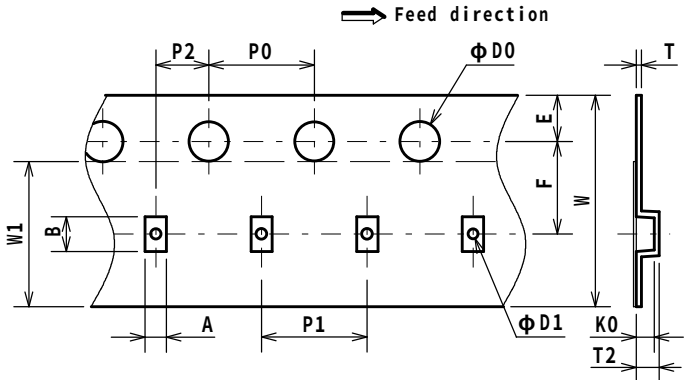


Unit	: mm
Substrate	: FR4
Terminal treat	: Ni/Pd/Au
Molding material	: Epoxy resin

■ PACKING SPECIFICATION (EPFFP6-X2)

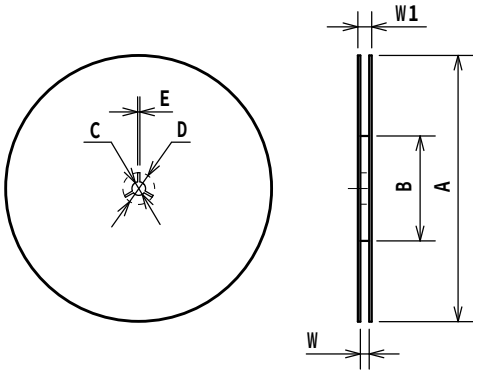
TAPING DIMENSIONS

Unit: mm



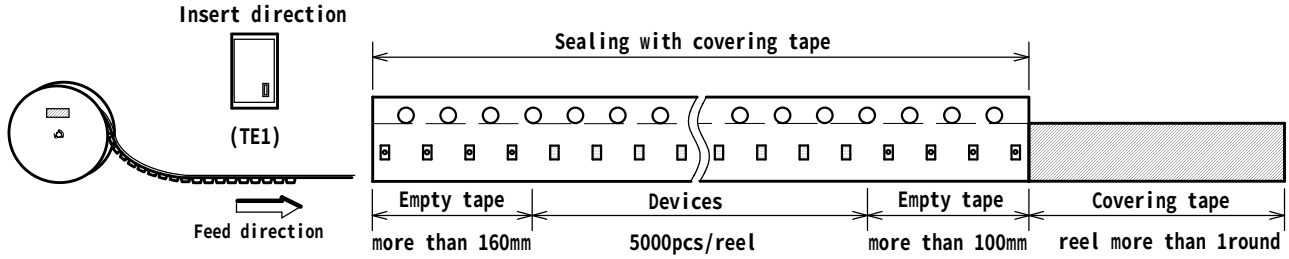
SYMBOL	DIMENSION	REMARKS
A	0.85±0.03	BOTTOM DIMENSION
B	1.25±0.03	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	0.35±0.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.2±0.05	
T2	0.75	
K0	0.45±0.05	
W	$8.0^{+0.3}_{-0.1}$	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

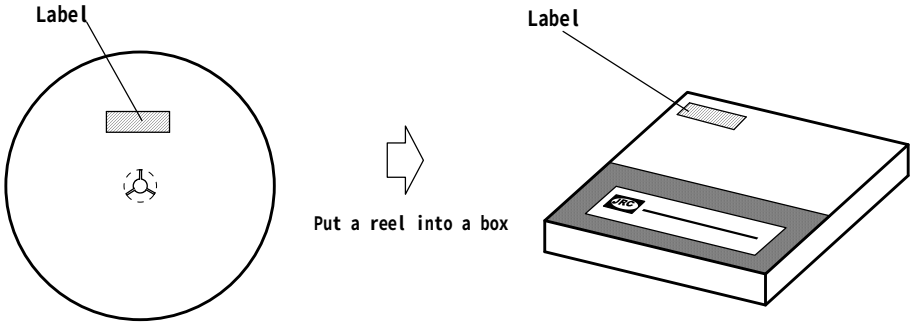


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	ϕ 60^{+1}_{0}
C	ϕ 13±0.2
D	ϕ 21±0.8
E	2±0.5
W	$9^{+0.3}_{0}$
W1	11.4±0.1

TAPING STATE



PACKING STATE



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